Integrated Circuit Systems, Inc.

ICS9222-01

Dual Memory Clock Generator

General Description

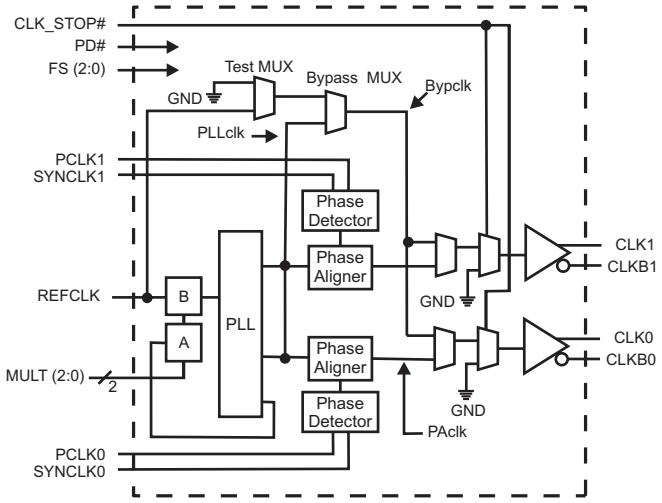
The **ICS9222-01** is a High-speed clock generator providing two channels up to 450 MHz differential clock source for direct Rambus_memory system. It includes two independent DDLL's (Distributed Delay locked loop) and phase detection mechanisms to synchronize eachdirect Rambus_ channel clock to an external system clock. **ICS9222-01** provides a solution for a broad range of Direct Rambus memory applications. The device works in conjunction with the ICS964S101, as well as 9250-22 and others (depending on chipset).

The **ICS9222-01** power management support system turns "off" the Rambus channel clock to minimize power consumption for mobile and other power sensitive applications. In "clock off" mode the device remains "on" while the output is disabled, allowing fast transitions between clock-off and clock–on states. In "power down" mode it completely powers down for minimum power dissipation.

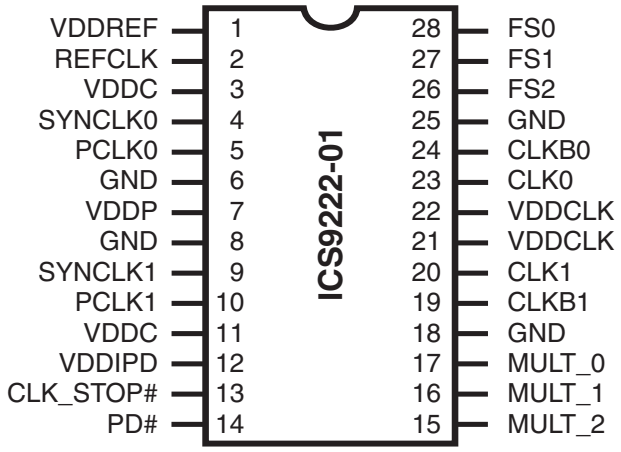
Features

- Compatible with all Direct Rambus™ based ICs
- Up to 450 MHz differential clock source for direct Rambus™ memory system
- Cycle to cycle jitter is less than 100 ps
- 3.3 ± 5% supply
- Synchronization flexibility: Supports systems that need clock domains of Rambus channel to synchronize with system or processor clock, or systems that do not require synchronization of the Rambus clock to another system clock.
- Excellent power management support
- REFCLK input is from the main clock generator such as a 9250-22.

Block Diagram



Pin Configuration



28-Pin TSSOP

Pin Descriptions

Pin #	Name	Type	Description
1, 7, 21, 22	VDD	PWR	3.3 V power supply
2	REFCLK	IN	Reference clock
3, 11	VDDC	PWR	Power for phase aligners
6, 8, 18, 25	GND	PWR	Ground
4, 5, 9, 10	PCLK, SYNCLK	IN	Phase controller input, used to drive a phase aligner that adjusts the phase of the busclk.
12	VDDIPD	PWR	Voltage for phase detector inputs
13	CLK_ STOP#	IN	Active low output enable/disable for CLK/CLKB
14	PD#	IN	3.3V CMOS active low power down, the device is powered down when the "(PD#) =0"
15, 16, 17	MULT (2:0)	IN	3.3V CMOS PLL Multiplier select, logic for selecting the multiply ratio for the PLL from the input REFCLK
19, 24	CLKB (1:0)	OUT	Clock output Complement
20, 23	CLK (1:0)	OUT	Clock output
26, 27, 28	FS (2:0)	IN	3.3V CMOS Mode control, used in selecting bypass, test, normal, and output test (OE)

PLL Divider Selection and PLL Values (PLLCLK=REFCLK*A/B)

MULT_0	MULT_1	MULT_2	A	B	CLK(1:0)/CLKB(1:0) w/ REFCLK= 50MHz	CLK(1:0)/CLKB(1:0) w/ REFCLK= 66MHz
0	0	0	4	1	Reserved	267MHz
0	0	1	9	2	Reserved	300
0	1	0	6	1	300	400
0	1	1	9	1	450	Reserved
1	0	0	8	3	Reserved	Reserved
1	0	1	16	3	Reserved	356
1	1	0	8	1	400	Reserved
1	1	1	10	1	Reserved	Reserved

Bypass and Test Mode Select

FS0	FS1	FS2	MODE	CLK (1:0)	CLKB (1:0)
0	0	0	Normal	CLK	CLKB
0	0	1	Supplier Test	Reserved	Reserved
0	1	0	OE	Tristate	Tristate
0	1	1	OE	Tristate	Tristate
1	0	0	Bypass	Non-aligned CLK	Non-aligned CLKB
1	0	1	Supplier Test	Reserved	Reserved
1	1	0	Test	REFCLK	REFCLKB
1	1	1	Reserved	Reserved	Reserved

Absolute Maximum Ratings

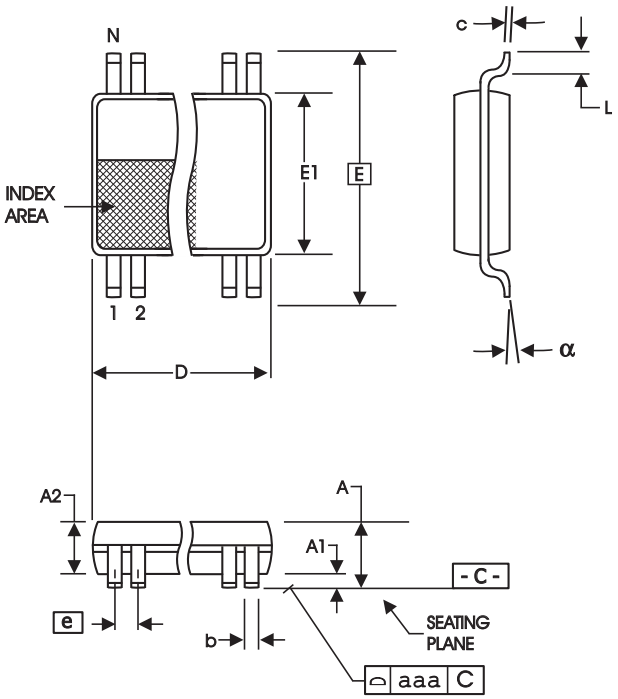
Supply Voltage . . . . . 4.0 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input / Supply / Outputs

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-10% (unless otherwise stated)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.465	V
REFCLK Input cycle time	$t_{CYCLE,IN}$	10	40	ns
Input Cycle-to-Cycle Jitter	$t_{J,IN}$	-	250	ps
Input Duty Cycle over 10K cycles	DC_{IN}	40%	60%	t_{CYCLE}
Input frequency of modulation	$F_{M,IN}$	30	33	kHz
Modulation index	$P_{M,IN}$	0.25	0.5	%
Phase detector input cycle time at PCLK (1:0) & SYNCLK (1:0)	$t_{CYCLE,PD}$	30	100	ns
Initial phase error at phase detector inputs	$t_{err,init}$	-0.5	0.5	$t_{CYCLE,PD}$
Phase detector input duty cycle over 10K cycles	$DC_{IN,PD}$	25%	75%	$t_{CYCLE,PD}$
Input rise & fall times (measured at 20%-80% of input voltage) for PCLK (1:0), SYNCLK (1:0) & REFCLK	t_{IR}, t_{IF}	-	1	ns
Input capacitance at PCLK (1:0) & SYNCLK (1:0) & REFCLK	$C_{IN,PD}$	-	7	pF
Input capacitance matching at PCLK (1:0) & SYNCLK (1:0)	$\Delta C_{IN,PD}$	-	0.5	pF
Input capacitance at CMOS pins	$C_{IN,CMOS}$	-	10	pF
Input (CMOS) signal low voltage	V_{IL}	-	0.3	V_{DD}
Input (CMOS) signal high voltage	V_{IH}	0.7	-	V_{DD}
REFCLK input low voltage	$V_{IL,R}$	-	0.3	$V_{DD,IR}$
REFCLK input high voltage	$V_{IH,R}$	0.7	-	$V_{DD,IR}$
Input signal low voltage for PD inputs and STOP_CLK	$V_{IL,R}$	-	0.3	$V_{DD,IPD}$
Input signal high voltage for PD inputs and STOP_CLK	$V_{IH,R}$	0.7	-	$V_{DD,IPD}$
Input supply reference for REFCLK	$V_{DD,IR}$	1.235	3.465	V
Input supply reference for PD inputs	$V_{DD,IPD}$	1.235	3.465	V
Phase detector phase error for distributed loop measured at PCLK (1:0) & SYNCLK (1:0)	$t_{ERR,PD}$	-100	100	ps
Clock Cycle time	t_{CYCLE}	2.5	3.75	ns
Cycle-to-cycle jitter at CLK (1:0) & CLKB (1:0)	t_J	-	60	ps
Total jitter over 2 ,3 or 4 cycles	t_J	-	100	ps
Phase aligner phase step size CLK (1:0) & CLKB (1:0)	t_{STEP}	1	-	ps
PLL output phase error when tracking SSC	$t_{ERR,SSC}$	-100	100	ps
Output crossing-point voltage	V_X	1.3	1.8	V
Output voltage during Clk Stop (CLK_STOP#=0)	$V_{X,STOP}$	1.1	2	V
Output Voltage swing	V_{COS}	0.4	1	V
Output low voltage	V_{OL}	1	-	V
Output high voltage	V_{OH}	-	2.35	V
Output duty cycle over 10K cycles	DC	40%	60%	t_{CYCLE}
Output cycle-to-cycle duty cycle error	$t_{DC,ERR}$	-	50	ps
Output rise & fall times (measured at 20%-80% of input voltage) for PCLK (1:0), SYNCLK (1:0) & REFCLK	t_{CR},t_{CF}	300	500	ps
Difference between rise and fall times on a single device (20%-80%)	$t_{CR,CF}$	-	100	ps
Operating Supply Current 400MHz			250	mA



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153
10-0035

4.40 mm. Body, 0.65 mm. pitch TSSOP
(173 mil) (0.0256 Inch)

Ordering Information

ICS9222yG-01LF-T

Example:

ICS XXXX y G - PPP LF - T

Designation for tape and reel packaging

Lead Free, RoHS Compliant (Optional)

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
G=TSSOP

Revision Designator (will not correlate with datasheet revision)

Device Type

Prefix
ICS = Standard Device

0274C—11/14/05

Revision History

Rev.	Issue Date	Description	Page #
C	11/14/2005	Added LF to Ordering Information	5