Integrated Circuit Systems, Inc.

ICS85357-11

4:1 OR 2:1, CRYSTAL OSCILLATOR-TO-3.3V LVPECL / ECL MULTIPLEXER

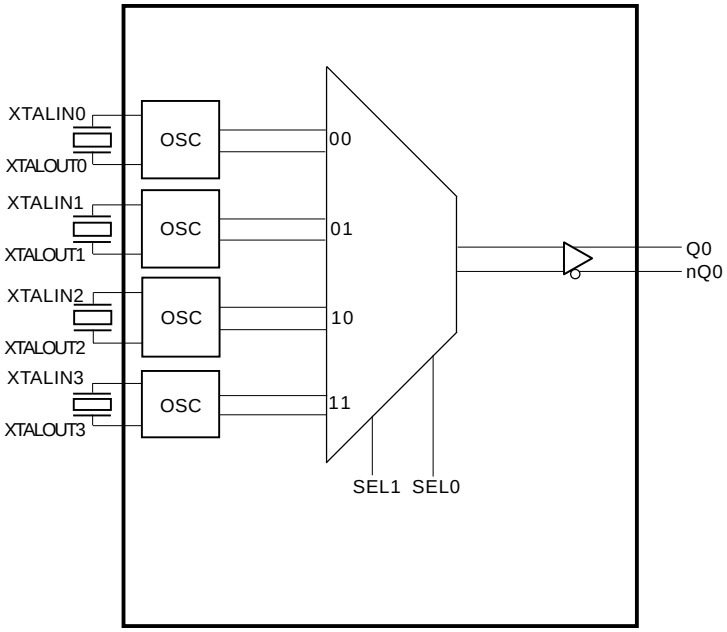
GENERAL DESCRIPTION

The ICS85357-11 is a 4:1 or 2:1, Crystal Oscillator-to-3.3V LVPECL / ECL Multiplexer and is a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS85357-11 has 4 selectable crystal inputs. The device can support 10MHz - 25MHz parallel resonant crystals by connecting external capacitors between XTALIN/XTALOUT and ground. The select pins have internal pulldown resistors and leaving one input unconnected (pulled to logic low by the internal resistor) will transform the device into a 2:1 multiplexer. The SEL1 lead is the most significant line and the binary number applied to the select pins will select the same numbered data input (i.e., 00 selects XTALIN0/XTALOUT0).

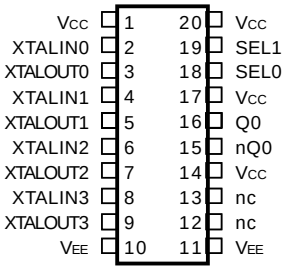
FEATURES

- 1 differential 3.3V LVPECL output
- 4:1 or 2:1 Crystal Oscillator Multiplexer
- Supports parallel resonant crystals with a frequency range of 10MHz - 25MHz. The oscillator circuit is optimized for parallel resonant mode, and will require external capacitance
- Maximum output frequency up to 25MHz
- LVCMOS SEL0 and SEL1 inputs have internal pulldown resistors
- Part-to-part skew: 150ps (maximum)
- Propagation delay: 2ns (maximum)
- LVPECL mode operating voltage supply range: V_{CC} = 3.135V to 3.465V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.135V to -3.465V
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS85357-11

20-Lead TSSOP
4.40mm x 6.50mm x 0.92mm body package
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 14, 17, 20	V_{CC}	Power		Positive supply pins. Connect to 3.3V.
2	XTALIN0	Input		Parallel resonant crystal input.
3	XTALOUT0	Input		Parallel resonant crystal input.
4	XTALIN1	Input		Parallel resonant crystal input.
5	XTALOUT1	Input		Parallel resonant crystal input.
6	XTALIN2	Input		Parallel resonant crystal input.
7	XTALOUT2	Input		Parallel resonant crystal input.
8	XTALIN3	Input		Parallel resonant crystal input.
9	XTALOUT3	Input		Parallel resonant crystal input.
10, 11	V_{EE}	Power		Negative supply pins. Connect to ground.
12, 13	nc	Unused		No connect.
15, 16	nQ0, Q0	Output		Differential clock outputs. LVPECL interface levels.
18	SEL0	Input	Pulldown	Clock select input. LVCMOS / LVTTL interface levels.
19	SEL1	Input	Pulldown	Clock select input. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	SEL0, SEL1				4	pF
R_{PULLUP}	Input Pullup Resistor				51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		KΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs		Clock Out
SEL1	SEL0	CLK
0	0	XTALIN0, XTALOUT0
0	1	XTALIN1, XTALOUT1
1	0	XTALIN2, XTALOUT2
1	1	XTALIN3, XTALOUT3

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, V_O	-0.5V to V_{CC} + 0.5V
Package Thermal Impedance, θ_{JA}	73.2°C/W (0lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				50	mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	SEL0, SEL1		2		3.765	V
V_{IL}	Input Low Voltage	SEL0, SEL1		-0.3		0.8	V
I_{IH}	Input High Current	SEL0, SEL1	V_{CC} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	SEL0, SEL1	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA

TABLE 4C. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 1.0	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		0.85	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation / cut		Fundamental / Parallel Resonant			
Frequency		10		25	MHz
Equivalent Series Resistance (ESR)		50		80	Ω
Shunt Capacitance				7	pF
Series Pin Inductance		3		7	nH
Operating Temperature Range		0		70	°C

TABLE 6. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, T_A=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency Range		10		25	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 25MHz	1		2	ns
tsk(pp)	Part-to-Part Skew; NOTE 2, 4				150	ps
t_R	Output Rise Time	20% to 80%	300		700	ps
t_F	Output Fall Time	20% to 80%	300		700	ps
odc	Output Duty Cycle; NOTE 3, 4		47		53	%
oscTOL	Crystal Oscillator Tolerance; NOTE 3			±20		ppm

All parameters measured at 25MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point. Measured overdriving the XTAL input.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points. Measured overdriving the XTAL input.
NOTE 3: Measured using C1 = 22pF and C2 = 27pF in parallel with 18pF crystals. Refer to Figure 6 in the Application Section.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

PARAMETER MEASUREMENT INFORMATION

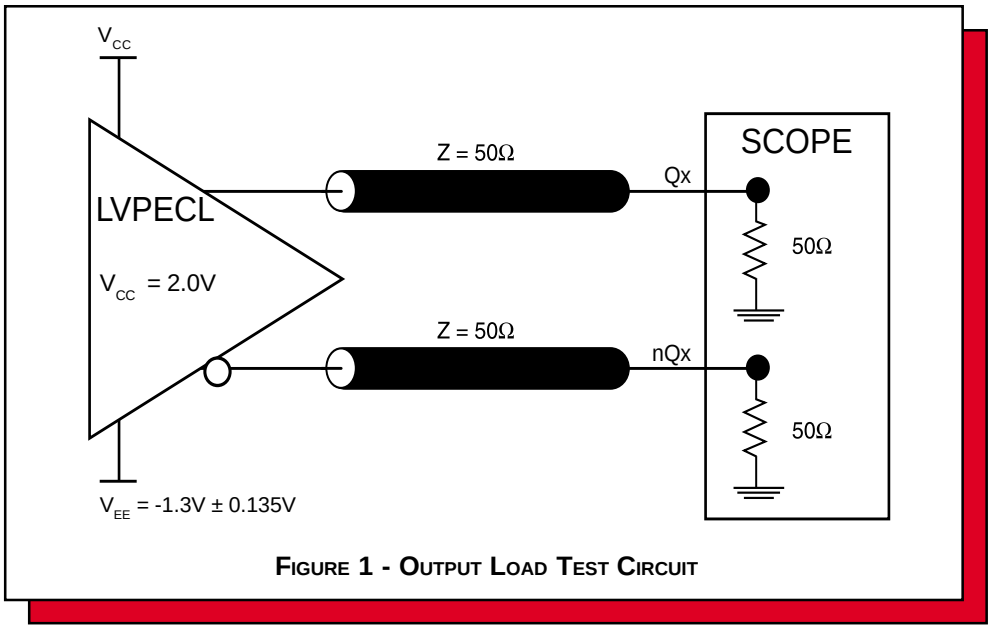


FIGURE 1 - OUTPUT LOAD TEST CIRCUIT

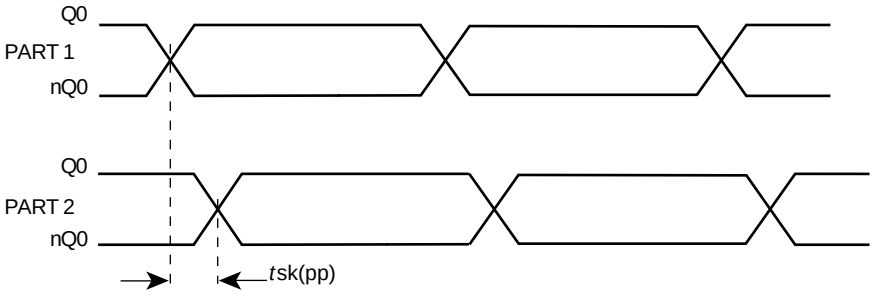


FIGURE 2 - PART-TO-PART SKEW

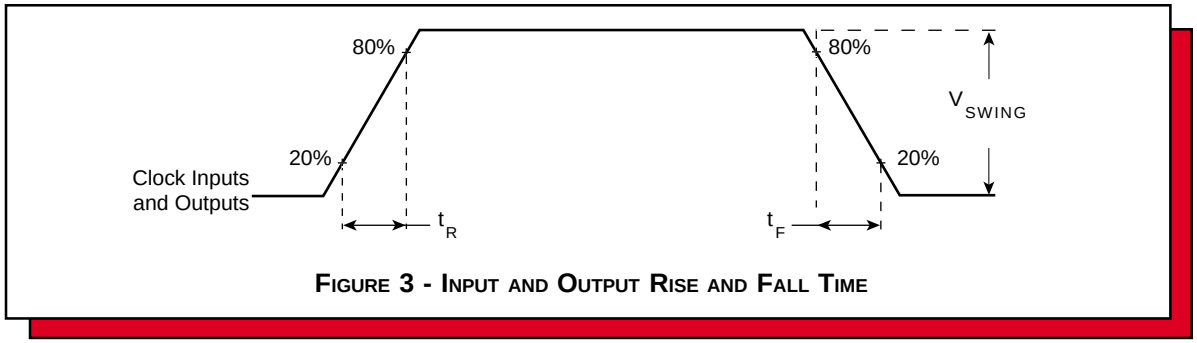


FIGURE 3 - INPUT AND OUTPUT RISE AND FALL TIME

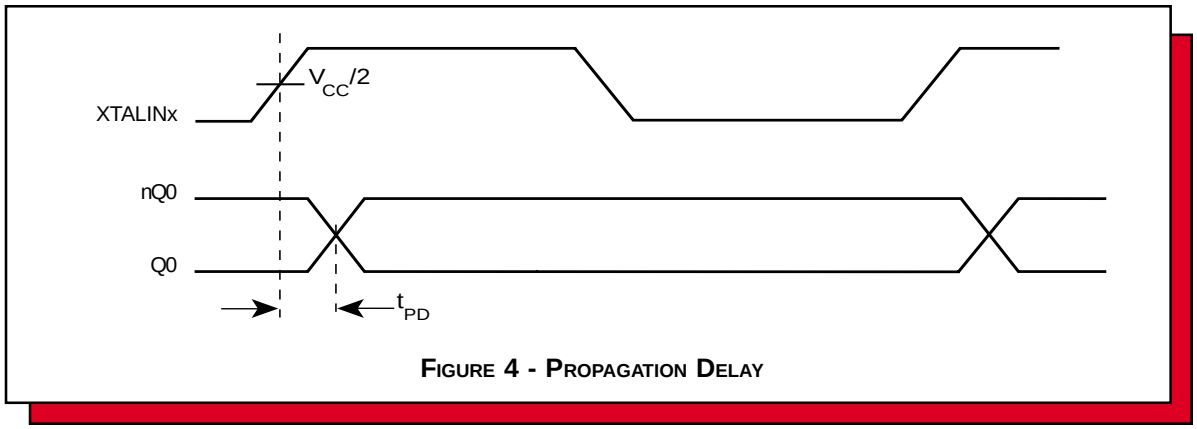


FIGURE 4 - PROPAGATION DELAY

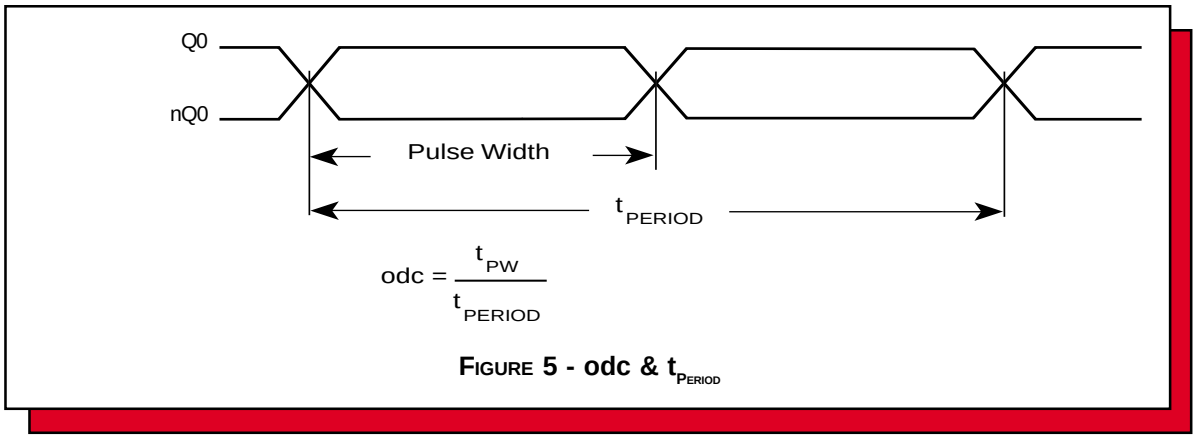


FIGURE 5 - odc & t_{PERIOD}

APPLICATION INFORMATION

CRYSTAL INPUT INTERFACE

A crystal can be characterized for either series or parallel mode operation. The ICS85357-11 has a built-in crystal oscillator circuit. This interface can accept either a series or parallel crystal without additional components and generate frequencies with accuracy suitable for most applications. Additional accuracy can be achieved by adding two small capacitors C1 and C2 as shown in *Figure 6*. Typical results using parallel 18pF crystals are shown in Table 7.

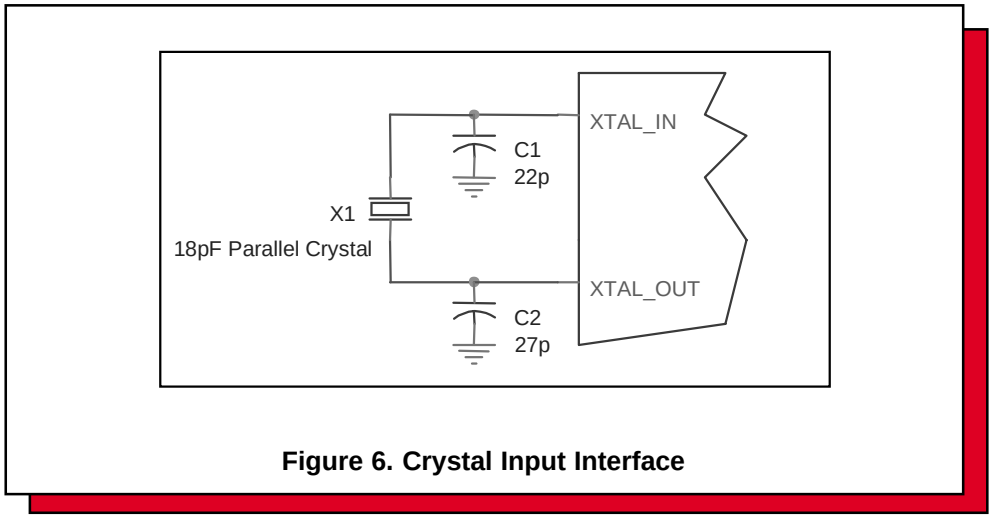


Figure 6. Crystal Input Interface

Table 7. Typical Results of Crystal Input Interface Frequency Fine Tuning

Crystal Frequency (MHz)	C1 (pF)	C2 (pF)	Measured Output Frequency (MHz)	Accuracy (PPM)	Duty Cycle (%)
14.31818	22	27	14.318011	-12	47.46
15.00	22	27	14.999862	-9	47.70
16.66	22	27	16.660162	10	47.70
19.44	22	27	19.440081	4	46.85
24.00	22	27	24.000183	8	46.00

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85357-11.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS85357-11 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 50mA = **173.3mW**
- Power (outputs)$_{MAX}$ = **30.2mW/Loaded Output pair**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 173.3mW + 30.2mW = **203.5mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = junction-to-ambient thermal resistance

Pd_total = Total device power dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.204W * 66.6°C/W = 83.6°C. This is well below the limit of 125°C

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 8. Thermal Resistance θ_{JA} for 20-pin TSSOP, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

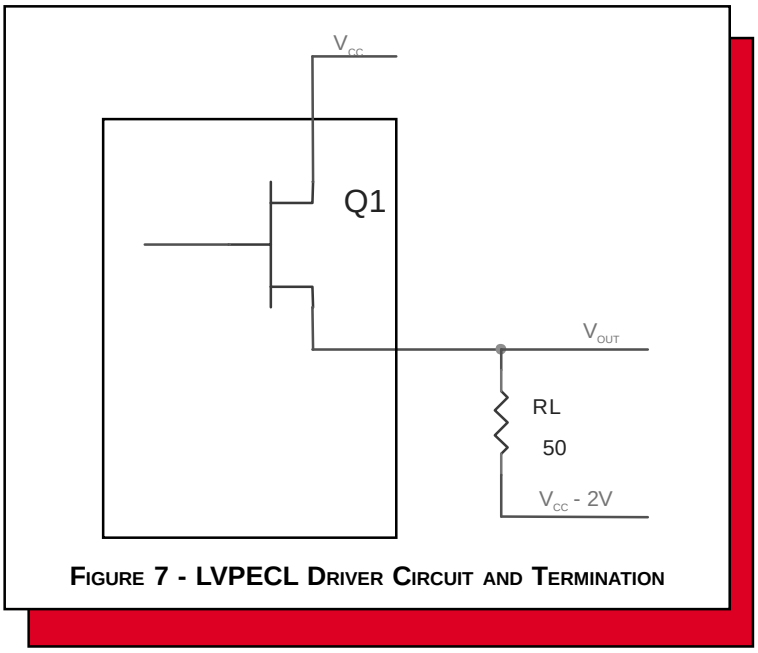


FIGURE 7 - LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX})$

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX})$

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 1.0V}$

  Using V_{CC_MAX} = 3.465, this results in V_{OH_MAX} = **2.465V**

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$

  Using V_{CC_MAX} = 3.465, this results in V_{OL_MAX} = **1.765V**

Pd_H = [(2.465V - (3.465V - 2V))/50Ω] * (3.465V - 2.465V) = **20mW**
Pd_L = [(1.765V - (3.465V - 2V))/50Ω] * (3.465V - 1.765V) = **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

RELIABILITY INFORMATION

TABLE 9. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS85357-11 is: 413

PACKAGE OUTLINE - G SUFFIX

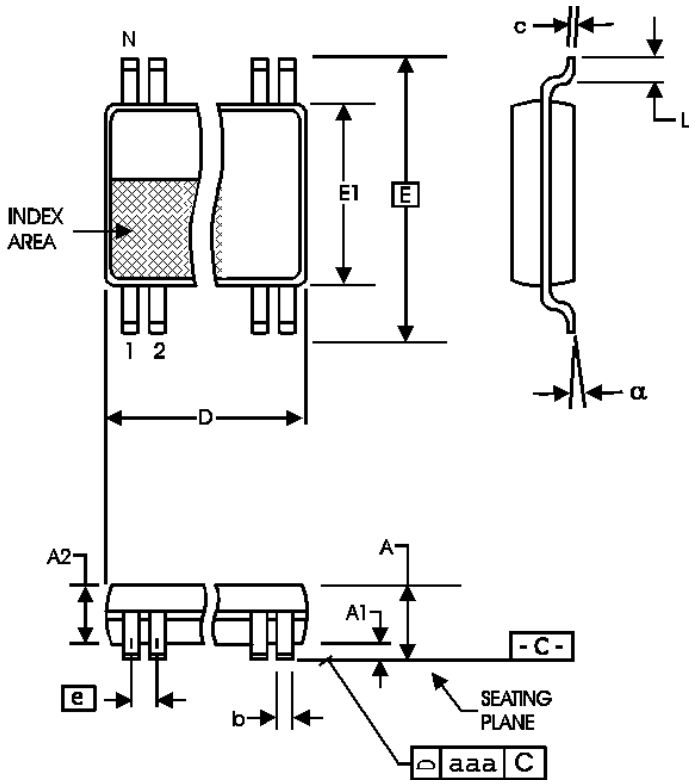


TABLE 10. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 11. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS85357AG-11	ICS85357AG11	20 lead TSSOP	72 per tube	0°C to 70°C
ICS85357AG-11T	ICS85357AG11	20 lead TSSOP on Tape and Reel	2500	0°C to 70°C