
HM62V256 Series

32,768-word × 8-bit Low Voltage Operation CMOS Static RAM

HITACHI

ADE-203-136E (Z)

Rev. 5.0

Jun. 19, 1995

Features

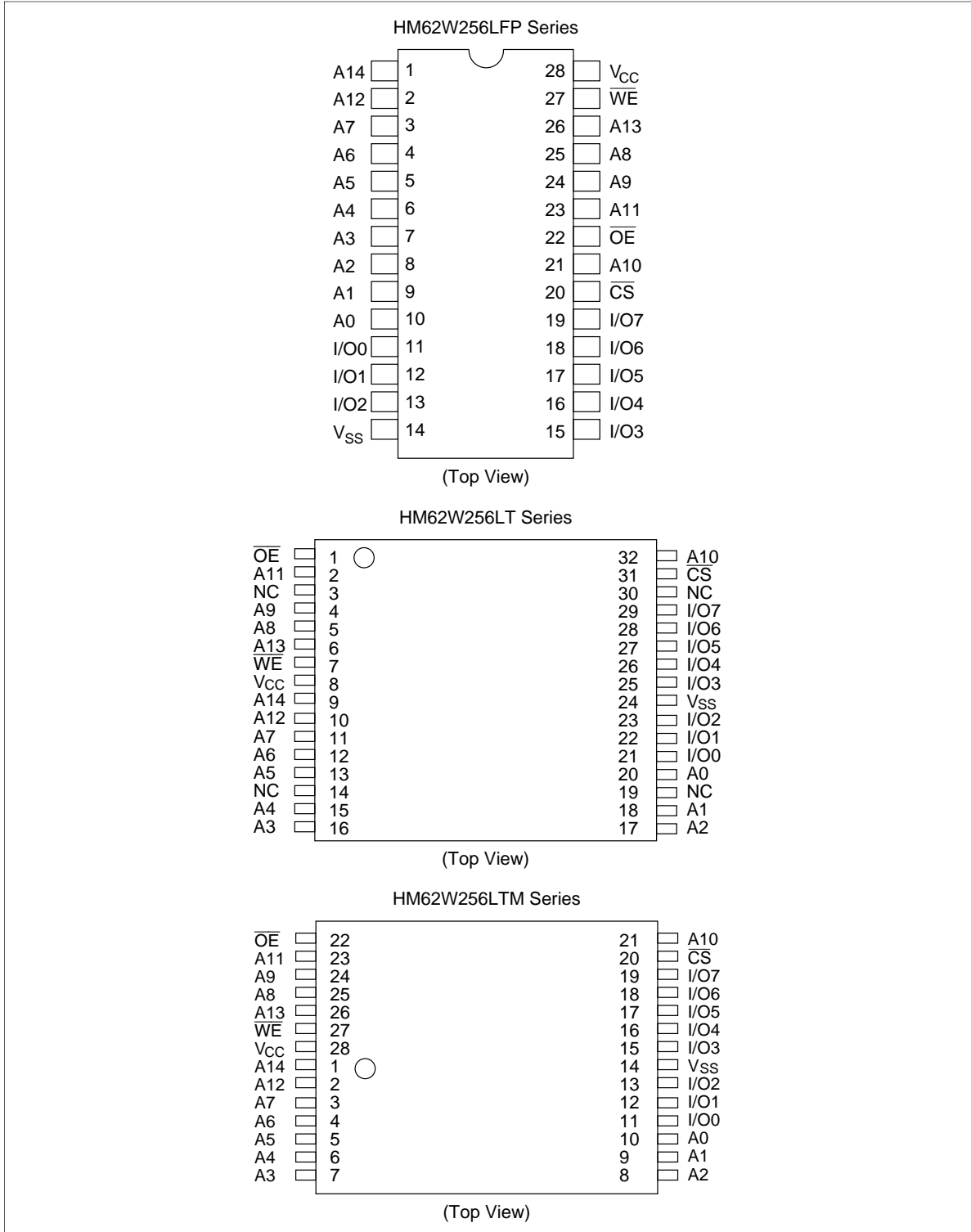
- Low voltage operation SRAM
Operating Supply Voltage: 2.7 V to 3.6 V
- 0.8 μm Hi-CMOS process
- High speed
Access time: 70/85/100 ns (max)
- Low power
Standby: 0.15 μW (typ)
- Completely static memory
No clock or timing strobe required
- Directly LVTTTL compatible: All inputs and outputs

Ordering Information

Type No.	Access Time	Package
HM62V256LFP-10T	100 ns	450 mil 280 pin plastic SOP (FP-28DA)
HM62V256LFP-7SLT	70 ns	
HM62V256LFP-10SLT	100 ns	
HM62V256LFP-8ULT	85 ns	
HM62V256LT-10	100 ns	8 mm × 14 mm 32 pin TSOP (normal type) (TFP-32DA)
HM62V256LT-8SL	85 ns	
HM62V256LTM-10	100 ns	8 mm × 13.4 mm 28-pin TSOP (normal type) (TFP-28DA)
HM62V256LTM-7SL	70 ns	
HM62V256LTM-10SL	100 ns	
HM62V256LTM-8UL	85 ns	

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Pin Arrangement

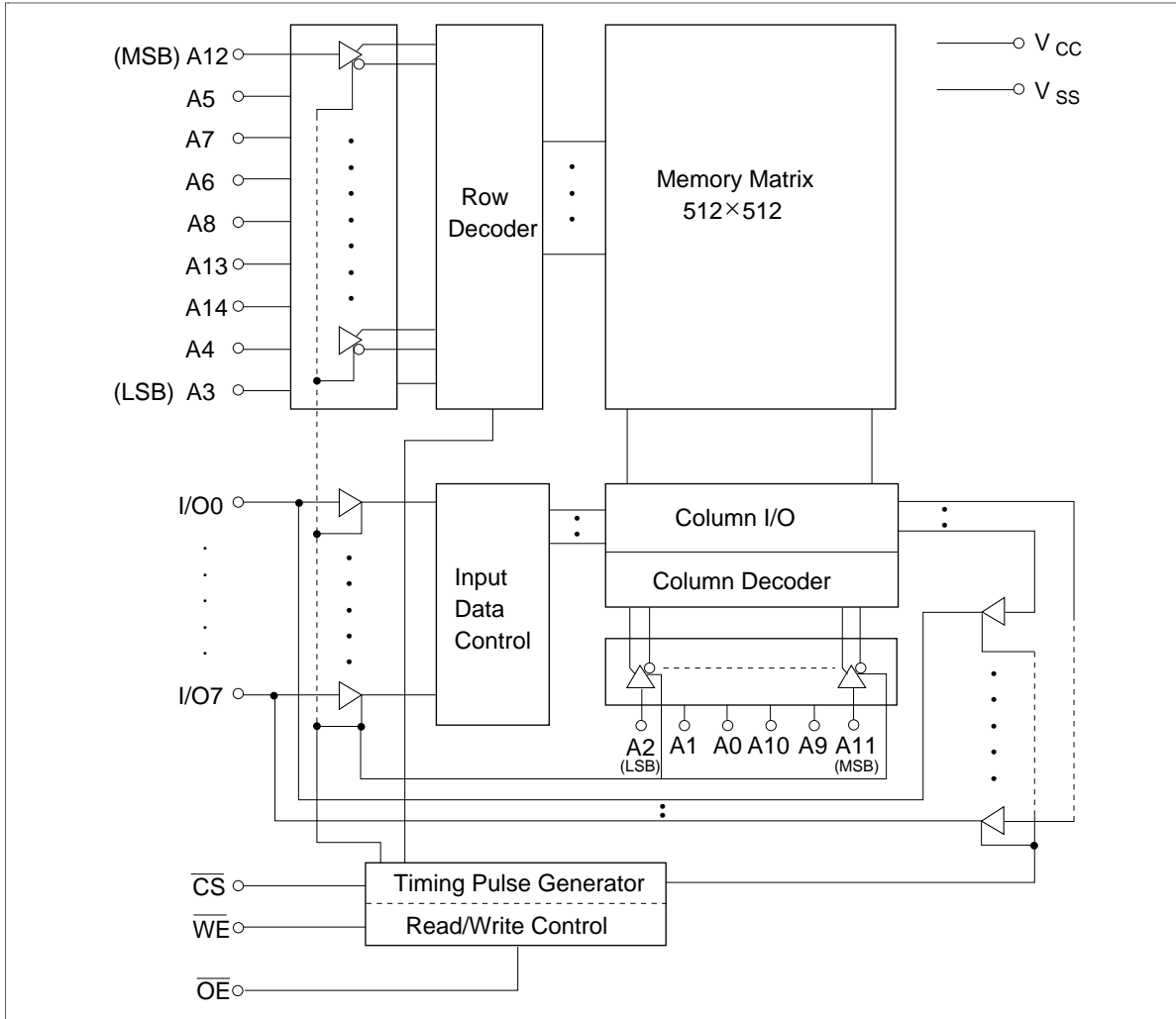


Pin Description

Pin name	Function
A0 to A14	Address inputs
I/O0 to I/O7	Data input/output
$\overline{\text{CS}}$	Chip select
$\overline{\text{WE}}$	Write enable
$\overline{\text{OE}}$	Output enable
NC	No connection
V _{CC}	Power supply
V _{SS}	Ground

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Block Diagram



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Function Table

\overline{WE}	\overline{CS}	\overline{OE}	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
X	H	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle (1)–(3)
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: X: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage ¹	V_{CC}	–0.5 to 4.6	V
Terminal voltage ¹	V_T	–0.5 ² to $V_{CC}+0.5$ ³	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	–55 to +125	°C
Storage temperature under bias	T_{bias}	–10 to +85	°C

- Notes: 1. Relative to V_{SS}
 2. V_T min: –3.0 V for pulse half-width ≤ 50 ns
 3. Maximum voltage is 4.6V

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
	V_{SS}	0	0	0	V
Input high(logic 1) voltage	V_{IH}	$0.7V_{CC}$	—	$V_{CC}+0.3$	V
Input low(logic 0) voltage	V_{IL}	–0.3 ¹	—	$0.2V_{CC}$	V

Note: 1. V_T min: –3.0 V for pulse half-width ≤ 50 ns

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 2.7 V to 3.6V, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ ¹	Max	Unit	Test conditions	
Input leakage current	I _{LI}	—	—	1	μA	V _{SS} ≤ Vin ≤ V _{CC}	
Output leakage current	I _{LO}	—	—	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, V _{SS} ≤ V _{IO} ≤ V _{CC}	
Operating power supply current (DC)	I _{CCDC1}	—	—	15	mA	$\overline{CS} = V_{IL}$, others = V _{IH} /V _{IL} I _{IO} = 0 mA	
	I _{CCDC2}	—	—	10	mA	$\overline{CS} \leq 0.2$ V, V _{IH} ≥ V _{CC} - 0.2 V, V _{IL} ≤ 0.2 V, I _{IO} = 0 mA	
Average operating power supply current	HM62V256-7	I _{CCAC1}	—	—	30	mA	min cycle, duty = 100 %, I _{IO} = 0 mA $\overline{CS} = V_{IL}$, others = V _{IH} /V _{IL}
	HM62V256-8	I _{CCAC1}	—	—	27		
	HM62V256-10	I _{CCAC1}	—	—	24		
		I _{CCAC2}	—	—	15	mA	Cycle time ≥ 1 μs, duty = 100% I _{IO} = 0 mA, $\overline{CS} \leq 0.2$ V, V _{IH} ≥ V _{CC} - 0.2 V, V _{IL} ≤ 0.2 V
Standby power supply current	I _{SB}	I _{SB}	—	0.1	1	mA	$\overline{CS} = V_{IH}$
		I _{SB1}	—	0.05	50	μA	Vin ≥ 0 V, $\overline{CS} \geq V_{CC} - 0.2$ V,
		—	—	0.05	10 ⁻²		
		—	—	0.05	4 ⁻³		
Output low voltage	V _{OL}	—	—	0.2	V	I _{OL} = 20 μA	
Output high voltage	V _{OH}	V _{CC} - 0.2	—	—	V	I _{OH} = -20 μA	

- Notes: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and not guaranteed.
 2. This characteristic is guaranteed only for L-SL version.
 3. This characteristic is guaranteed only for L-UL version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

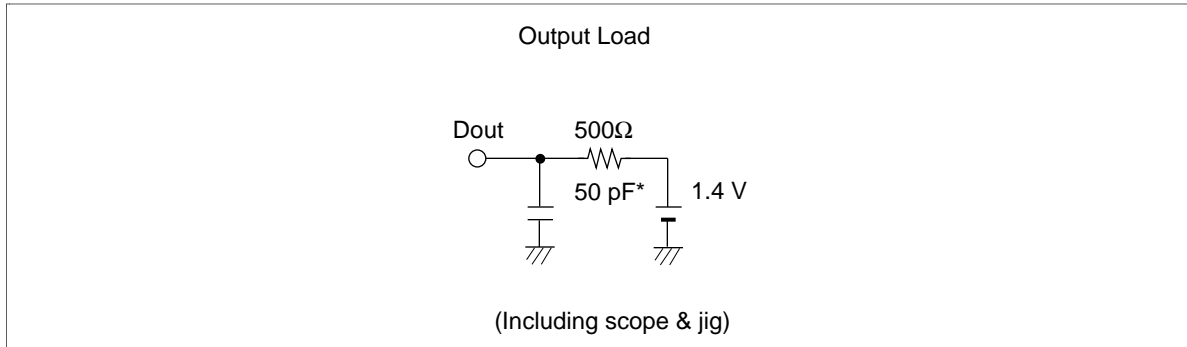
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance ^{*1}	C _{in}	—	—	5	pF	Vin = 0 V
Input/output capacitance ^{*1}	C _{IO}	—	—	8	pF	V _{IO} = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 2.7$ V to 3.6 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference level: 1.4 V



Read Cycle

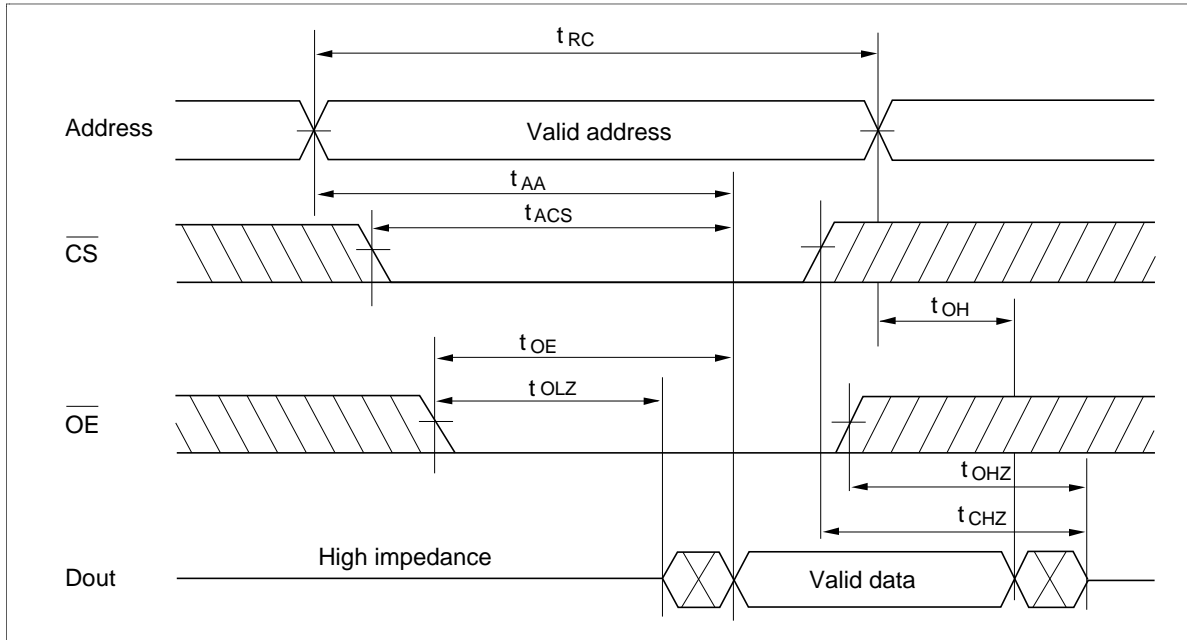
Parameter	Symbol	HM62V256						Unit	Notes
		-7		-8		-10			
		Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	70	—	85	—	100	—	ns	
Address access time	t_{AA}	—	70	—	85	—	100	ns	
Chip select access time	t_{ACS}	—	70	—	85	—	100	ns	
Output enable to output valid	t_{OE}	—	35	—	45	—	50	ns	
Chip selection to output in low-Z	t_{CLZ}	10	—	10	—	10	—	ns	2
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	5	—	ns	2
Chip deselection to output in high-Z	t_{CHZ}	0	25	0	30	0	35	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	25	0	30	0	35	ns	1, 2
Output hold from address change	t_{OH}	10	—	10	—	10	—	ns	

Notes: 1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

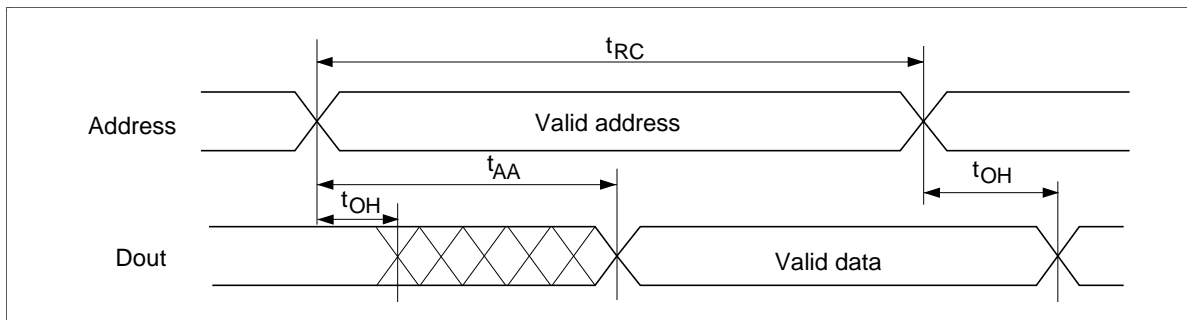
2. This parameter is sampled and not 100% tested.

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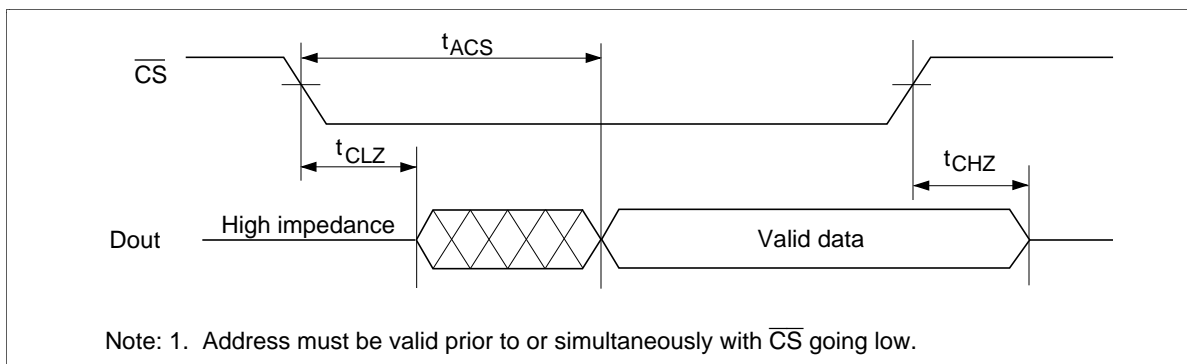
Read Timing Waveform (1) ($\overline{WE} = V_{IH}$)



Read Timing Waveform (2) ($\overline{WE} = V_{IH}, \overline{CS} = V_{IL}, \overline{OE} = V_{IL}$)



Read Timing Waveform (3) ($\overline{WE} = V_{IH}, \overline{OE} = V_{IL}$)*1



Note: 1. Address must be valid prior to or simultaneously with \overline{CS} going low.

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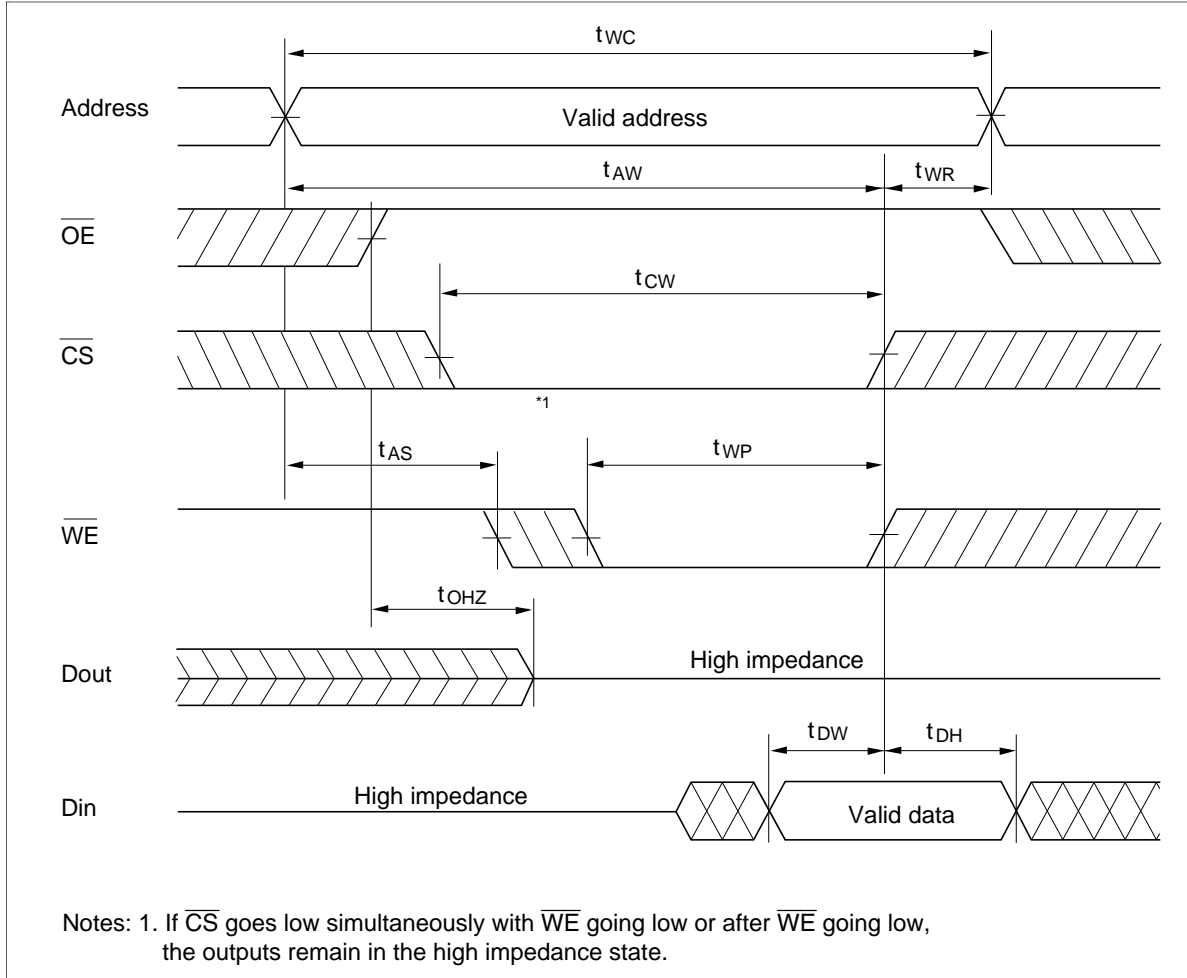
Write Cycle

Parameter	Symbol	HM62V256						Unit	Notes
		-7		-8		-10			
		Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	70	—	85	—	100	—	ns	
Chip selection to end of write	t_{CW}	50	—	75	—	80	—	ns	4
Address setup time	t_{AS}	0	—	0	—	0	—	ns	5
Address valid to end of write	t_{AW}	50	—	75	—	80	—	ns	
Write pulse width	t_{WP}	45	—	55	—	60	—	ns	3, 8
Write recovery time	t_{WR}	0	—	0	—	0	—	ns	6
Write to output in high-Z	t_{WHZ}	0	25	0	30	0	35	ns	1, 2, 7
Data to write time overlap	t_{DW}	30	—	35	—	40	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	10	—	10	—	10	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	25	0	30	0	35	ns	1, 2, 7

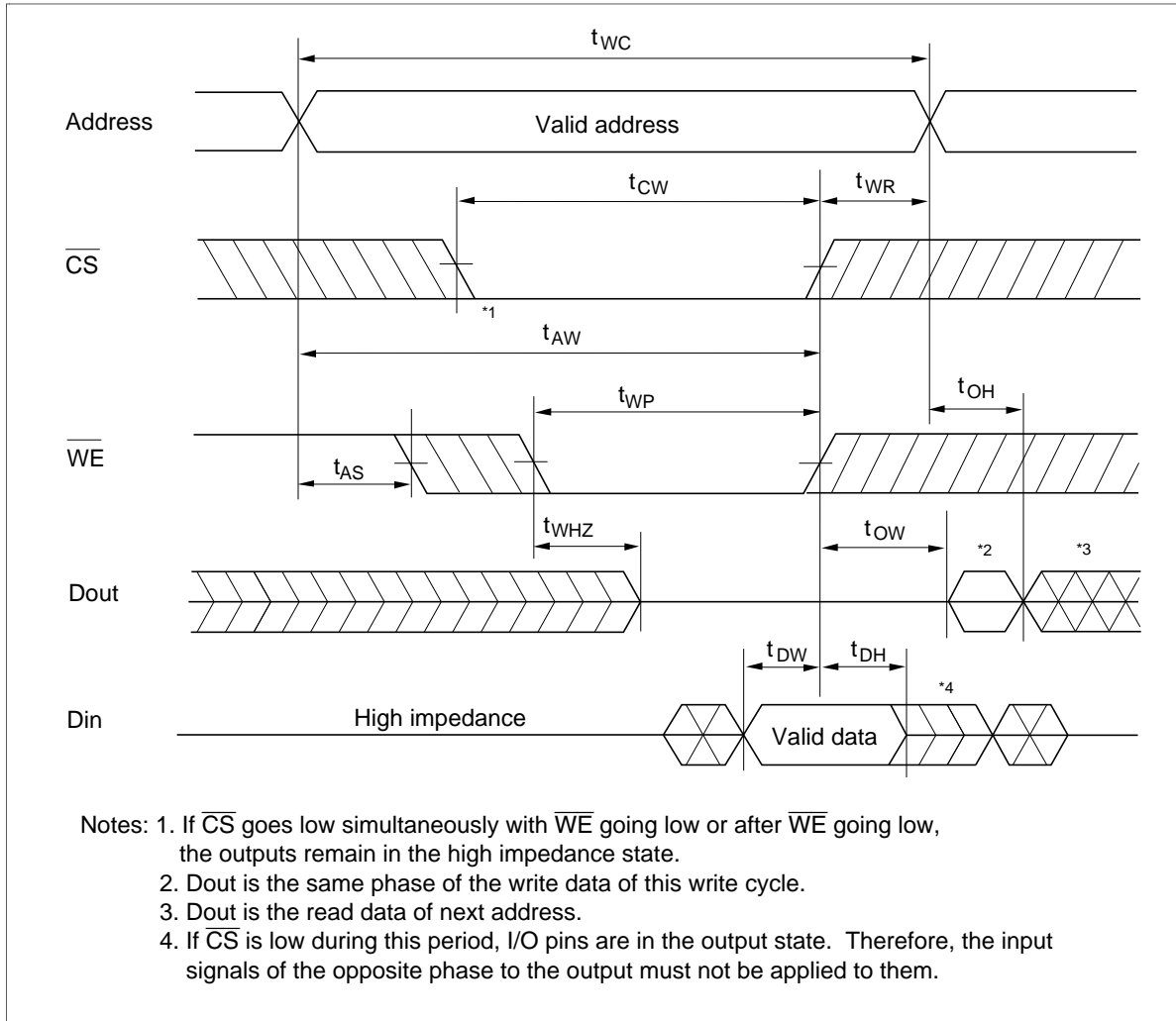
- Notes:
- t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 - This parameter is sampled and not 100% tested.
 - A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} . A write begins at the later transition of \overline{CS} going low or \overline{WE} going low. A write ends at the earlier transition of \overline{CS} going high or \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
 - t_{CW} is measured from \overline{CS} going low to the end of write.
 - t_{AS} is measured from the address valid to the beginning of write.
 - t_{WR} is measured from the earlier of \overline{WE} or \overline{CS} going high to the end of write cycle.
 - During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
 - In the write cycle with \overline{OE} low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention, $t_{WP} \geq t_{WHZ} \max + t_{DW} \min$.

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Write Timing Waveform (1) ($\overline{\text{OE}}$ Clock)



Write Timing Waveform (2) (\overline{OE} Low Fixed)



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Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions ⁶
V_{CC} for data retention	V_{DR}	2.0	—	3.6	V	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$, $V_{in} \geq 0\text{ V}$
Data retention current	I_{CCDR}	—	0.05	27^{*2}	μA	$V_{CC} = 2.7\text{ V}$, $V_{in} \geq 0\text{ V}$ $\overline{CS} \geq V_{CC} - 0.2\text{ V}$
		—	0.05	7^{*3}		
		—	0.05	2^{*4}		
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}^{*5}	—	—	ns	

Notes: 1. Typical values are at $V_{CC} = 2.7\text{ V}$, $T_a = 25^\circ\text{C}$ and not guaranteed.

2. $9\text{ }\mu\text{A}$ max at $T_a = 0$ to 40°C .

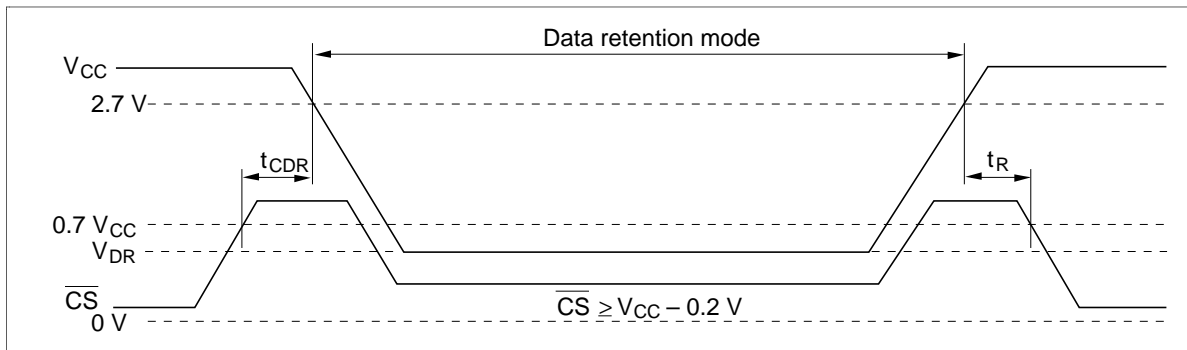
3. This characteristics guaranteed for only L-SL version. $2.0\text{ }\mu\text{A}$ max at $T_a = 0$ to 40°C .

4. This characteristics guaranteed for only L-UL version. $0.4\text{ }\mu\text{A}$ max at $T_a = 0$ to 40°C .

5. t_{RC} = read cycle time.

6. \overline{CS} controls address buffer, \overline{WE} buffer, \overline{OE} buffer, and D_{in} buffer. If \overline{CS} controls data retention mode, other input levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.

Low V_{CC} Data Retention Timing Waveform

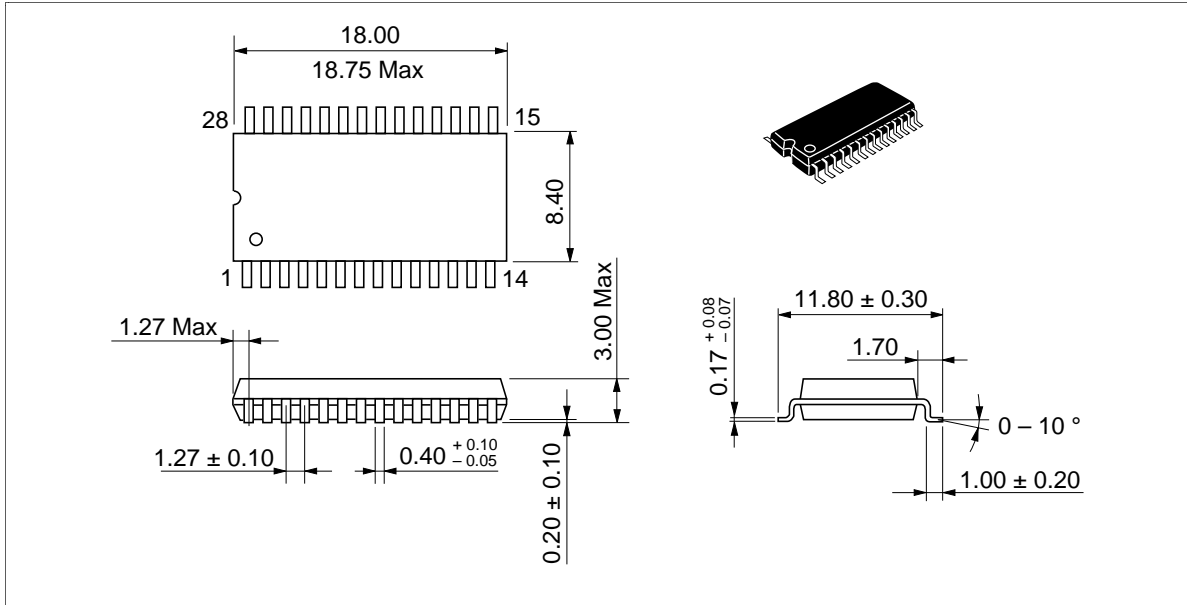


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Package Dimensions

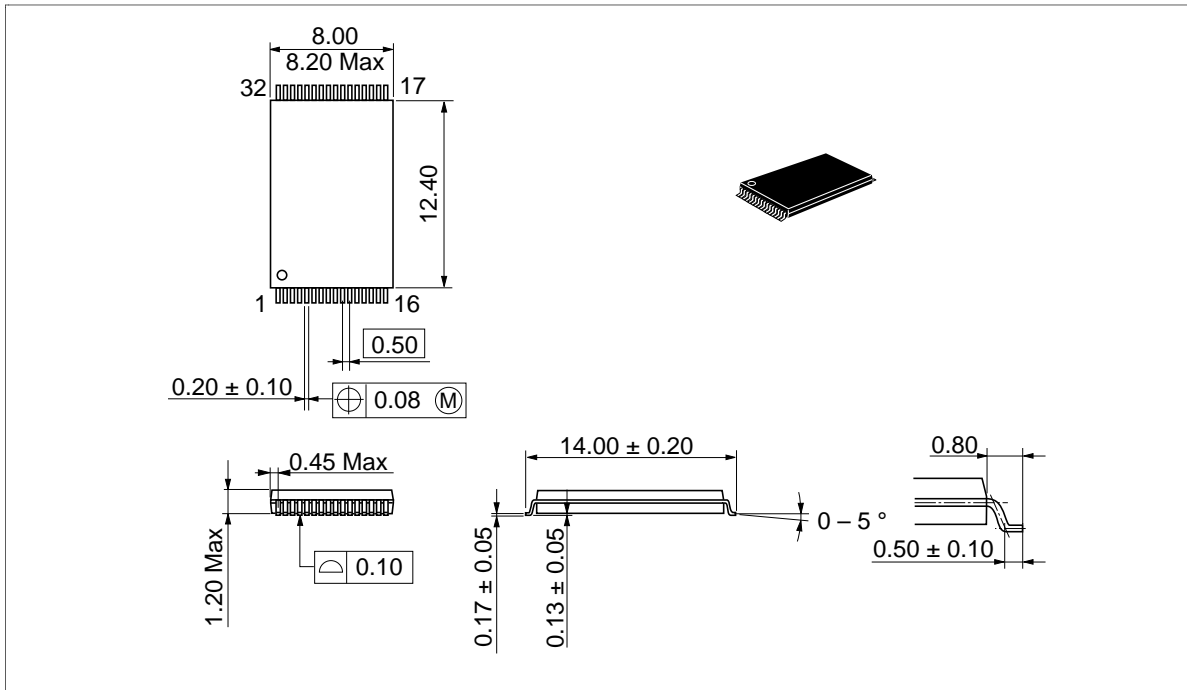
HM62V256LFP Series (FP-28DA)

Unit: mm



HM62V256LT Series (TFP-32DA)

Unit: mm



HM62V256 Series

HM62V256LTM Series (TFP-28DA)

Unit: mm

