

# H5N3004P

Silicon N Channel MOS FET  
High Speed Power Switching

**RENESAS**

ADE-208-1523 (Z)

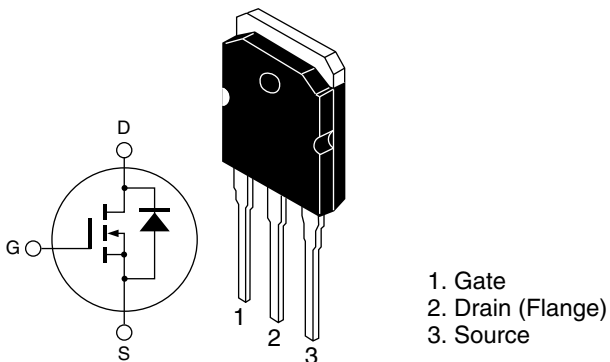
Rev.0  
Apr. 2002

## Features

- Low on-resistance
- Low leakage current
- High speed switching
- Low gate charge ( $Q_g$ )
- Avalanche ratings

## Outline

TO-3P



## Absolute Maximum Ratings

(Ta=25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	300	V
Gate to source voltage	$V_{GSS}$	±30	V
Drain current	$I_D$	25	A
Drain peak current	$I_D$ (pulse) <sup>Note1</sup>	100	A
Body-drain diode reverse drain current	$I_{DR}$	25	A
Body-drain diode reverse drain peak current	$I_{DR}$ (pulse) <sup>Note1</sup>	100	A
Avalanche current	$I_{AP}$ <sup>Note3</sup>	25	A
Channel dissipation	$P_{ch}$ <sup>Note2</sup>	150	W
Channel to case Thermal impedance	$\theta_{ch-c}$	0.833	°C/W
Channel temperature	$T_{ch}$	150	°C
Storage temperature	$T_{stg}$	-55 to +150	°C

Notes: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$

2. Value at  $T_c = 25^\circ C$

3.  $T_{ch} \leq 150^\circ C$

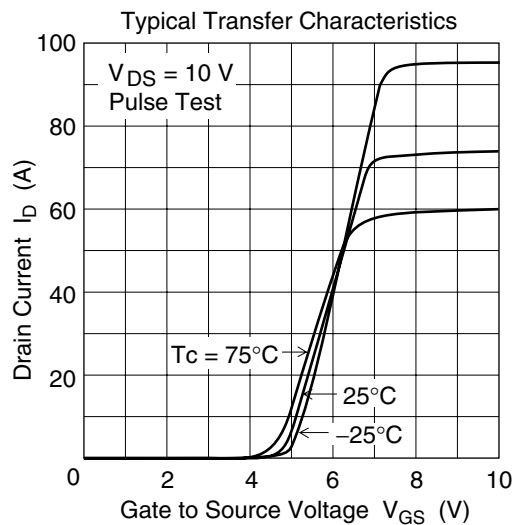
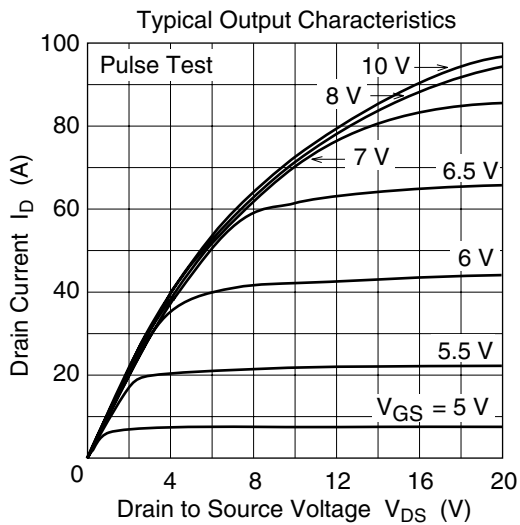
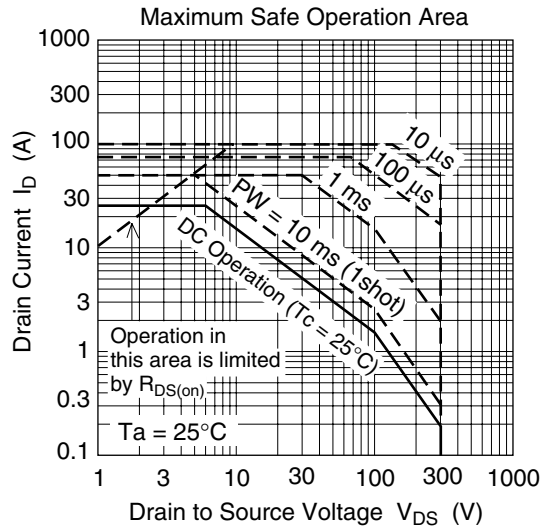
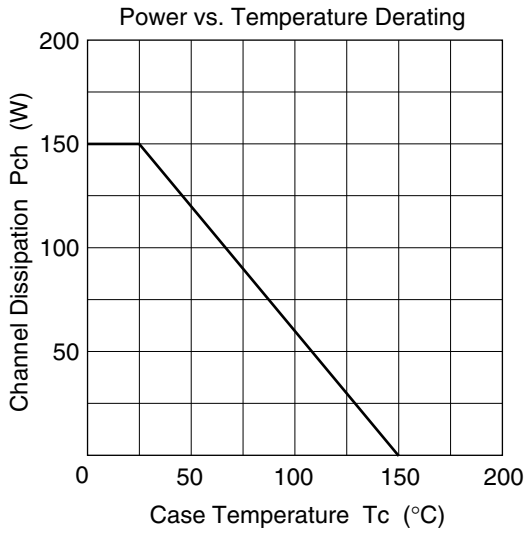
## Electrical Characteristics

(Ta=25°C)

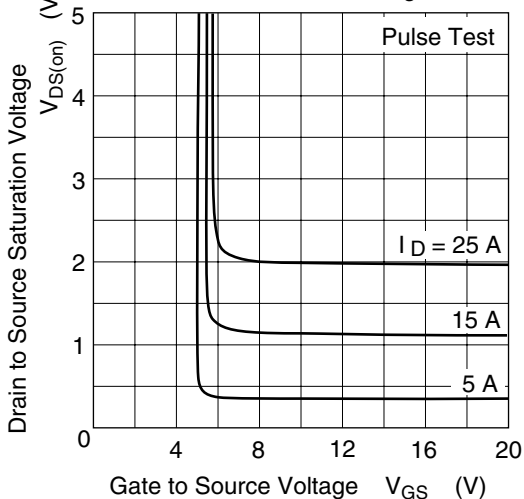
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	300	•	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	•	1	$\mu\text{A}$	$V_{DS} = 300 \text{ V}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	•	$\pm 0.1$	$\mu\text{A}$	$V_{GS} = \pm 30 \text{ V}$ , $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	•	4.0	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Forward transfer admittance	$ y_{fs} $	15	25	—	S	$I_D = 12.5 \text{ A}$ , $V_{DS} = 10 \text{ V}^{\text{Note4}}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.076	0.093	$\Omega$	$I_D = 12.5 \text{ A}$ , $V_{GS} = 10 \text{ V}^{\text{Note4}}$
Input capacitance	$C_{iss}$	—	3600	•	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	$C_{oss}$	—	400	•	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	100	•	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	50	•	ns	$I_D = 12.5 \text{ A}$
Rise time	$t_r$	—	120	—	ns	$R_L = 12 \Omega$
Turn-off delay time	$t_{d(off)}$	—	180	•	ns	$V_{GS} = 10 \text{ V}$
Fall time	$t_f$	—	90	—	ns	$R_g = 10 \Omega$
Total gate charge	$Q_g$	—	110	—	nC	$V_{DD} = 240 \text{ V}$
Gate to source charge	$Q_{gs}$	—	18	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	55	—	nC	$I_D = 25 \text{ A}$
Body-drain diode forward voltage	$V_{DF}$	—	0.9	1.35	V	$I_F = 25 \text{ A}$ , $V_{GS} = 0$
Body-drain diode reverse recovery time	$t_{rr}$	—	250	—	ns	$I_F = 25 \text{ A}$ , $V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$
Body-drain diode reverse recovery charge	$Q_{rr}$	—	2.3	—	$\mu\text{C}$	

Notes: 4. Pulse test

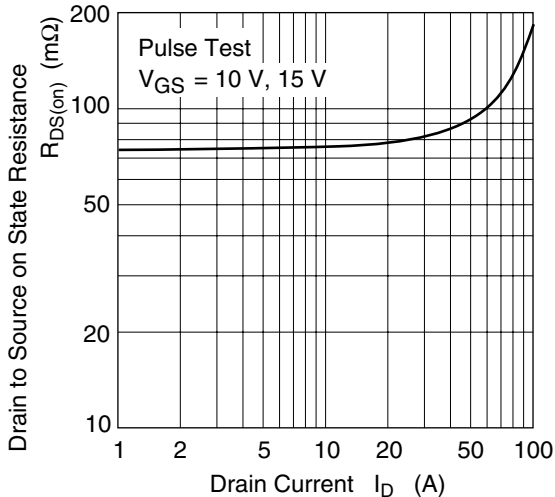
## Main Characteristics



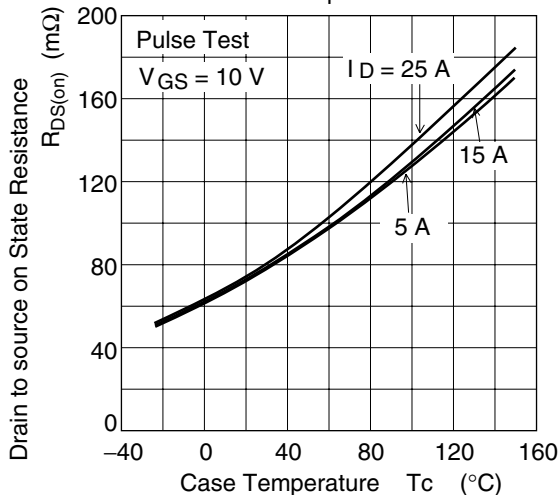
Drain to Source Saturation Voltage vs. Gate to Source Voltage



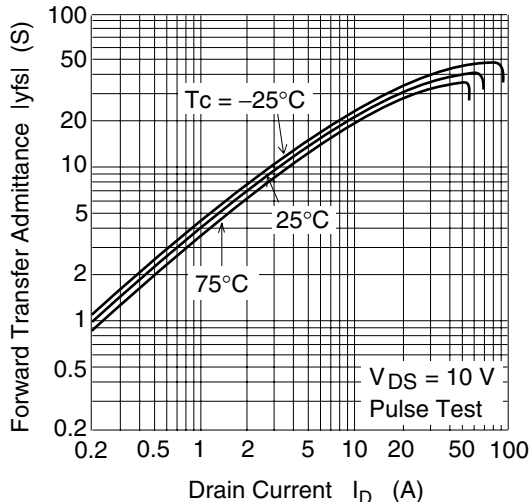
Static Drain to Source on State Resistance vs. Drain Current



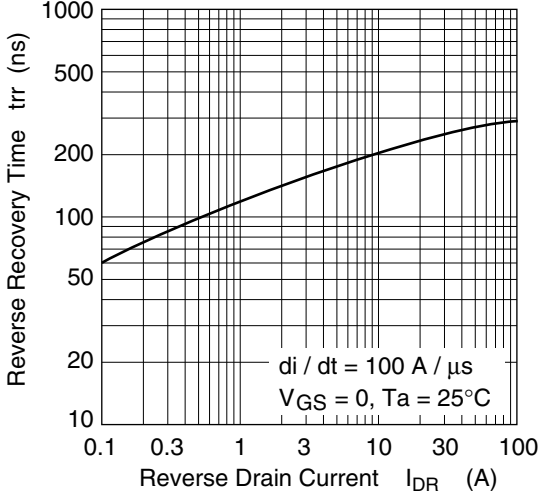
Static Drain to Source on State Resistance vs. Temperature



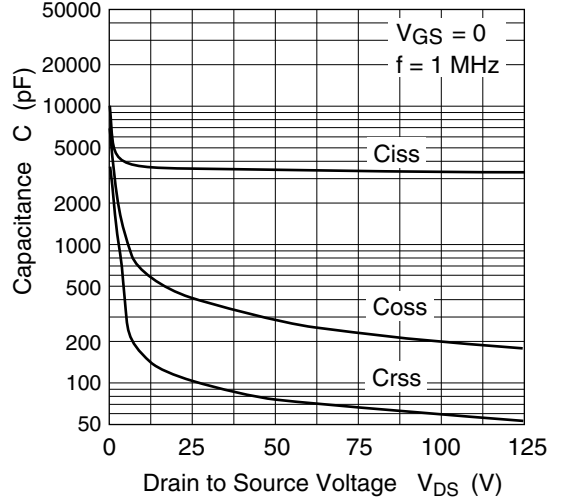
Forward Transfer Admittance vs. Drain Current



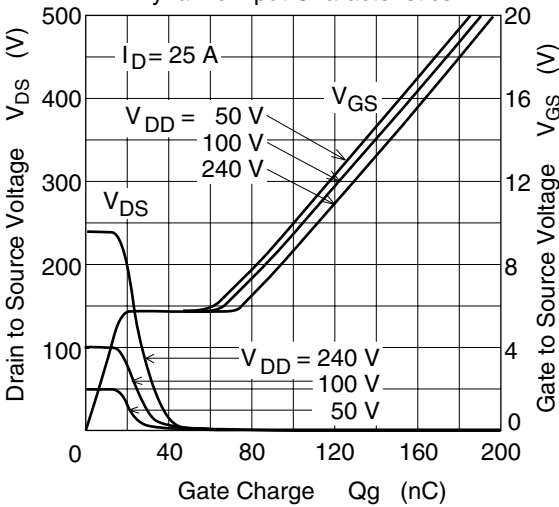
Body-Drain Diode Reverse Recovery Time



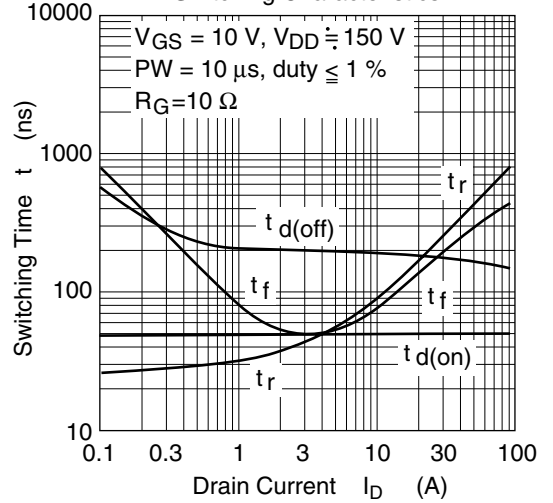
Typical Capacitance vs. Drain to Source Voltage

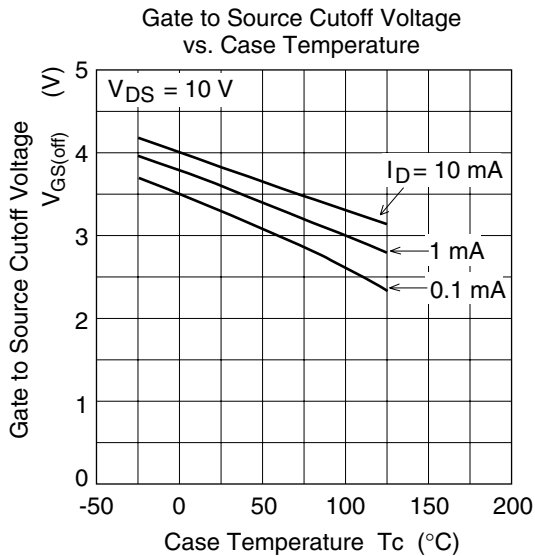
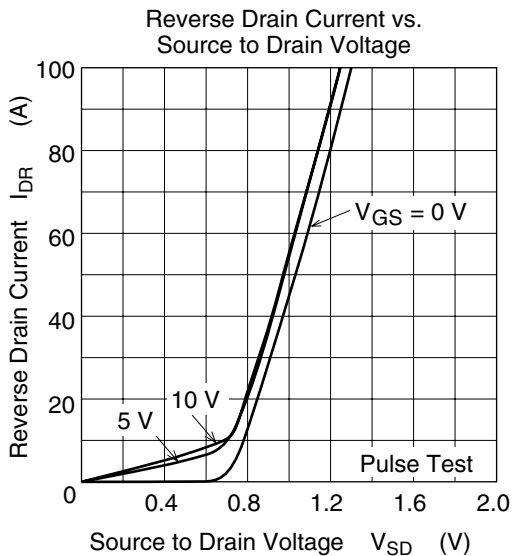


Dynamic Input Characteristics

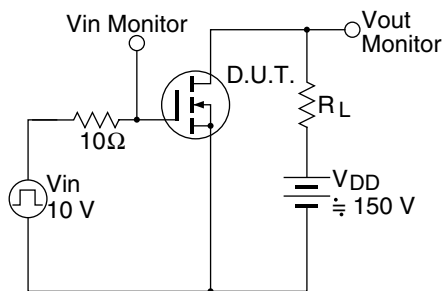


Switching Characteristics

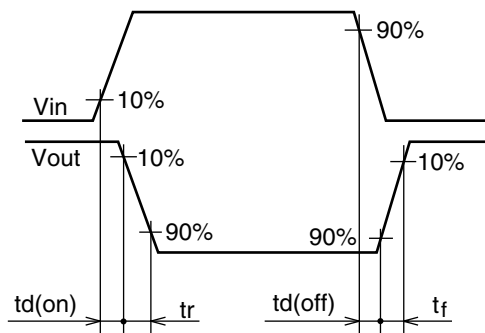


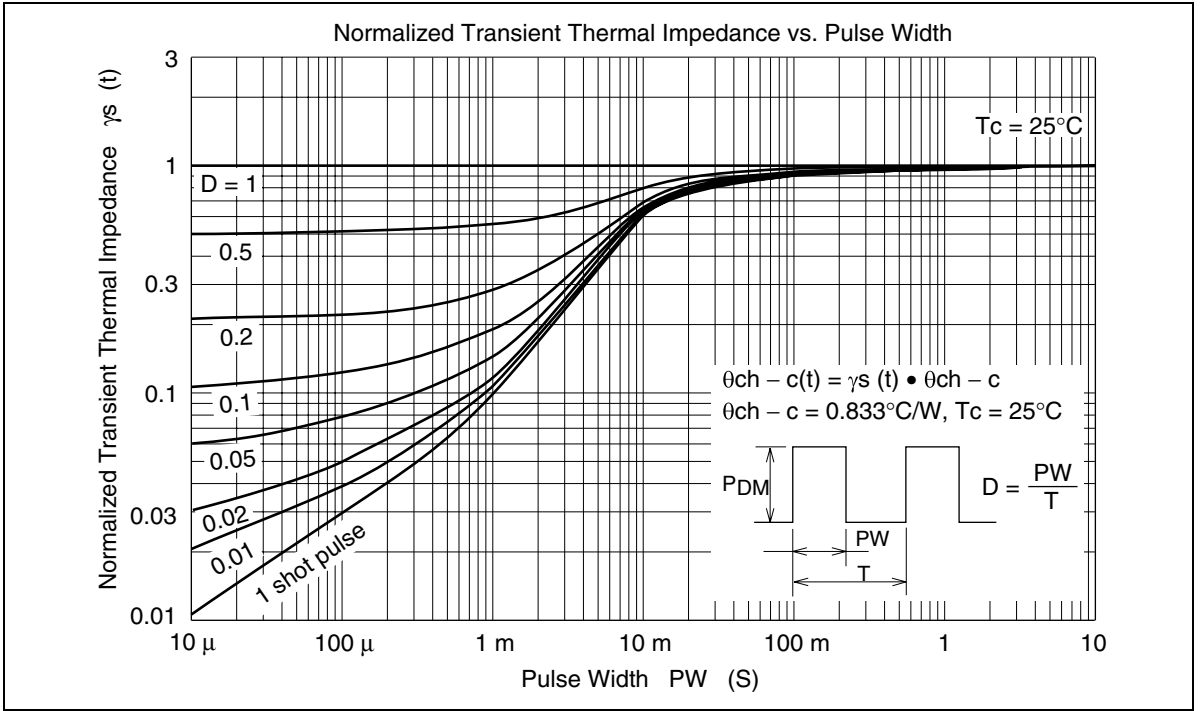


Switching Time Test Circuit



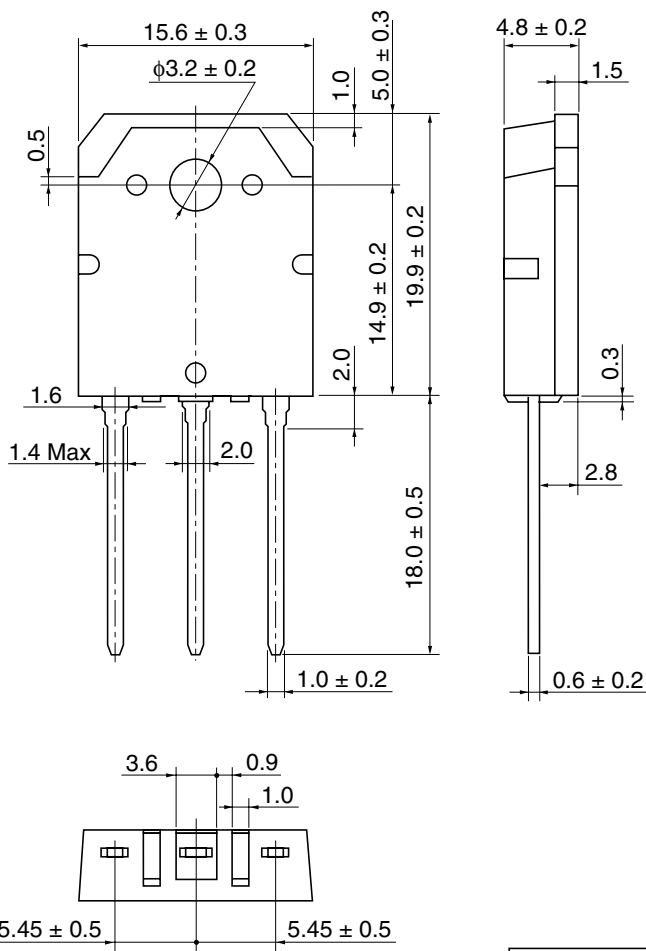
Waveform



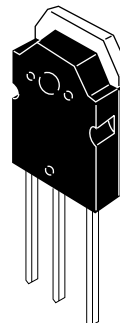




Package Dimensions



As of July, 2001  
Unit: mm



Hitachi Code	TO-3P
JEDEC	—
JEITA	Conforms
Mass (reference value)	5.0 g

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