

FQB3N60C

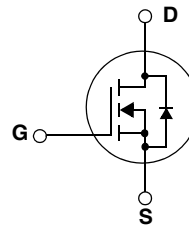
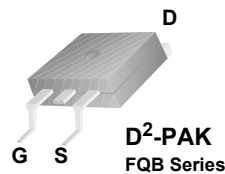
600V N-Channel MOSFET

Features

- 3A, 600V, $R_{DS(on)} = 3.4\Omega @ V_{GS} = 10V$
- Low gate charge (typical 10.5 nC)
- Low C_{rss} (typical 5 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.



Absolute Maximum Ratings

Symbol	Parameter	FQB3N60C	Unit
V_{DSS}	Drain-Source Voltage	600	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	3 1.8	A A
I_{DM}	Drain Current - Pulsed (Note 1)	12	A
V_{GSS}	Gate-Source voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	150	mJ
I_{AR}	Avalanche Current (Note 1)	3	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	75 0.62	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	1.67	°C/W
$R_{\theta JA}^*$	Thermal Resistance, Junction-to-Ambient*	--	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQB3N60C	FQB3N60CTM	D2-PAK	330mm	24mm	800

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	600	--	--	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250μA, Referenced to 25°C	--	0.6	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 600V, V _{GS} = 0V V _{DS} = 480V, T _C = 125°C	--	--	1 10	μA μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30V, V _{DS} = 0V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30V, V _{DS} = 0V	--	--	-100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2.0	--	4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10V, I _D = 1.5A	--	2.8	3.4	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40V, I _D = 1.5A (Note 4)	--	3.5	--	S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	--	435	565	pF
C _{oss}	Output Capacitance		--	45	60	pF
C _{rss}	Reverse Transfer Capacitance		--	5	8	pF
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 300V, I _D = 3A R _G = 25Ω (Note 4, 5)	--	12	34	ns
t _r	Turn-On Rise Time		--	30	70	ns
t _{d(off)}	Turn-Off Delay Time		--	35	80	ns
t _f	Turn-Off Fall Time		--	35	80	ns
Q _g	Total Gate Charge	V _{DS} = 480V, I _D = 3A V _{GS} = 10V (Note 4, 5)	--	10.5	14	nC
Q _{gs}	Gate-Source Charge		--	2.1	--	nC
Q _{gd}	Gate-Drain Charge		--	4.5	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	3	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	12	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0V, I _S = 3A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _S = 3A di _F /dt = 100A/μs (Note 4)	--	260	--	ns
Q _{rr}	Reverse Recovery Charge		--	1.6	--	μC

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I_{AS} = 3A, V_{DD} = 50V, L = 30mH, R_G = 25Ω, Starting T_J = 25°C
3. I_{SD} ≤ 3A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

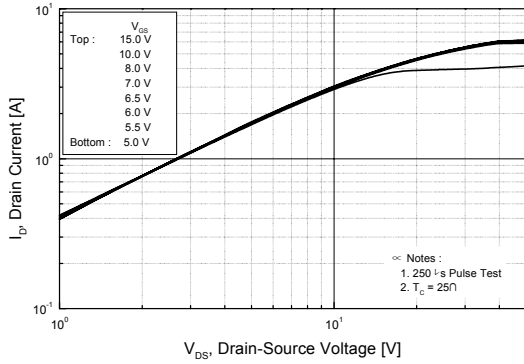


Figure 2. Transfer Characteristics

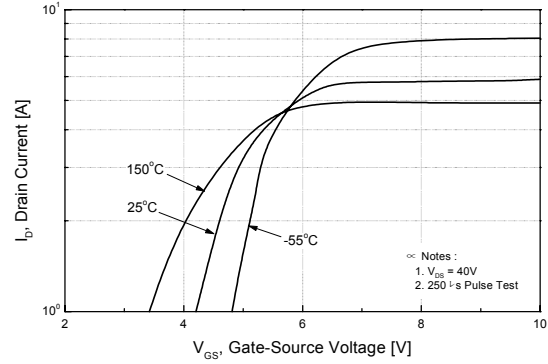


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

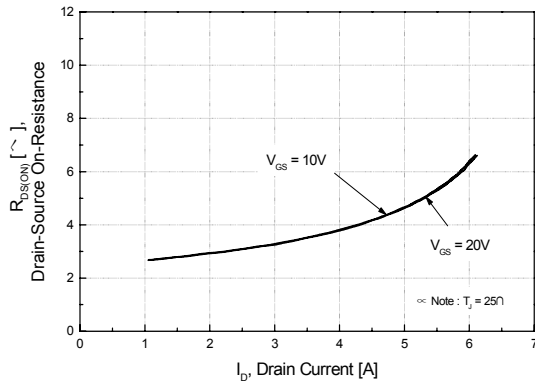


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

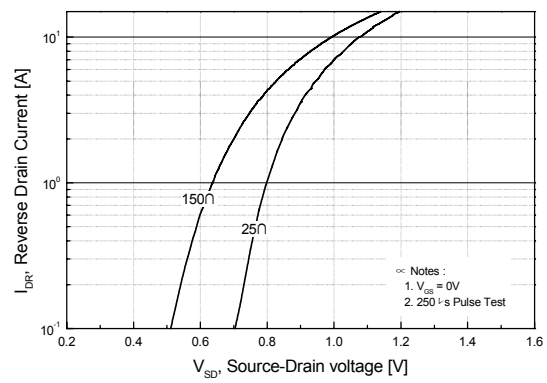


Figure 5. Capacitance Characteristics

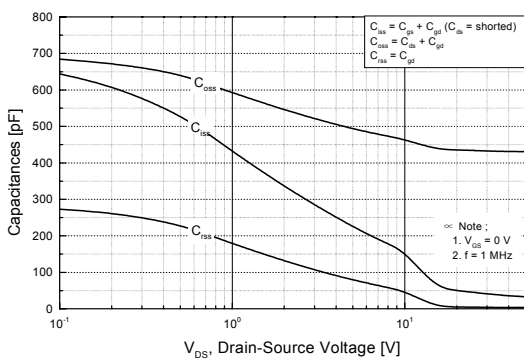
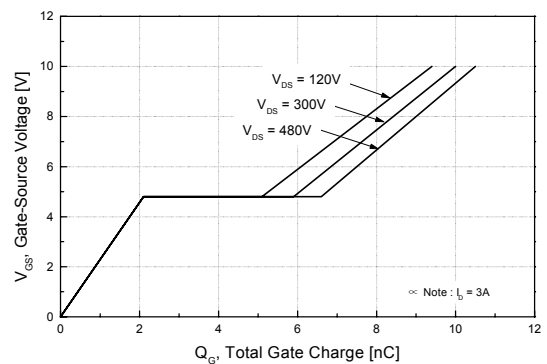


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

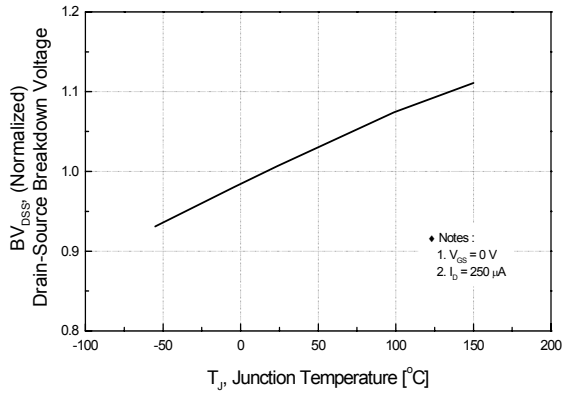


Figure 8. On-Resistance Variation vs. Temperature

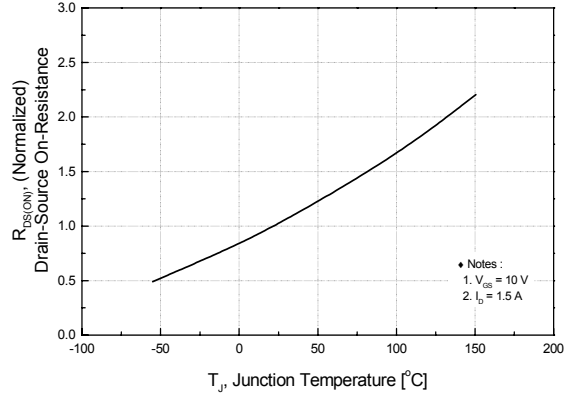


Figure 9. Maximum Safe Operating Area

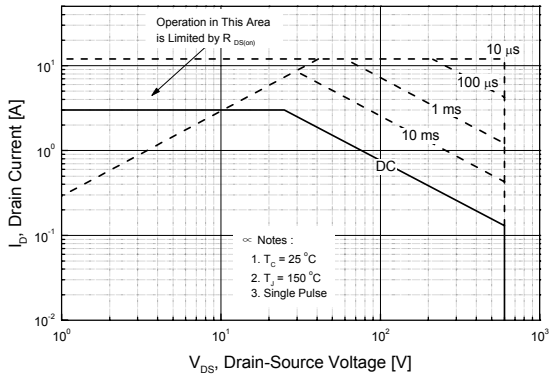


Figure 10. Maximum Drain Current vs. Case Temperature

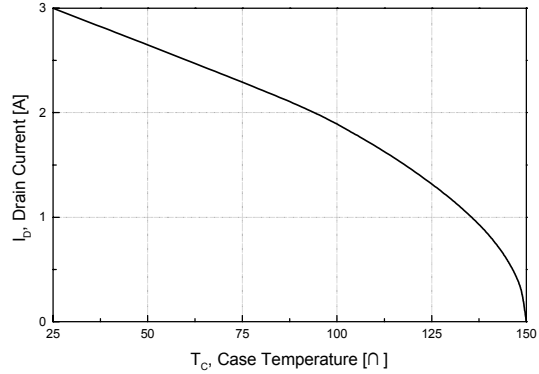
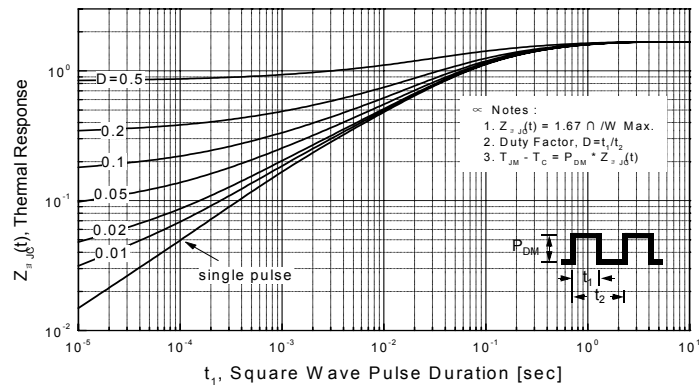
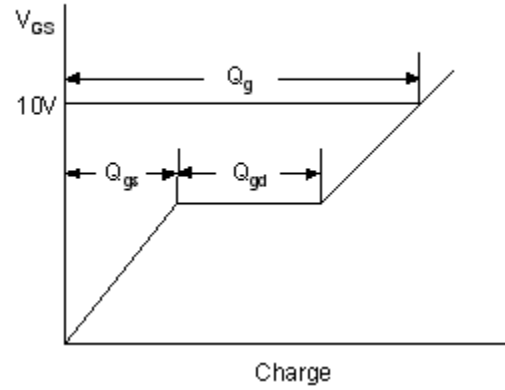
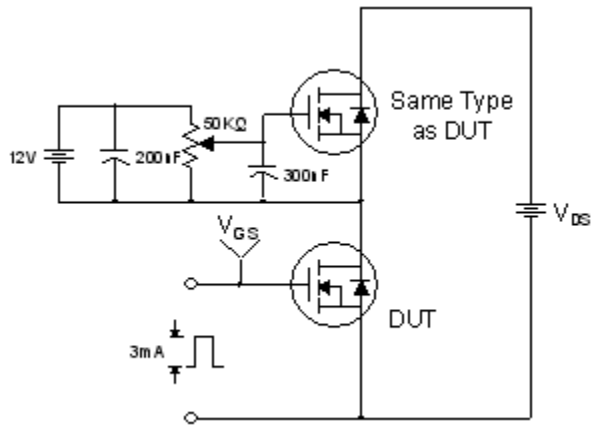


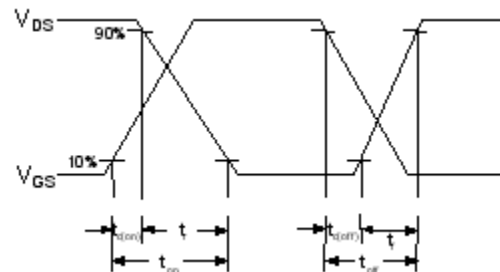
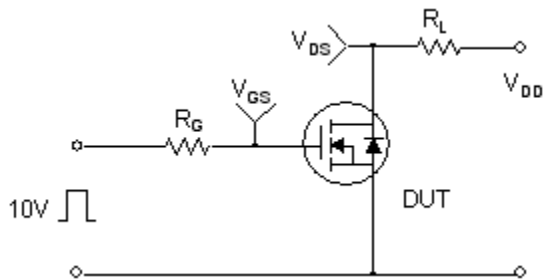
Figure 11. Transient Thermal Response Curve



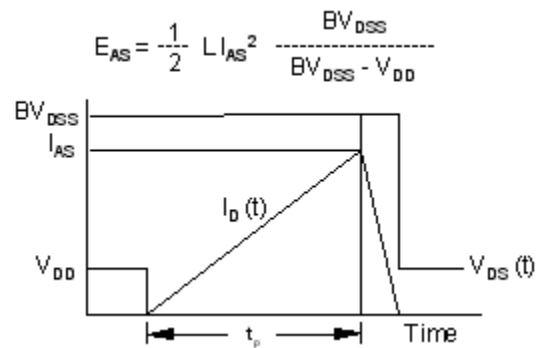
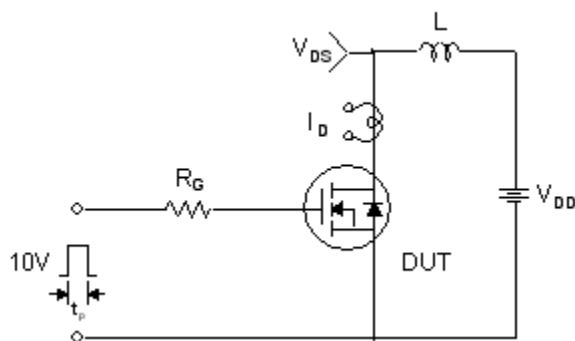
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

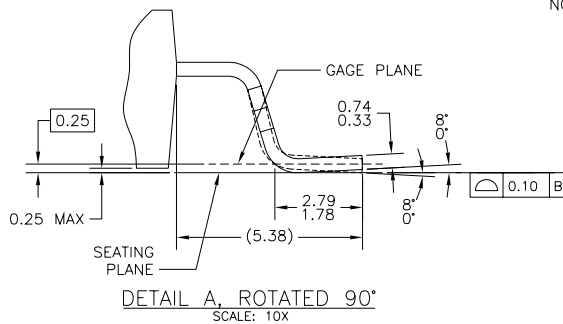
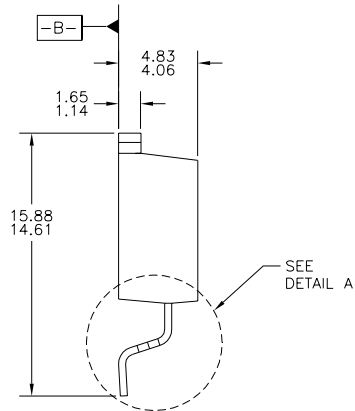
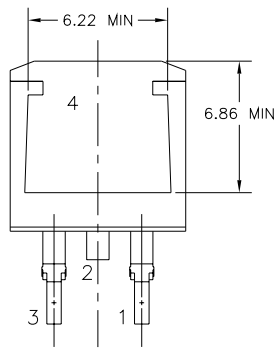
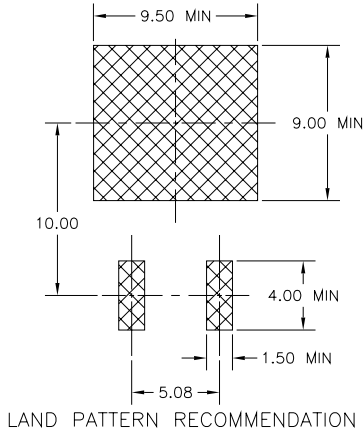
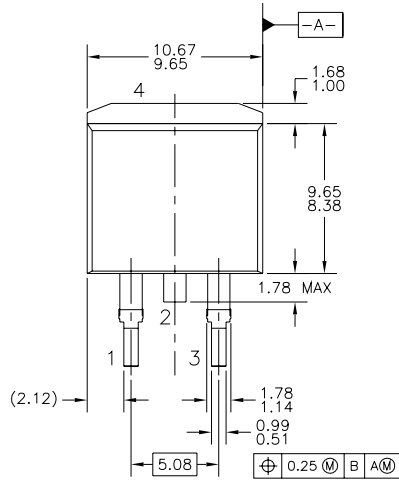


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

D2-PAK



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) REFERENCE JEDEC, TO-263, ISSUE D, VARIATION AB, DATED JULY 2003.
 - C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1982.
 - D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
 - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

T0263A02REVD

Dimensions in Millimeters

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