

**PERFORMANCE**

- ◆ 20 dBm Output Power ( $P_{1dB}$ )
- ◆ 21 dB Power Gain ( $G_{1dB}$ ) at 1.85 GHz
- ◆ 0.7 dB Noise Figure at 1.85 GHz
- ◆ 30 dBm Output IP3
- ◆ 50% Power-Added Efficiency at 1.85 GHz
- ◆ Useable Gain to 26 GHz
- ◆ Evaluation Boards Available



GATE LEAD IS ANGLED

**DESCRIPTION AND APPLICATIONS**

The *FPD200P70* is a packaged *depletion mode* AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). It utilizes a  $0.25\ \mu\text{m} \times 200\ \mu\text{m}$  Schottky barrier Gate, defined by *high-resolution stepper-based* photolithography. . The *FPD200P70* is also available in die form .

Typical applications include gain blocks and medium power stages for applications to 26 GHz.

**ELECTRICAL SPECIFICATIONS AT 22°C**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>RF SPECIFICATIONS MEASURED AT <math>f = 1850\ \text{MHz}</math> USING CW SIGNAL (except as noted)</b>						
Power at 1dB Gain Compression	$P_{1dB}$	$V_{DS} = 5\ \text{V}; I_{DS} = 50\% I_{DSS}$		20		dBm
Gain at 1dB Gain Compression	SSG	$V_{DS} = 5\ \text{V}; I_{DS} = 50\% I_{DSS}$		21		dB
Power-Added Efficiency	PAE	$V_{DS} = 5\ \text{V}; I_{DS} = 50\% I_{DSS}; P_{OUT} = P_{1dB}$		45		%
Maximum Stable Gain ( $S_{21}/S_{12}$ )	MSG	$V_{DS} = 5\ \text{V}; I_{DS} = 50\% I_{DSS}$		15		
$f = 12\ \text{GHz}$				11		
$f = 18\ \text{GHz}$						
Noise Figure	NF	$V_{DS} = 5\ \text{V}; I_{DS} = 25\% I_{DSS}$		0.7		dB
Output Third-Order Intercept Point	IP3	$V_{DS} = 5\ \text{V}; I_{DS} = 50\% I_{DSS}$		30		dBm
$P_{OUT} = 9\ \text{dBm SCL}$						
Saturated Drain-Source Current	$I_{DSS}$	$V_{DS} = 1.3\ \text{V}; V_{GS} = 0\ \text{V}$	45	60	75	mA
Maximum Drain-Source Current	$I_{MAX}$	$V_{DS} = 1.3\ \text{V}; V_{GS} \cong +1\ \text{V}$		120		mA
Transconductance	$G_M$	$V_{DS} = 1.3\ \text{V}; V_{GS} = 0\ \text{V}$		80		mS
Gate-Source Leakage Current	$I_{GSO}$	$V_{GS} = -5\ \text{V}$		1	10	$\mu\text{A}$
Pinch-Off Voltage	$ V_P $	$V_{DS} = 1.3\ \text{V}; I_{DS} = 0.2\ \text{mA}$	0.7	0.9	1.3	V
Gate-Source Breakdown Voltage	$ V_{BDGS} $	$I_{GS} = 0.2\ \text{mA}$	12	14		V
Gate-Drain Breakdown Voltage	$ V_{BDGD} $	$I_{GD} = 0.2\ \text{mA}$	14.5	16		V
Thermal Resistivity (see Notes)	$\theta_{JC}$	$V_{DS} > 3\ \text{V}$		325		$^{\circ}\text{C}/\text{W}$

**• ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	$V_{DS}$	$-3V < V_{GS} < +0V$		8	V
Gate-Source Voltage	$V_{GS}$	$0V < V_{DS} < +8V$		-3	V
Drain-Source Current	$I_{DS}$	For $V_{DS} > 2V$		$I_{DSS}$	mA
Gate Current	$I_G$	Forward or reverse current		5	mA
RF Input Power <sup>2</sup>	$P_{IN}$	Under any acceptable bias state		60	mW
Channel Operating Temperature	$T_{CH}$	Under any acceptable bias state		175	°C
Storage Temperature	$T_{STG}$	Non-Operating Storage	-40	150	°C
Total Power Dissipation	$P_{TOT}$	See De-Rating Note below		470	mW
Gain Compression	Comp.	Under any bias conditions		5	dB
Simultaneous Combination of Limits <sup>3</sup>		2 or more Max. Limits		80	%

<sup>1</sup> $T_{Ambient} = 22^{\circ}C$  unless otherwise noted      <sup>2</sup>Max. RF Input Limit must be further limited if input VSWR > 2.5:1

<sup>3</sup>Users should avoid exceeding 80% of 2 or more Limits simultaneously

**Notes:**

- Operating conditions that exceed the Absolute Maximum Ratings will result in permanent damage to the device.
- Total Power Dissipation defined as:  $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$ , where:
  - $P_{DC}$ : DC Bias Power
  - $P_{IN}$ : RF Input Power
  - $P_{OUT}$ : RF Output Power
- Total Power Dissipation to be de-rated as follows above  $22^{\circ}C$ :
  - $P_{TOT} = 470mW - (3mW/^{\circ}C) \times T_{PACK}$
  - where  $T_{PACK} =$  source tab lead temperature above  $22^{\circ}C$
  - (coefficient of de-rating formula is the Thermal Conductivity)

Example: For a  $65^{\circ}C$  source lead temperature:  $P_{TOT} = 470mW - (3 \times (65 - 22)) = 341mW$

**• HANDLING PRECAUTIONS**

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 0 (< 250V) per JESD22-A114-B, Human Body Model, and Class A (< 200V) per JESD22-A115-A, Machine Model.

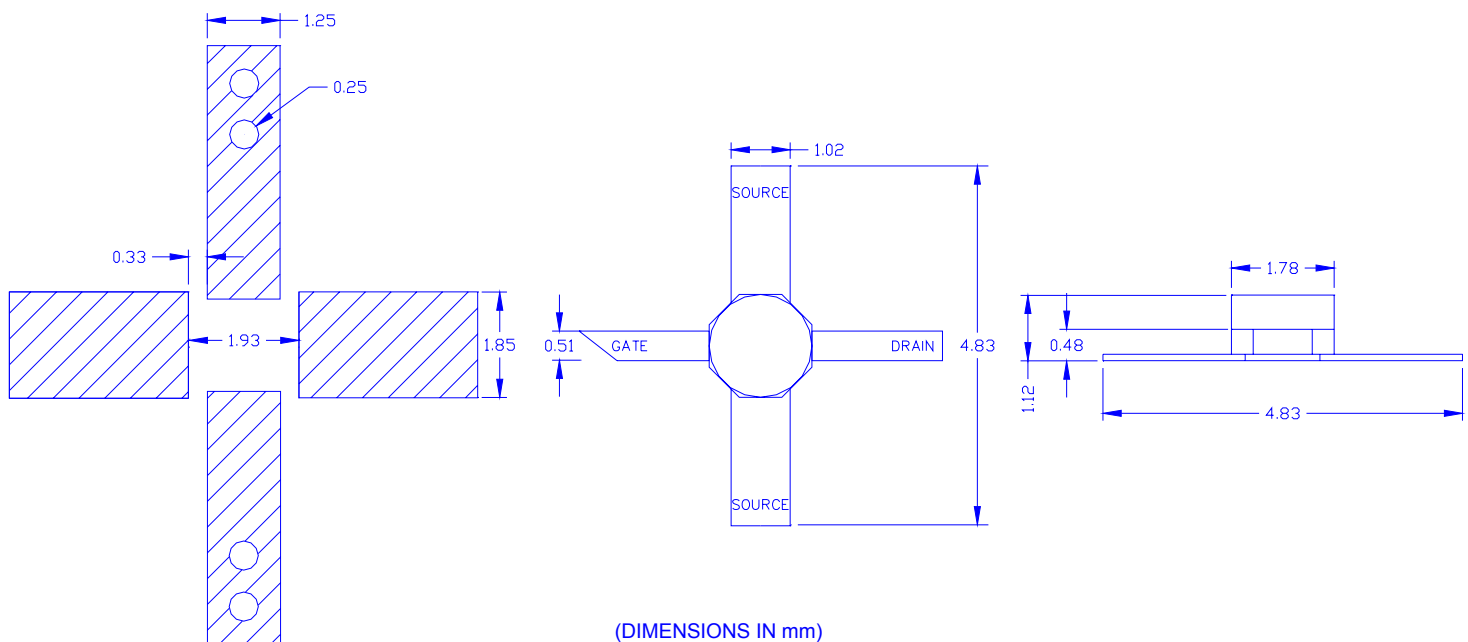
**• APPLICATIONS NOTES & DESIGN DATA**

Applications Notes are available from your local Filtronic Sales Representative or directly from the factory. Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site. Evaluation Boards available upon request.

- BIASING GUIDELINES

- Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate. Contact your Sales Representative for additional information.
- Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices such as the FPD200P70.
- For standard Class A operation, a 50% of  $I_{DSS}$  bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. Note that pHEMTs, since they are “quasi- E/D mode” devices, exhibit Class AB traits when operated at 50% of  $I_{DSS}$ . To achieve a larger separation between  $P_{1dB}$  and  $IP3$ , an operating point in the 25% to 33% of  $I_{DSS}$  range is suggested. Such Class AB operation will not degrade the  $IP3$  performance.

- PACKAGE OUTLINE AND RECOMMENDED PC BOARD LAYOUT



All information and specifications subject to change without notice.