FC1703

Receiver RFIC for Dual-Band Triple Mode

DESCRIPTION

The FC1703 is designed primarily for use in a receiver front-end of the dual-band, triple-mode system, operating in the Advanced Mobile Phone System (AMPS), Cellular Code-Division Multiple-Access (CDMA), and PCS CDMA. The IC contains low-noise amplifiers (LNA), and mixers with a balanced IF outputs. The unit operates at 2.7V single power and is designed to use with RF SAW filter. It is possible to adjust current level, gain, and IIP3 by changing resistors. The IC is manufactured on a SiGe BiCMOS process, and is packaged in a leadless small package, named MLF-24

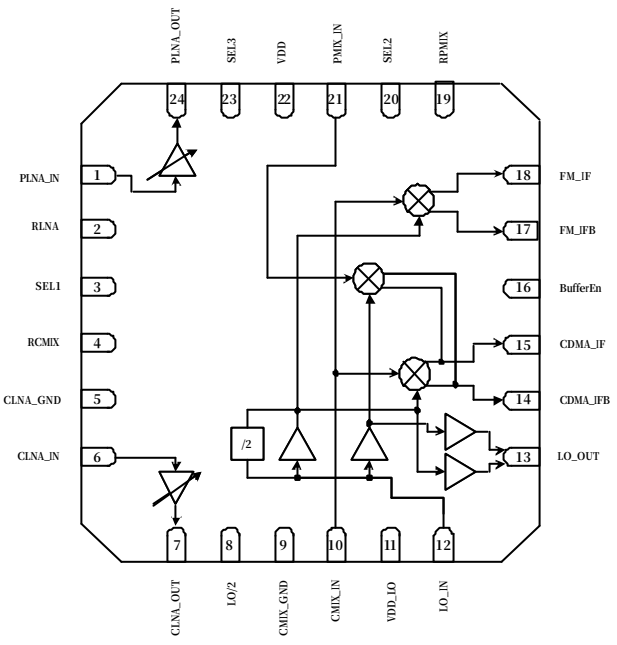
FEATURES

- Complete Receiver Front-end of the dual-band Cellular/PCS Mobile-phone System, (AMPS and CDMA)
- Integrated LNA, and Down-converting mixers
- Triple-mode of LNA
- Low Single voltage operation (2.7V)
- High Linearity
- Low power consumption
- Adjustable IIP3, Gain and Current
- 4mm x 4mm Small leadless package

APPLICATIONS

- AMPS-mode Cellular mobile phone.
- CDMA-mode Cellular mobile phone.
- Japan CDMA-mode Cellular mobile phone.
- CDMA-mode US-PCS mobile phone.
- CDMA-mode Korean-PCS mobile phone.
- Cellular CDMA/AMPS/US-PCS Dual-band Triple-mode mobile phone.
- Japan-CDMA/Korea-PCS Dual-band mobile phone
- General Purpose Down-Converter.

PIN CONFIGURATION



For latest specifications, technical questions and additional product information, visit our website or e-mail us.

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PIN DESCRIPTIONS

Pin	Function	Description	Note
1	PLNA_IN	High-Band RF Input. Requires a blocking capacitor which may be used as part of the input matching network	
2	RLNA	LNA Bias-Setting Resistor Connection	
3	SEL1	Control Pin. See Truth Table for Mode Select Pin.	
4	RCMIX	Cellular Mixer Bias-Setting Resistor Connection	
5	CLNA_GND	Ground Reference for Cellular LNA. This pin should be connected to GND through 0 ohm.	
6	CLNA_IN	Low-Band RF Input. Requires a blocking capacitor which may be used as part of the input matching network	
7	CLNA_OUT	Low-Band LNA Output Port. Connect a pull-up inductor to Vcc and an external series blocking capacitor which may be used as a part of the output matching network	
8	LO/2	LO Divider-Select Input. LOW disables LO divider, HIGH selects divider in cellular and FM modes. See Truth Table for Mode Select Pin.	
9	CMIX_GND	Ground Reference for Cellular Mixer. This pin should be connected to GND through 0 ohm.	
10	CMIX_IN	Low-Band Mixer Input. Requires a blocking capacitor which may be used as part of the input matching network.	
11	VDD_LO	Power Supply Pin for LO.	
12	LO_IN	LO Input Port. Requires an external DC blocking capacitor.	
13	LO_OUT	LO Buffer Output Port.	
14	CDMA_IFB	Mixer IFB Output.	
15	CDMA_IF	Mixer IF Output. Pin14 and 15 are matched at 50 ohm in EV Board. But they can be matched at differential 1000ohm.	
16	BufferEn	LO Output Buffer Enable. Drive BufferEn HIGH to power up the LO output buffer associated with the selected band. See Truth Table for Mode Select Pin.	
17	FM_IFB	FM IFB Output	
18	FM_IF	FM IF Output . Pin17 and 18 are matched at 50 ohm in EV Board. But they can be matched at single-ended 850ohm	
19	RPMIX	PCS Mixer Bias Setting Resistor Connection	
20	SEL2	Control Pin. See Truth Table for Mode Select Pin.	
21	PMIX_IN	High-Band Mixer Input. Requires a blocking capacitor which may be used as part of the input matching network.	
22	VDD	Power Supply Pin.	
23	SEL3	Control Pin. See Truth Table for Mode Select Pin.	
24	PLNA_OUT	High-Band LNA Output Port. Connect a pull-up inductor to Vcc and an external series blocking capacitor which may be used as a part of the output matching network	

APPLICATIONS

1. Cellular CDMA/AMPS & US-PCS

ABSOLUTE MAXIMUM RATINGS

Parameter	Unit	Rating	Note
Supply Voltage	V	-0.5~ 3.6	
Digital Input Voltage to GND	V	-0.3 ~ Vcc+0.3	
Input Power Level	dBm	+6	
Storage Temperature	℃	-40 ~ +150	
Operating Temperature	℃	-40 ~ +85	
Junction Temperature	℃	+150	
Lead Temperature(Soldering, 10sec)	℃	+240	

DC ELECTRICAL CHARACTERISTICS

(Vcc = 2.6 to 3.1V, T = -40 to +80℃, Typical values are at T = +25℃ and Vcc = 2.7V)

Parameter	Unit	Specification			Note
		Min	Typ	Max	
Supply Voltage	V		2.7		
Cellular CDMA Mode	mA		27	34	
FM Mode	mA		27	34	
US-PCS CDMA Mode	mA		20	24	
Shutdown Mode	uA		<50		
LO Buffer Supply Current	mA		7	9	BufferEn = High
Additional Operational Current Divider Active	mA		2	3	Cellular and FM mode; LO/2=High

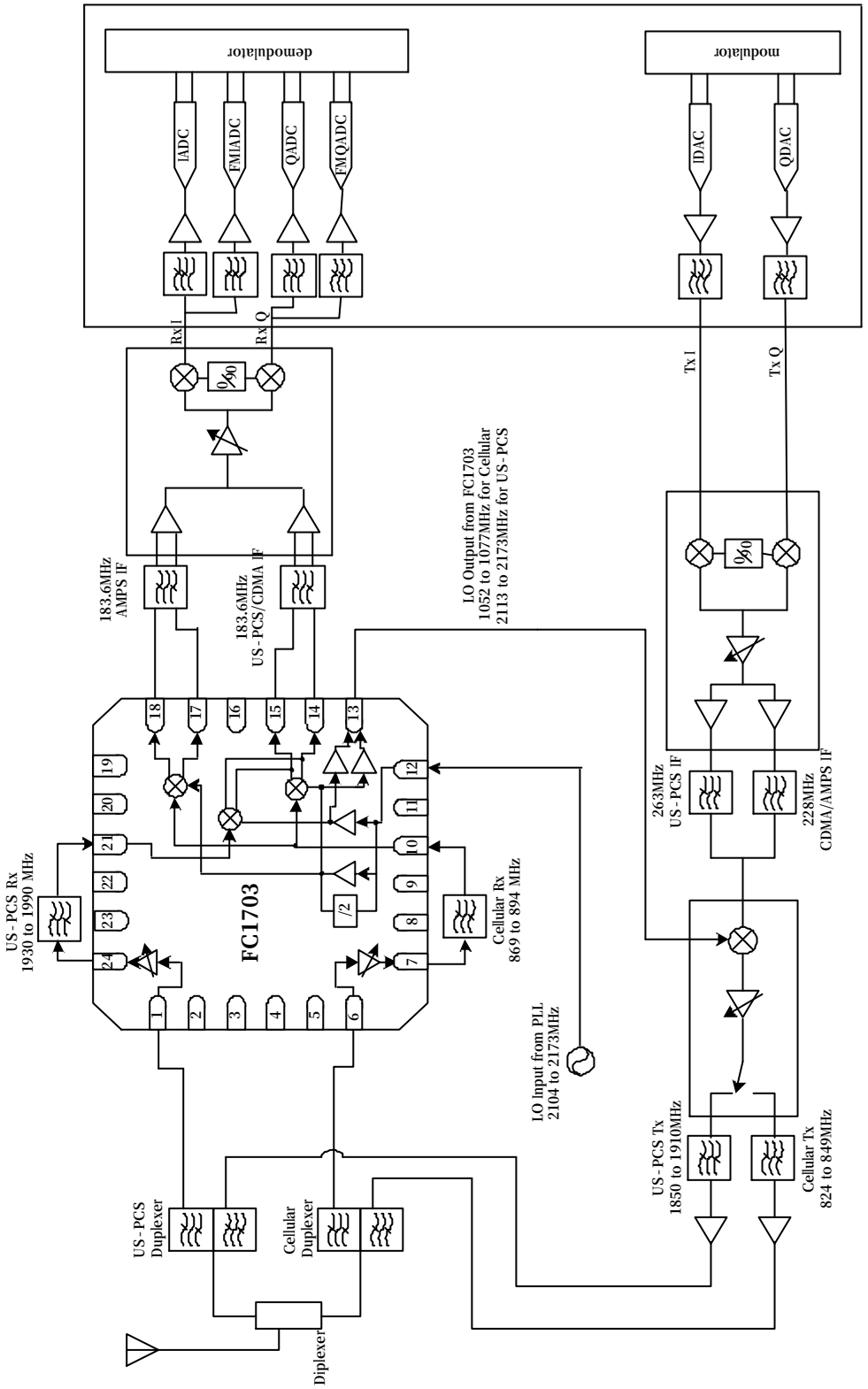
AC ELECTRICAL CHARACTERISTICS

Parameter	Unit	Specification			Note
		Min	Typ	Max	
OVERALL CONDITION					
Low-Band RF Frequency Range	MHz	869		894	
High-Band RF Frequency Range	MHz	1930		1990	
Low-Band LO Frequency Range	MHz	950		1100	
High-Band LO Frequency Range	MHz	1750		2210	
IF Frequency Range	MHz	80		220	
LO Input Level	dBm	-15	-5		

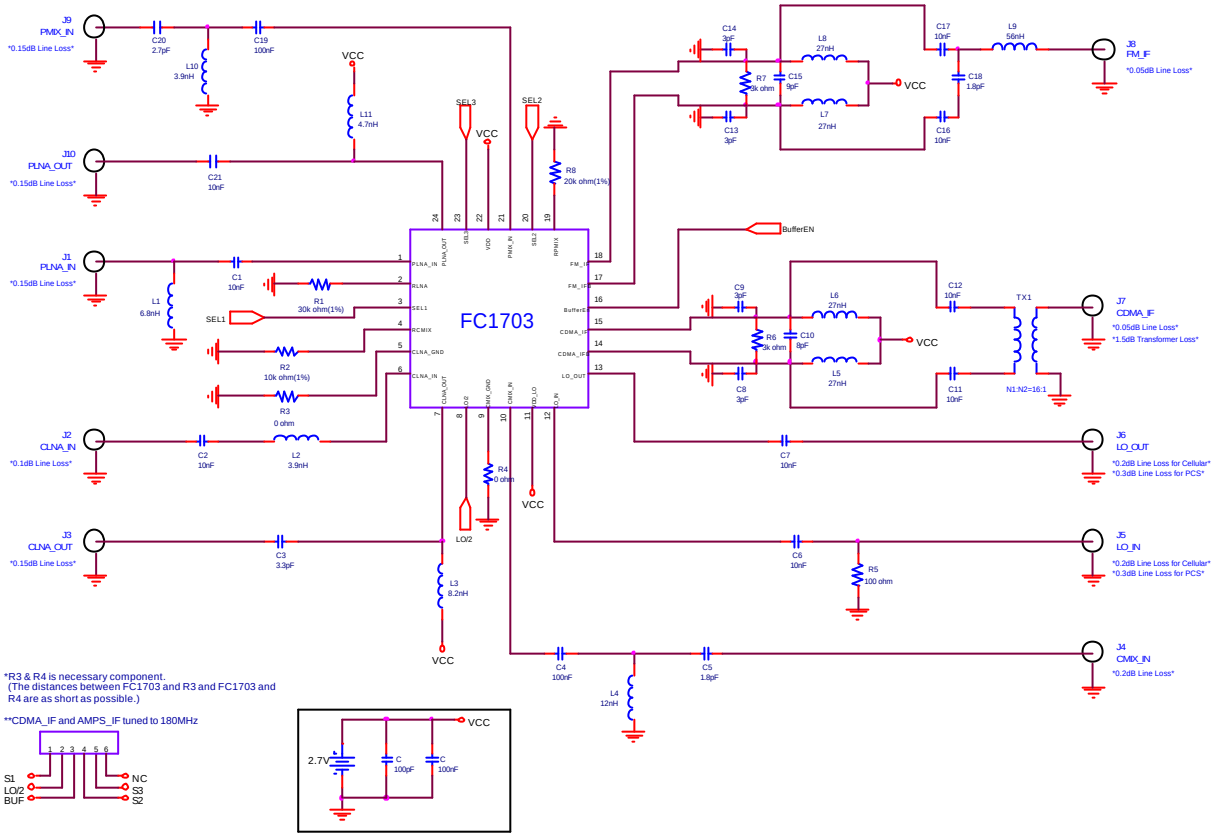
Parameter	Unit	Specification			Note
			Typ	Max	
CELLULAR LNA PERFORMANCE					
HIGH-GAIN MODE					
Gain	dB	14.5	15.5		
Noise Figure	dB		1.5	2.0	
IIP3	dBm	8	9.5		
MID-GAIN MODE					
Gain	dB	4	5		
Noise Figure	dB		4	4.5	
IIP3	dBm	8.5	10		
BYPASS MODE					
Gain	dBm	-3	-2		
Noise Figure	dB		3	3.5	
IIP3	dBm	18.5	20		
US-PCS LNA PERFORMANCE					
HIGH-GAIN MODE					
Gain	dB	15.5	16.5		
Noise Figure	dB		1.8	2.2	
IIP3	dBm	6.5	8		
BYPASS MODE					
Gain	dB	-3.5	-3		
Noise Figure	dB		4	6	
IIP3	dBm	18.5	20		
CELLULAR MIXER PERFORMANCE					
CDMA MODE					
Gain	dB	11	13		
Noise Figure	dB		7	9	
IIP3	dBm	5	8		
FM MODE					
Gain	dB	11	13		
Noise Figure	dB		7	9	
IIP3	dBm	5	8		
US-PCS MIXER PERFORMANCE					
Gain	dB	9.5	11		
Noise Figure	dB		6	8	
IIP3	dBm	3	5		
ALL MODES					
LO Output Level	dBm	-7	-6		BufferEn = HIGH PLO = -5dBm

*note : Gain, IIP3, NF and Current are adjustable by changing resistor R1,R2 and R8

SYSTEM BLOCK CONFIGURATION



TYPICAL APPLICATION SCHEMATIC (Cellular CDMA/AMPS & US-PCS)



NOTE: RF and IF matching component values are dependent on board layout, RF and IF SAW filter and the IF frequency selected. Please contact FCI application engineering for assistance.

- **Measurement Condition**

VDD : 2.7V
Low-Band LNA RF Frequency : 869 ~ 894 MHz (Center : 880 MHz) RF input Power : -30 ~ -25 dBm
Low-Band Mixer RF Frequency : 869 ~ 894 MHz (Center : 880 MHz) RF input Power : -30 ~ -25 dBm
Low-Band Mixer LO Frequency : 2098 ~ 2148 MHz (Center : 2120 MHz) LO input Power : -5 dBm
High-Band LNA RF Frequency : 1930 ~ 1990 MHz (Center : 1960 MHz) RF input Power : -30 ~ -25 dBm
High-Band Mixer RF Frequency :1930 ~ 1990 MHz (Center : 1960 MHz) RF input Power : -30 ~ -25 dBm
High-Band Mixer LO Frequency :2110 ~ 2170 MHz (Center : 2140 MHz) LO input Power : -5 dBm
Mixer IF Frequency : 180 MHz

2. J-CDMA & K-PCS

ABSOLUTE MAXIMUM RATINGS

Parameter	Unit	Rating	Note
Supply Voltage	V	-0.5~ 3.6	
Digital Input Voltage to GND	V	-0.3 ~ Vcc+0.3	
Input Power Level	dBm	+6	
Storage Temperature	℃	-40 ~ +150	
Operating Temperature	℃	-40 ~ +85	
Junction Temperature	℃	+150	
Lead Temperature(Soldering, 10sec)	℃	+240	

DC ELECTRICAL CHARACTERISTICS

(Vcc = 2.6 to 3.1V, T = -40 to +80℃, Typical values are at T = +25℃ and Vcc = 2.7V)

Parameter	Unit	Specification			Note
		Min	Typ	Max	
Supply Voltage	V		2.7		
J-CDMA Mode	mA		27	34	
K-PCS CDMA Mode	mA		20	24	
Shutdown Mode	uA		<50		
LO Buffer Supply Current	mA		7	9	BufferEn = High
Additional Operational Current Divider Active	mA		2	3	J-CDMA mode; LO/2=High

AC ELECTRICAL CHARACTERISTICS

Parameter	Unit	Specification			Note
		Min	Typ	Max	
OVERALL CONDITION					
J-CDMA RF Frequency Range	MHz	831		871	
K-PCS RF Frequency Range	MHz	1840		1870	
LO Frequency Range	MHz	2000		2110	
IF Frequency Range	MHz		183.6		
LO Input Level	dBm	-15	-5		

Parameter	Unit	Specification			Note
		Min	Typ	Max	
J-CDMA LNA PERFORMANCE					
HIGH-GAIN MODE					
Gain	dB	14.5	15.5		*note
Noise Figure	dB		1.5	2.0	*note
IIP3	dBm	8	9.5		*note
MID-GAIN MODE					
Gain	dB	4	5		
Noise Figure	dB		4	4.5	
IIP3	dBm	8.5	10		
BYPASS MODE					
Gain	dBm	-3	-2		
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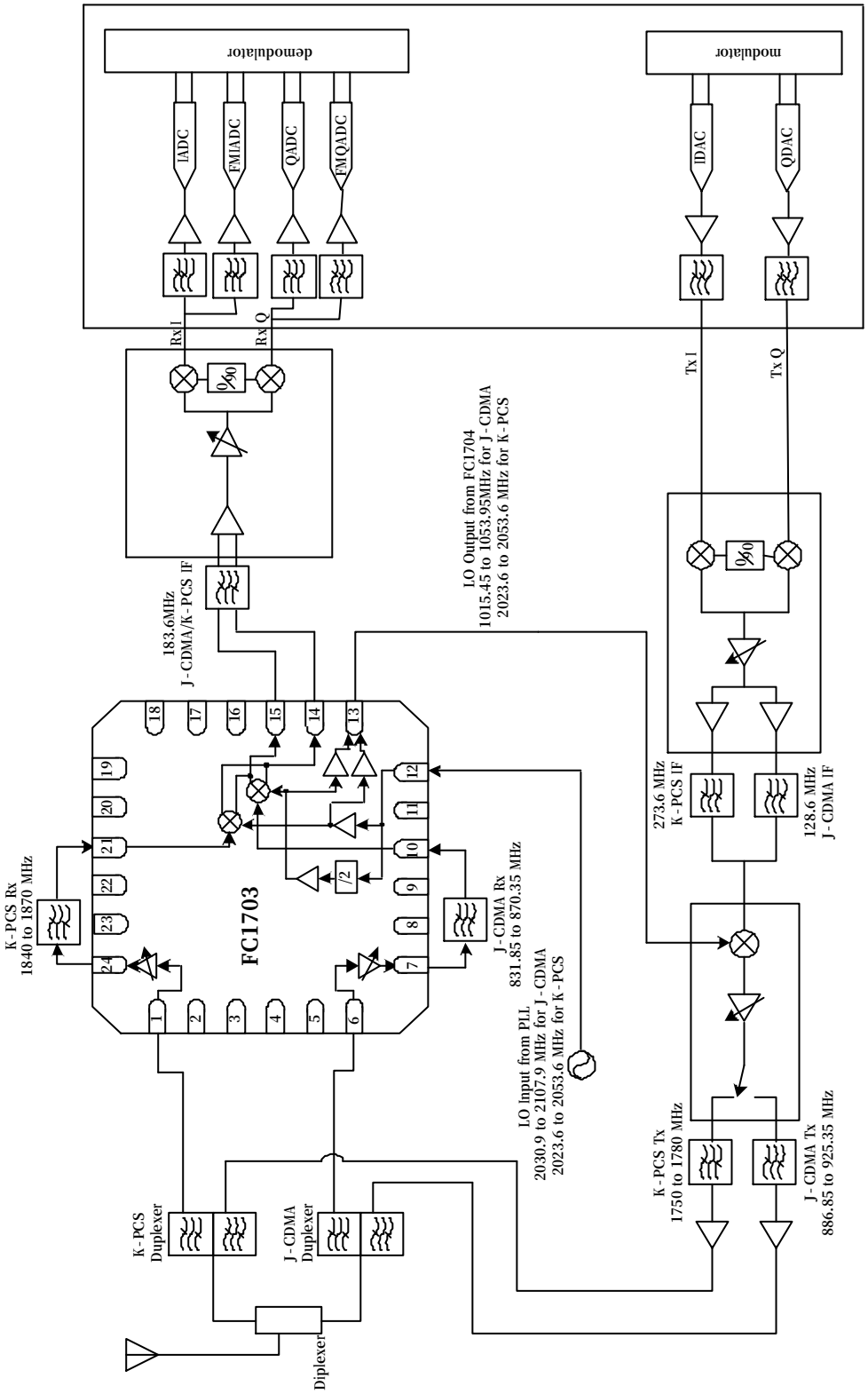
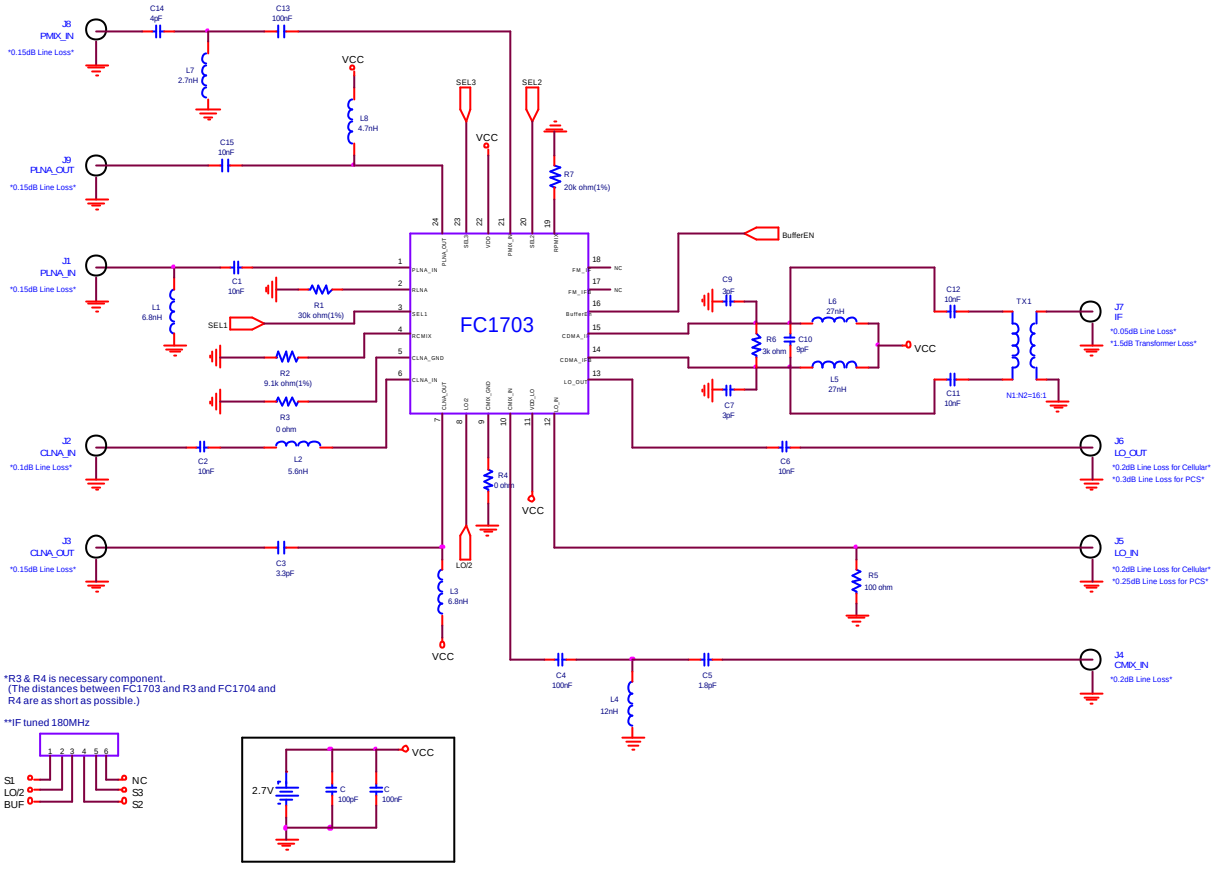
IIP3	dBm	18.5	20		
K-PCS LNA PERFORMANCE					
HIGH-GAIN MODE					
Gain	dB	15.5	16.5		*note
Noise Figure	dB		1.8	2.2	*note
IIP3	dBm	6.5	8		*note
BYPASS MODE					
Gain	dB	-3.5	-3		
Noise Figure	dB		4	6	
IIP3	dBm	18.5	20		
J-CDMA MIXER PERFORMANCE					
Gain	dB	11	13		*note
Noise Figure	dB		7	9	*note
IIP3	dBm	5	8		*note
K-PCS MIXER PERFORMANCE					
Gain	dB	9	10.5		*note
Noise Figure	dB		6	8	*note
IIP3	dBm	3	5		*note
ALL MODES					
LO Output Level	dBm	-7	-6		BufferEn = HIGH PLO = -5dBm

*note : Gain, IIP3, NF and Current are adjustable by changing resistor R1,R2 and R8

SYSTEM BLOCK CONFIGURATION



TYPICAL APPLICATION SCHEMATIC (J-CDMA & K-PCS)



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- **Measurement Condition**

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  Low-Band Mixer RF Frequency : 869 ~ 894 MHz (Center : 880 MHz) RF input Power : -30 ~ -25 dBm
  Low-Band Mixer LO Frequency : 2098 ~ 2148 MHz (Center : 2120 MHz) LO input Power : -5 dBm
  High-Band LNA RF Frequency : 1930 ~ 1990 MHz (Center : 1960 MHz) RF input Power : -30 ~ -25 dBm
  High-Band Mixer RF Frequency :1930 ~ 1990 MHz (Center : 1960 MHz) RF input Power : -30 ~ -25 dBm
  High-Band Mixer LO Frequency :2110 ~ 2170 MHz (Center : 2140 MHz) LO input Power : -5 dBm
  Mixer IF Frequency : 180 MHz

TRUTH TABLE FOR MODE SELECT PIN

1. Mode Selection & Gain Control

MODE	SEL1	SEL2	SEL3
Cellular CDMA with High-Gain LNA	0	0	0
Cellular CDMA with Mid-Gain LNA	0	0	1
Cellular CDMA with bypass LNA	0	1	0
Cellular FM	0	1	1
PCS CDMA with High-Gain LNA	1	0	0
PCS CDMA with bypass LNA	1	1	0
Power Down	1	1	1

2. LO Divider Control

Band	Mode	LO/2
Cellular AMPS / CDMA	LO (Use 1GHz band)	0
	LO/2 (User 2.1GHz band)	1

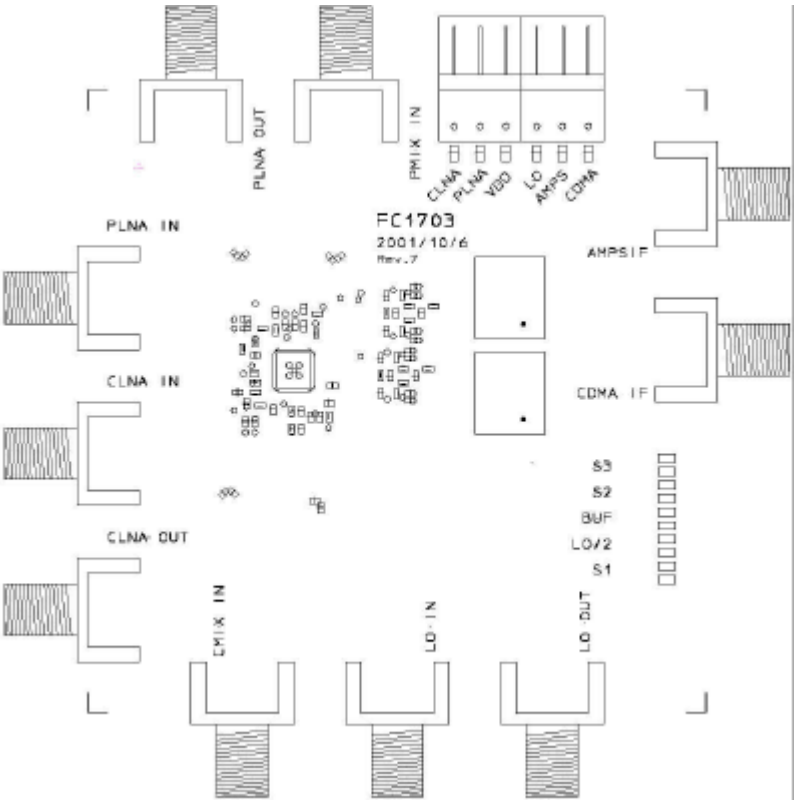
3. LO Output Buffer Control

Band	Mode	BufferEN
Cellular AMPS / CDMA	LO Output Buffer for Tx OFF	0
	LO Output Buffer for Tx ON	1
PCS	LO Output Buffer for Tx OFF	0
	LO Output Buffer for Tx ON	1

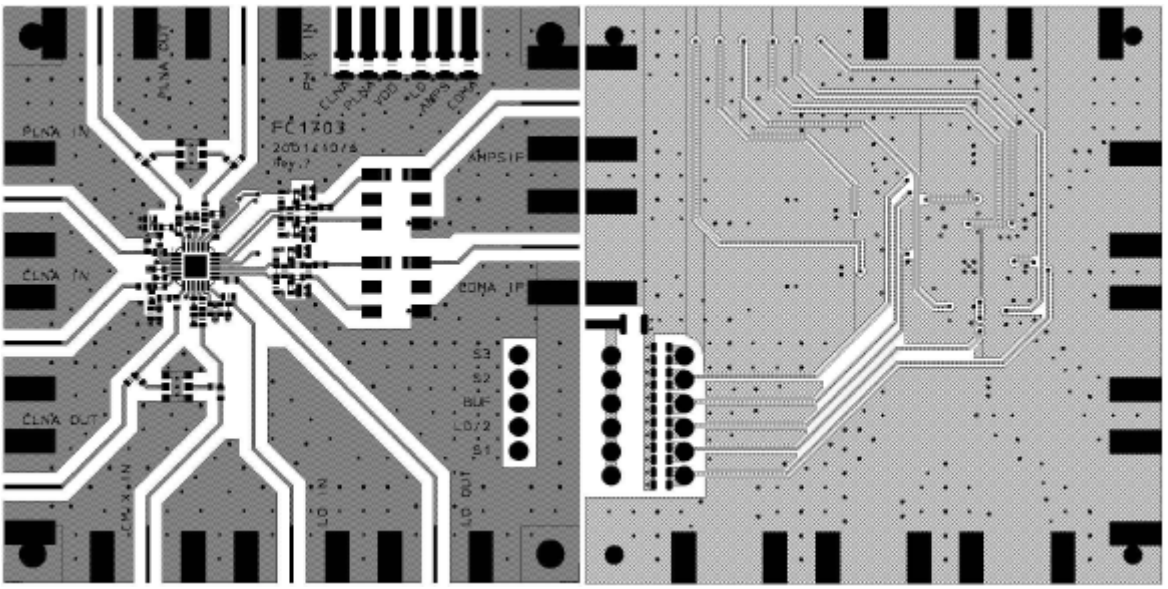
EVALUATION BOARD INFORMATIONS

Board Size 6cm x 6cm, Board Thickness 0.8mm, Board Material FR-4, Multi-Layer

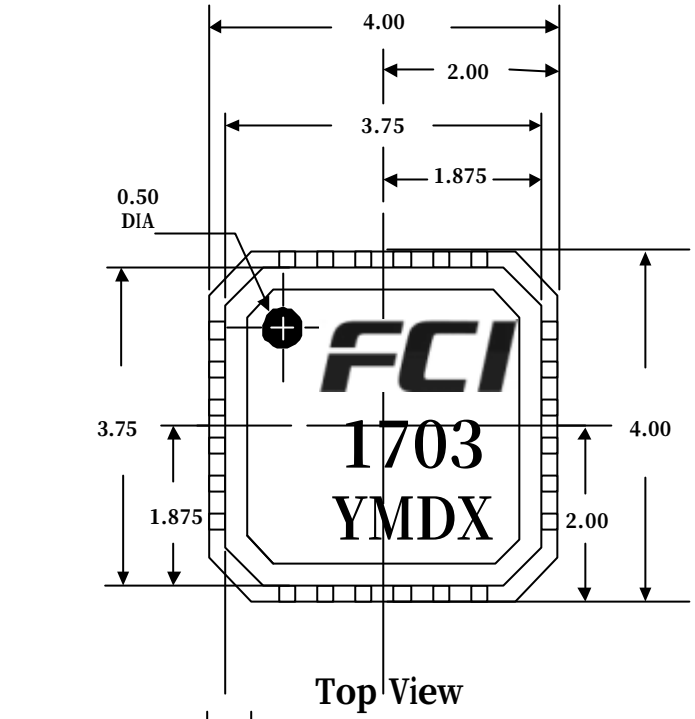
Assembly



Top **Back**

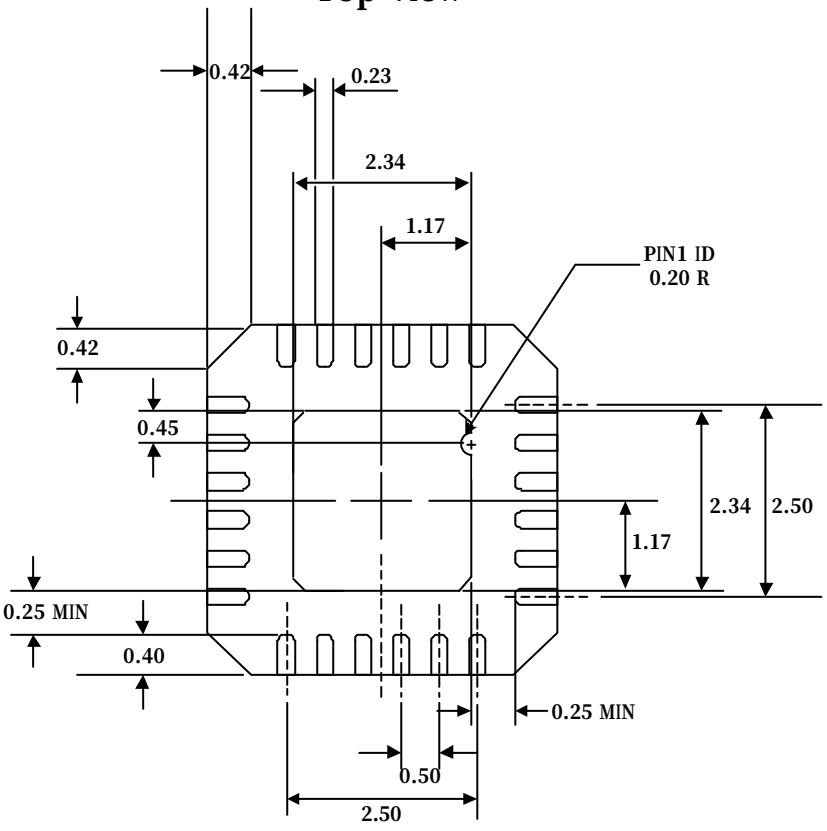


PACKAGE INFORMATION

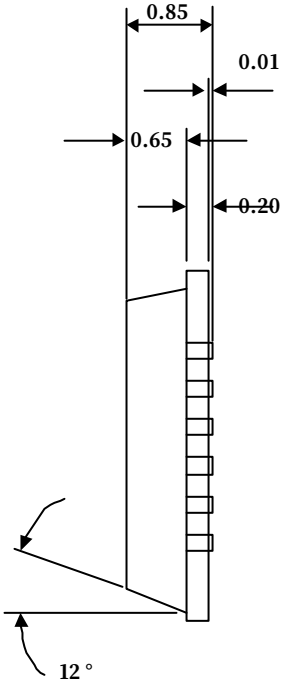


Top View

Line	Device Marking Description
1	FCI's Company Name
2	1703 = Product Name
3	YMDX LOT Code Y = Year code M = Month code D = Day code X = Manufacture code
⊕	Pin 1 Identifier



Bottom View



Side View

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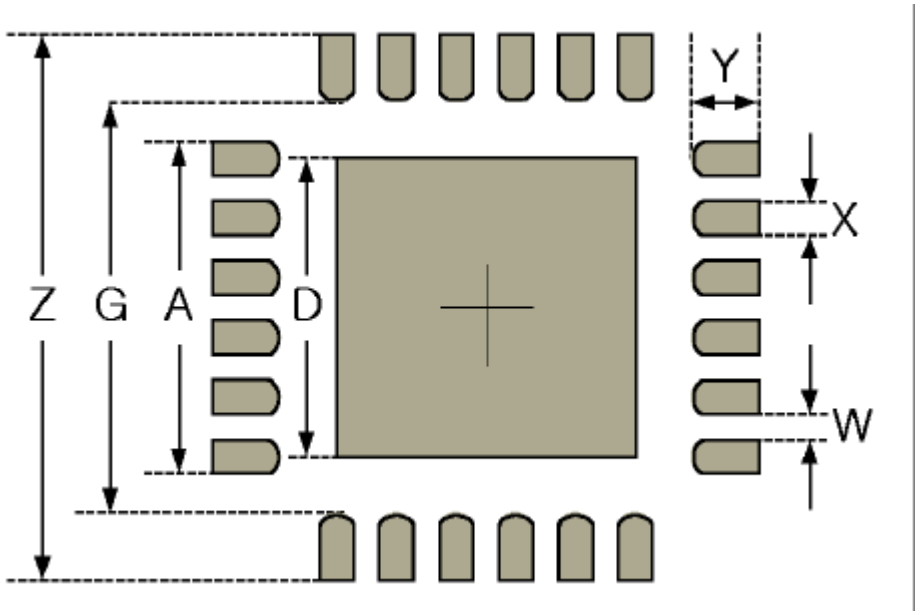
RECOMMENDED BOARD LAND PATTERN DIMENSIONS

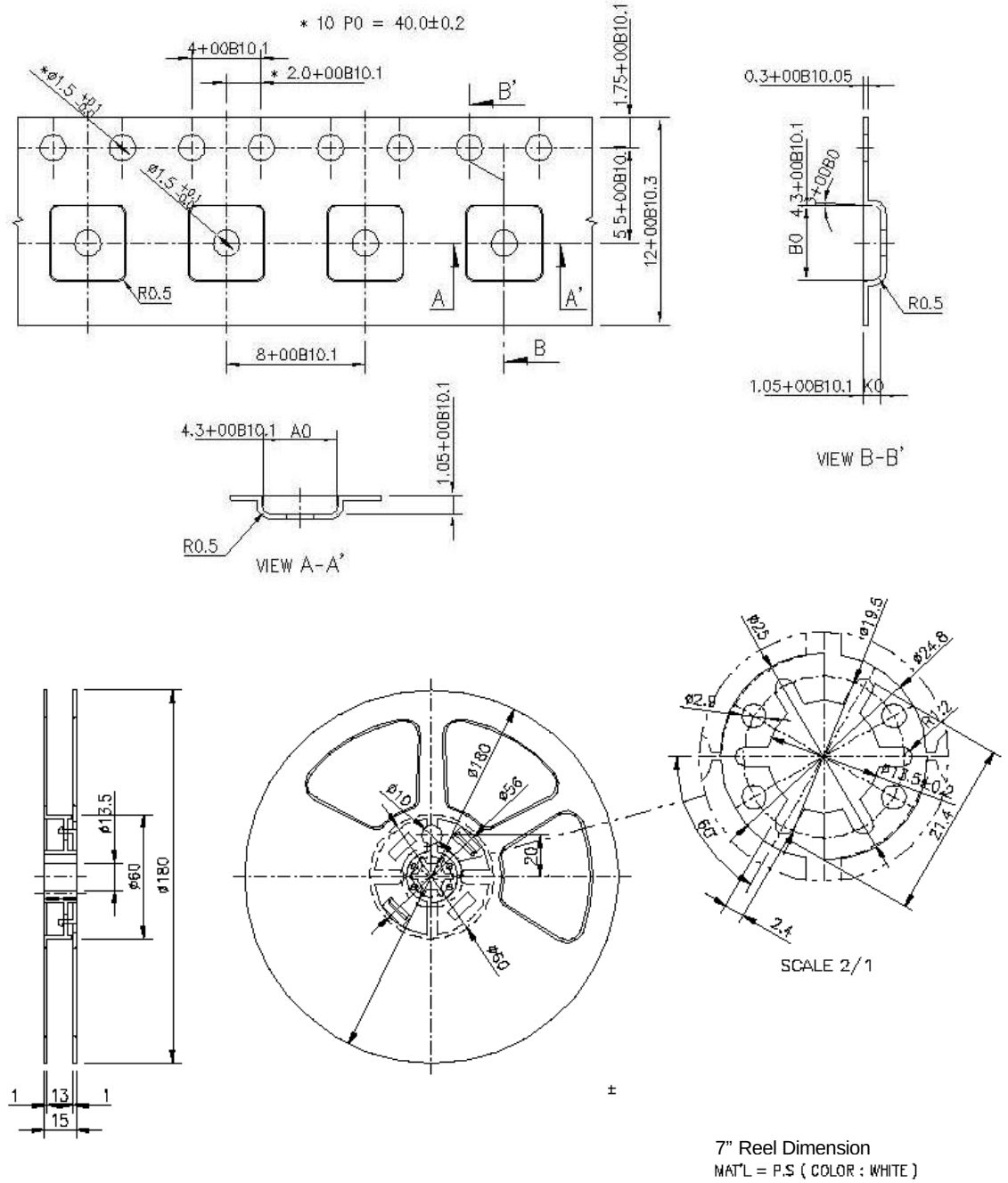


	Z	G	A	D	W	X	Y
Size	4.36	2.98	2.78	2.68	0.22	0.28	0.69

All Dimensions in mm

- *The solder mask opening should be 120 to 150 microns larger than the pad size resulting in 60 to 75 micron clearance between the copper pad and solder mask.*
- *Typically each pad on the PCB should have its own solder mask opening with a web of solder mask between two adjacent pads.*
- *It should be noted that the inner edge of the solder mask should be rounded, especially for corner leads to allow for enough solder mask web in the corner area.*
- *It is recommended that an array of thermal vias should be incorporated at 1.0 to 1.2mm pitch with via diameter of 0.3 to 0.33mm.*
- *The mask opening should be 100 microns smaller than the thermal land size on all four sides.*
- *The solder mask diameter should be 100 microns larger than the via diameter.*

TAPE / REEL FORMS AND DIMENSIONS



7" Reel Dimension
MAT'L = P.S (COLOR : WHITE)

ORDERING INFORMATION

	No of Device	Container
FC1203_BLK	10	Bulk (Anti-static bag)
FC1203_TR1	1,500	7" tape and reel
FC1203_TR2	2,500	13" tape and reel
FC1203_EVB	1	Anti-static bag

RECOMMENDED CONDITION FOR REFLOW SOLDERING

Figure 1 shows the typical process flow for mounting surface mount packages to printed circuit boards. The same process can be used for mounting the MLFs without any modifications. It is important to include post print and post reflow inspection, especially during process development. The volume of paste printed should be measured either by 2D or 3D techniques. The paste volume should be around 80 to 90% of stencil aperture volume to indicate good paste release. After reflow, the mounted package should be inspected in transmission x-ray for the presence of voids, solder balling, or other defects. Cross-sectioning may also be required to determine the fillet shape and size and joint standoff height.

A typical reflow profile for No Clean solder paste is shown in Figure 2. Since the actual reflow profile depends on the solder paste being used and the board density, a specific profile is not recommended. However, the temperature should not exceed 240℃ and the time above liquidus temperature should be less than 75 seconds. The maximum temperature can be increased for Pb free solder if the package has been qualified for higher temperature moisture sensitivity level. The ramp rate during preheat should be 3℃/second or lower.

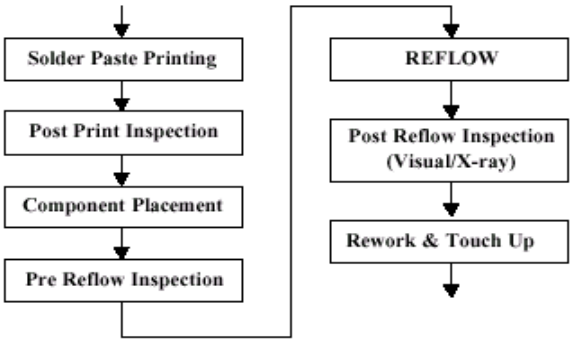


Figure 1. Typical PCB Mounting Process Flow.

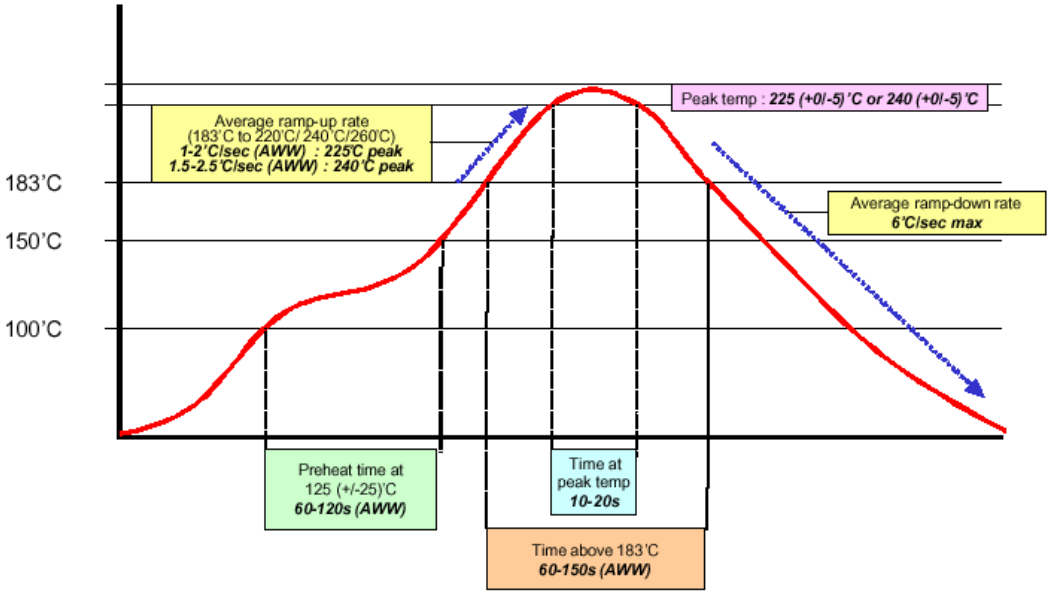


Figure 2. Typical Solder Reflow Profile

(from Application Notes for Amkor's MLF Package)

REWORK GUIDELINES

Since solder joints are not fully exposed in the case of MLFs, any retouch is limited to the side fillet. For defects underneath the package, the whole package has to be removed. Rework of MLF packages can be a challenge due to their small size. In most applications, MLFs will be mounted on smaller, thinner, and denser PCBs that introduces further challenges due to handling and heating issues. Since reflow of adjacent parts is not desirable during rework, the proximity of other components may further complicate this process. Because of the product dependent complexities, the following only provides a guideline and a starting point for the development of a successful rework process for these packages.

The rework process involves the following steps:

- Component Removal
- Site Redress
- Solder Paste Application,
- Component Placement, and
- Component Attachment.

These steps are discussed in the following in more detail. Prior to any rework, it is strongly recommended that the PCB assembly be baked for at least 4 hours at 125°C to remove any residual moisture from the assembly.

4.1. Component Removal

The first step in removal of component is the reflow of solder joints attaching component to the board. Ideally the reflow profile for part removal should be the same as the one used for part attachment. However, the time above liquidus can be reduced as long as the reflow is complete.

In the removal process, it is recommended that the board should be heated from the bottom side using convective heaters and hot gas or air should be used on the top side of he component. Special nozzles should be used to direct the heating in the component area and heating of adjacent components should be minimized. Excessive airflow should also be avoided since this may cause CSP to skew. Air velocity of 15 – 20 liters per minute is a good starting point.

Once the joints have reflowed, the Vacuum lift-off should be automatically engaged during the transition from reflow to cooldown. Because of their small size the vacuum pressure should be kept below 15" of Hg. This will allow the component not to be lifted out if all joints have not been reflowed and avoid the pad liftoff.

4.2. Site Redress

After the component has been removed, the site needs to be cleaned properly. It is best to use a combination of a blade-style conductive tool and desoldering braid. The width of he blade should be matched to the maximum width of the footprint and the blade temperature should be low enough not to cause any damage to the circuit board. Once the residual solder has been removed, the lands should be cleaned with a solvent. The solvent is usually specific to the type of paste used in the original assembly and paste manufacturer's recommendations should be followed.

4.3. Solder Paste Printing

Because of their small size and finer pitches, solder paste deposition for MLFs requires extra care. However, a uniform and precise deposition can be achieved if miniature stencil specific to the component is used. The stencil aperture should be aligned with the pads under 50 to 100X magnification. The stencil should then be lowered onto the PCB and the paste should be deposited with a small metal squeegee blade. The blade width should be the same as the package width to ensure single pass paste deposition thus avoiding any overprinting.

The stencil thickness and aperture size and shape should be the same as used for the original assembly. Also, no-clean flux should be used, as small standoff of MLFs does not leave much room for cleaning.

4.4. Component Placement

MLF packages are expected to have superior self-centering ability due to their small mass and the placement of this package should be similar to that of BGAs. As the leads are on the underside of the package, split-beam optical system should be used to align the component on the motherboard. This will form an image of solder balls overlaid on the mating footprint and aid in proper alignment. Again, the alignment should be done at 50 to 100X magnification. The placement machine should have the capability of allowing fine adjustments in X, Y, and rotational axes.

4.5. Component Attachment

The reflow profile developed during original attachment or removal should be used to attach the new component. Since all reflow profile parameters have already been optimized, using the same profile will eliminate the need for thermocouple feedback and will reduce operator dependencies.

(from Application Notes for Amkor's MLF Package)