

450MHz Fixed Gain Amplifiers with Enable

The EL5108 and EL5308 are fixed gain amplifiers with a bandwidth of 450MHz. This makes these amplifiers ideal for today's high speed video and monitor applications. They feature internal gain-setting resistors and can be configured in a gain of +1, -1 or +2. The same bandwidth is seen in both gain-of-1 and gain-of-2 applications.

The EL5108 and EL5308 also incorporate an enable and disable function to reduce the supply current to 25 μ A typical per amplifier. Allowing the \overline{CE} pin to float or applying a low logic level will enable the amplifier.

The EL5108 is offered in the 6 Ld SOT-23 and the industry-standard 8 Ld SO packages and the EL5308 is available in the 16 Ld SO and 16 Ld QSOP packages. All operate over the industrial temperature range of -40°C to +85°C.

Features

- Pb-free plus anneal available (RoHS compliant)
- Gain selectable (+1, -1, +2)
- 450MHz -3dB BW ($A_V = -1, +1, +2$)
- 3.5mA supply current per amplifier
- Single and dual supply operation, from 5V to 12V
- Available in SOT-23 packages
- 350MHz, 1.5mA product available (EL5106 & EL5306)

Applications

- Battery powered equipment
- Handheld, portable devices
- Video amplifiers
- Cable drivers
- RGB amplifiers

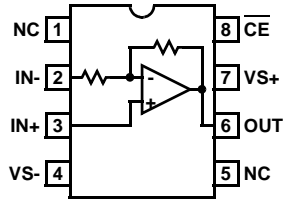
Ordering Information

PART NUMBER	PART MARKING	PACKAGE	TAPE & REEL	PKG. DWG. #
EL5108IW-T7	r	6 Ld SOT-23	7" (3K pcs)	MDP0038
EL5108IW-T7A	r	6 Ld SOT-23	7" (250 pcs)	MDP0038
EL5108IS	5108IS	8 Ld SO	-	MDP0027
EL5108IS-T7	5108IS	8 Ld SO	7"	MDP0027
EL5108IS-T13	5108IS	8 Ld SO	13"	MDP0027
EL5108ISZ (See Note)	5108ISZ	8 Ld SO	-	MDP0027
EL5108ISZ-T7 (See Note)	5108ISZ	8 Ld SO	7"	MDP0027
EL5108ISZ-T13 (See Note)	5108ISZ	8 Ld SO	13"	MDP0027
EL5308IS	EL5308IS	16 Ld SO (0.150")	-	MDP0027
EL5308IS-T7	EL5308IS	16 Ld SO (0.150")	7"	MDP0027
EL5308IS-T13	EL5308IS	16 Ld SO (0.150")	13"	MDP0027
EL5308IU	5308IU	16 Ld QSOP	-	MDP0040
EL5308IU-T7	5308IU	16 Ld QSOP	7"	MDP0040
EL5308IU-T13	5308IU	16 Ld QSOP	13"	MDP0040
EL5308IUZ (See Note)	5308IUZ	16 Ld QSOP (Pb-free)	-	MDP0040
EL5308IUZ-T7 (See Note)	5308IUZ	16 Ld QSOP (Pb-free)	7"	MDP0040
EL5308IUZ-T13 (See Note)	5308IUZ	16 Ld QSOP (Pb-free)	13"	MDP0040

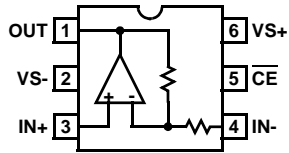
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

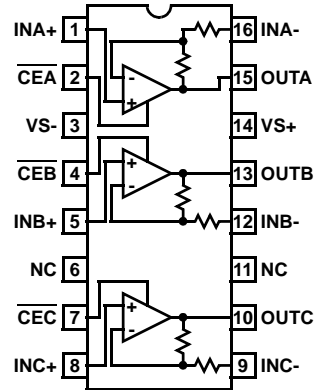
EL5108
(8 LD SO)
TOP VIEW



EL5108
(6 LD SOT-23)
TOP VIEW



EL5308
(16 LD SO, QSOP)
TOP VIEW



EL5108, EL5308

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Supply Voltage between V_{S+} and V_{S-} 13.2V
 Maximum Continuous Output Current 50mA
 Maximum Slewrate from V_{S+} to V_{S-} 1V/ μs
 Operating Junction Temperature 125°C
 Power Dissipation See Curves

Pin Voltages $V_{S-} -0.5\text{V}$ to $V_{S+} +0.5\text{V}$
 Storage Temperature -65°C to +150°C
 Ambient Operating Temperature -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications $V_{S+} = +5\text{V}$, $V_{S-} = -5\text{V}$, $R_L = 150\Omega$, $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	-3dB Bandwidth	$A_V = +1$		440		MHz
		$A_V = -1$		445		MHz
		$A_V = +2$		450		MHz
BW1	0.1dB Bandwidth	$A_V = +2$		40		MHz
SR	Slew Rate	$V_O = -2.5\text{V}$ to $+2.5\text{V}$, $A_V = +2$	3500	4500		V/ μs
t_S	0.1% Settling Time	$V_{OUT} = -2.5\text{V}$ to $+2.5\text{V}$, $A_V = +2$		10		ns
e_N	Input Voltage Noise			2		nV/ $\sqrt{\text{Hz}}$
i_N	Input Current Noise	$f = 2\text{kHz}$		12		pA/ $\sqrt{\text{Hz}}$
dG	Differential Gain Error (Note 1)	$A_V = +2$		0.01		%
dP	Differential Phase Error (Note 1)	$A_V = +2$		0.01		°
DC PERFORMANCE						
V_{OS}	Offset Voltage		-8	+3	+8	mV
$T_C V_{OS}$	Input Offset Voltage Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		5		$\mu\text{V}/^\circ\text{C}$
A_E	Gain Error	$V_O = -3\text{V}$ to $+3\text{V}$, $R_L = 150\Omega$		0.7	2.5	%
R_F, R_G	Internal R_F and R_G			325		Ω
INPUT CHARACTERISTICS						
CMIR	Common Mode Input Range		± 3	± 3.3		V
$+I_{IN}$	+ Input Current			2	8	μA
R_{IN}	Input Resistance	at I_{N+}		0.7		M Ω
C_{IN}	Input Capacitance			1		pF
OUTPUT CHARACTERISTICS						
V_O	Output Voltage Swing	$R_L = 150\Omega$ to GND	± 3.6	± 3.8		V
		$R_L = 1\text{k}\Omega$ to GND	± 3.8	± 4.0		V
I_{OUT}	Output Current	$R_L = 10\Omega$ to GND	100	135		mA
SUPPLY						
I_{SON}	Supply Current - Enabled (per amplifier)	No load, $V_{IN} = 0\text{V}$	3.18	3.7	4.35	mA
I_{SOFF}	Supply Current - Disabled (per amplifier)	No load, $V_{IN} = 0\text{V}$		9	25	μA
PSRR	Power Supply Rejection Ratio	DC, $V_S = \pm 4.75\text{V}$ to $\pm 5.25\text{V}$		75		dB

EL5108, EL5308

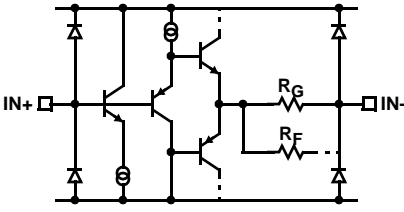
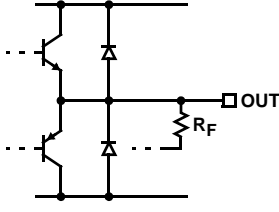
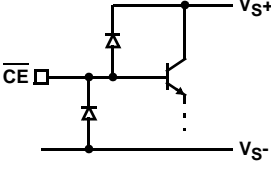
Electrical Specifications $V_{S+} = +5V$, $V_{S-} = -5V$, $R_L = 150\Omega$, $T_A = 25^\circ C$ unless otherwise specified. (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE						
t_{EN}	Enable Time			280		ns
t_{DIS}	Disable Time (Note 2)			560		ns
I_{IHCE}	\overline{CE} Pin Input High Current	$\overline{CE} = V_{S+}$	-1	5	25	μA
I_{ILCE}	\overline{CE} Pin Input Low Current	$\overline{CE} = V_{S-}$	+1		-1	μA
V_{IHCE}	\overline{CE} Input High Voltage for Power-down		$V_{S+} - 1$			V
V_{ILCE}	\overline{CE} Input Low Voltage for Enable				$V_{S+} - 3$	V

NOTES:

- Standard NTSC test, AC signal amplitude = 286mV_{p-p}, f = 3.58MHz
- Measured from the application of the \overline{CE} logic signal until the output voltage is at the 50% point between initial and final values

Pin Descriptions

EL5108 (SO8)	EL5108 (SOT23-6)	EL5308 (SO16, QSOP16)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
1, 5		6, 11	NC	Not connected	
2	4	9, 12, 16	IN-	Inverting input	 <p style="text-align: center;">CIRCUIT 1</p>
3	3	1, 5, 8	IN+	Non-inverting input	(Reference Circuit 1)
4	2	3	VS-	Negative supply	
6	1	10, 13, 15	OUT	Output	 <p style="text-align: center;">CIRCUIT 2</p>
7	6	14	VS+	Positive supply	
8	5	2, 4, 7	\overline{CE}	Chip enable	 <p style="text-align: center;">CIRCUIT 3</p>

Typical Performance Curves

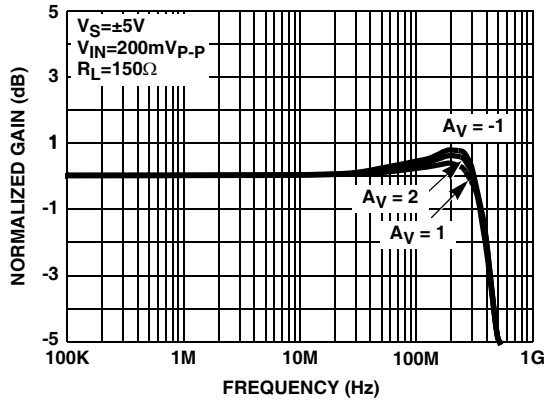


FIGURE 1. FREQUENCY RESPONSE

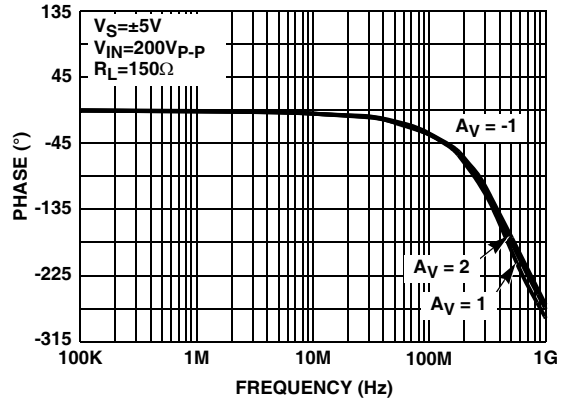


FIGURE 2. PHASE RESPONSE

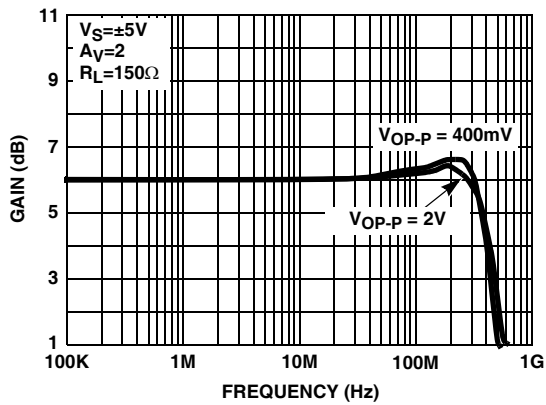


FIGURE 3. FREQUENCY RESPONSE vs OUTPUT VOLTAGE

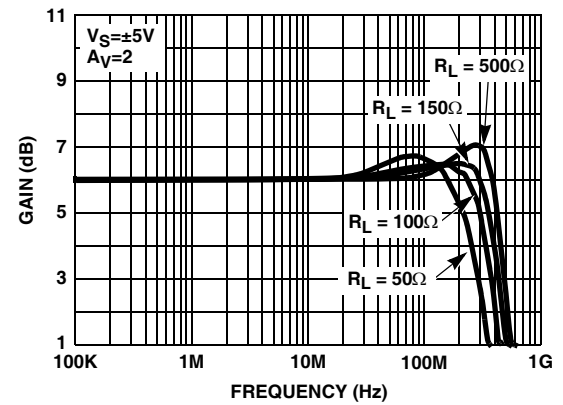


FIGURE 4. FREQUENCY RESPONSE vs R_L

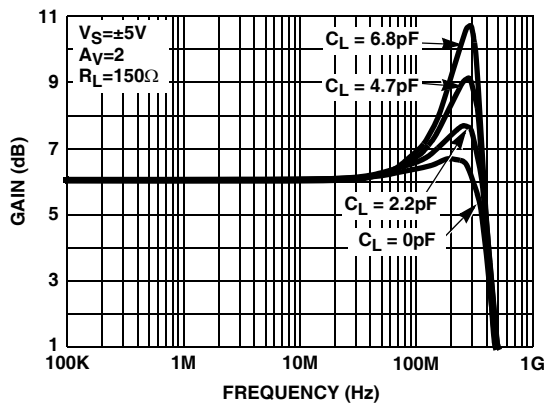


FIGURE 5. FREQUENCY RESPONSE FOR VARIOUS C_L

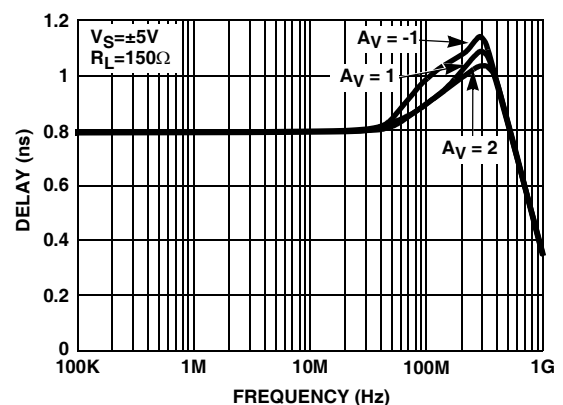


FIGURE 6. GROUP DELAY vs FREQUENCY

Typical Performance Curves (Continued)

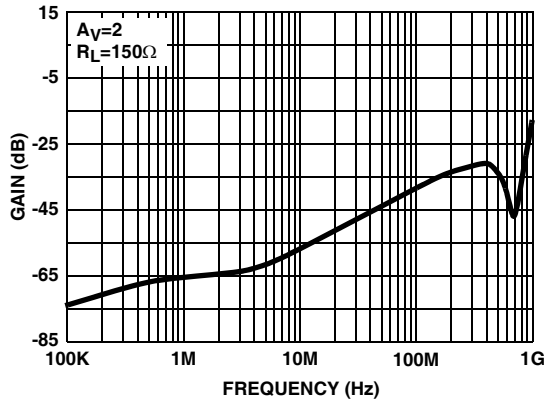


FIGURE 7. INPUT TO OUTPUT ISOLATION vs FREQUENCY (FOR DISABLE MODE)

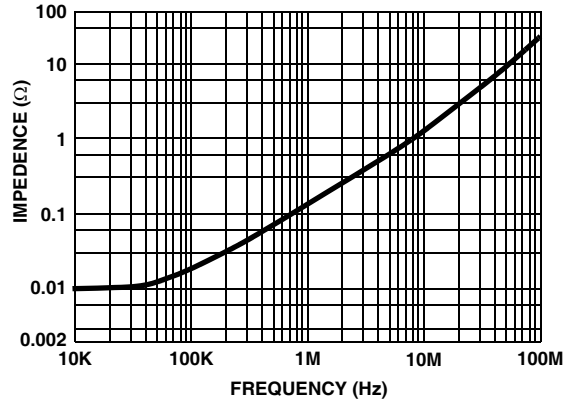


FIGURE 8. OUTPUT IMPEDANCE vs FREQUENCY

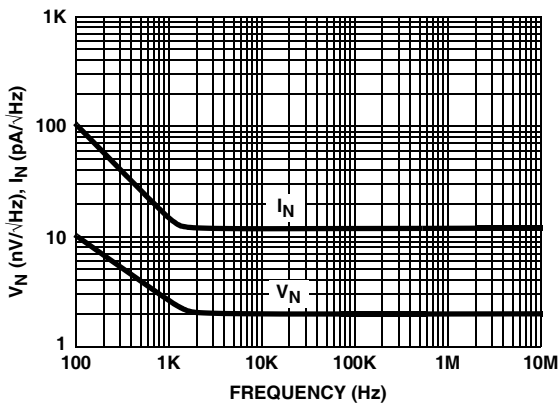


FIGURE 9. VOLTAGE AND CURRENT NOISE vs FREQUENCY

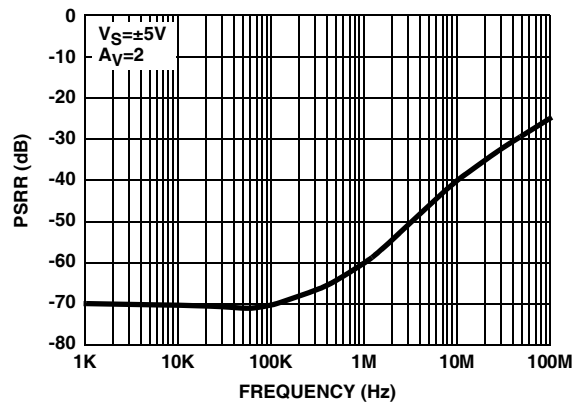


FIGURE 10. POWER SUPPLY REJECTION RATIO vs FREQUENCY

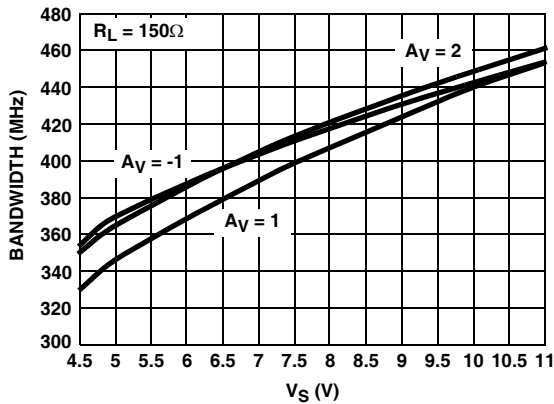


FIGURE 11. BANDWIDTH vs SUPPLY VOLTAGE

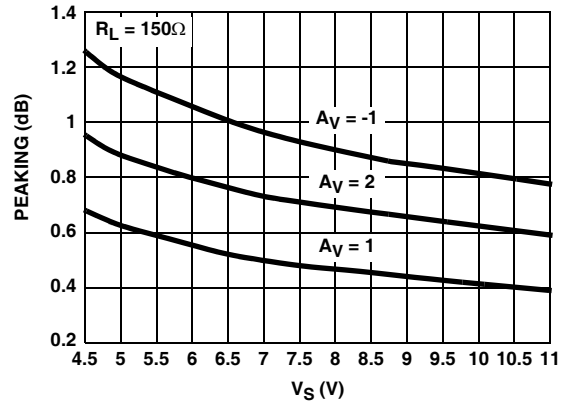


FIGURE 12. PEAKING vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

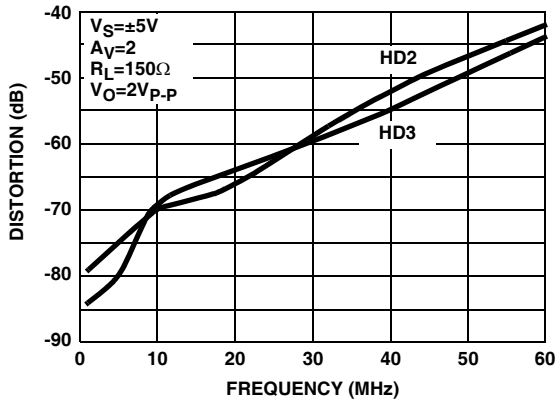


FIGURE 13. DISTORTION vs FREQUENCY

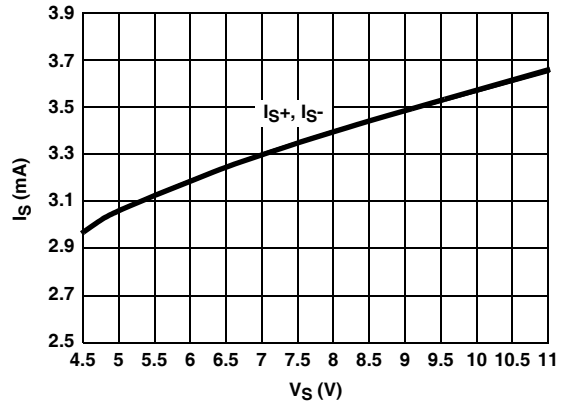


FIGURE 14. SUPPLY CURRENT vs SUPPLY VOLTAGE

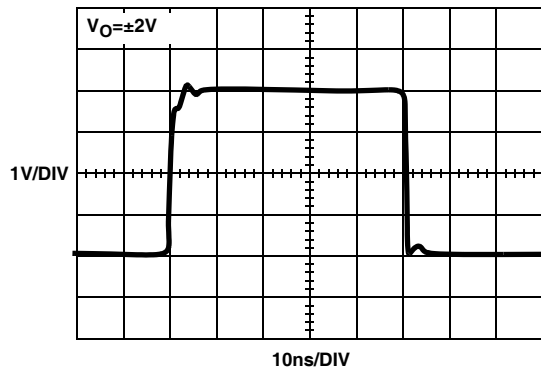


FIGURE 15. LARGE SIGNAL RESPONSE

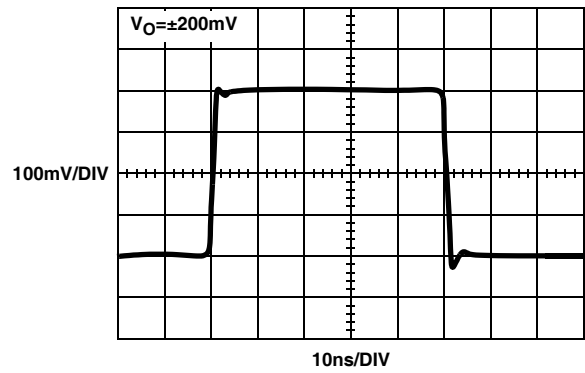


FIGURE 16. SMALL SIGNAL RESPONSE

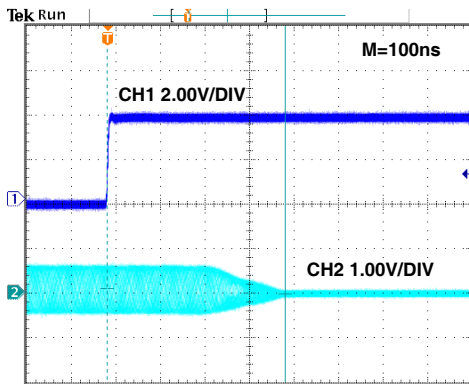


FIGURE 17. DISABLED RESPONSE

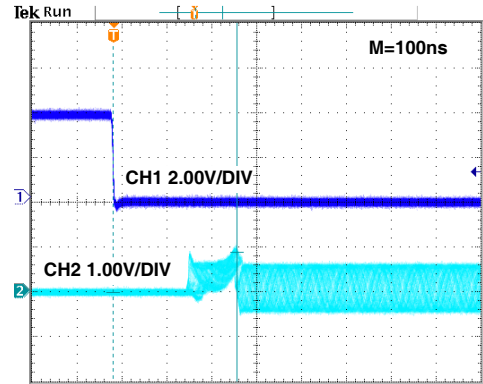


FIGURE 18. ENABLED RESPONSE

Typical Performance Curves (Continued)

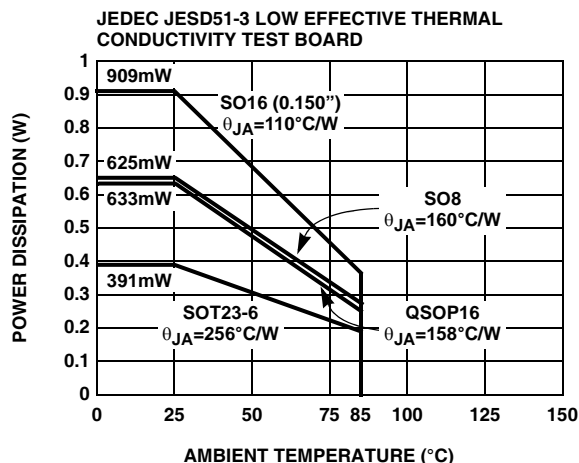


FIGURE 19. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

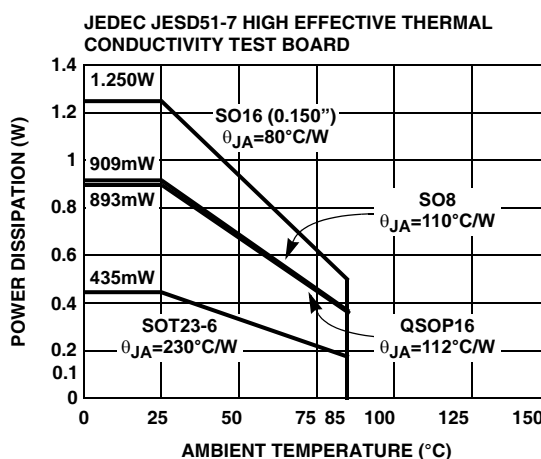


FIGURE 20. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

Product Description

The EL5108 and EL5308 are fixed gain amplifiers that offer a wide -3dB bandwidth of 450MHz and a low supply current of 3.5mA per amplifier. They work with supply voltages ranging from a single 5V to 10V and they are also capable of swinging to within 1.2V of either supply on the output. These combinations of high bandwidth, low power, and high slew rate make the EL5108 and EL5308 the ideal choice for many low-power/high-bandwidth applications such as portable, handheld, or battery-powered equipment.

For varying bandwidth and higher gains, consider the EL5166 with 1GHz on a 9mA supply current or the EL5164 with 600MHz on a 3.5mA supply current. Versions include single, dual, and triple amp packages with 6 Ld SOT-23, 16 Ld QSOP, and 8 Ld or 16 Ld SO outlines.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Low impedance ground plane construction is essential. Surface mount components are recommended, but if leaded components are used, lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. The combination of a 4.7µF tantalum capacitor in parallel with a 0.01µF capacitor has been shown to work well when placed at each supply pin.

Disable/Power-Down

The EL5108 and EL5308 amplifiers can be disabled and placing their outputs in a high impedance state. When disabled, the amplifier supply current is reduced to <25µA. The EL5108 and EL5308 are disabled when the \overline{CE} pin is pulled up to within 1V of the positive supply. Similarly, the amplifier is enabled by floating or pulling its \overline{CE} pin to at least 3V below the positive supply. For ±5V supply, this means that the amplifier will be enabled when \overline{CE} is 2V or less, and disabled when \overline{CE} is above 4V. Although the logic levels are not standard TTL, this choice of logic voltages allow the EL5108 and EL5308 to be enabled by tying \overline{CE} to ground, even in 5V single supply applications. The \overline{CE} pins can be driven from CMOS outputs.

Gain Setting

The EL5108 and EL5308 are built with internal feedback and gain resistors. The internal feedback resistors have equal value; as a result, the amplifier can be configured into gain of +1, -1, and +2 without any external resistors. Figure 21 shows the amplifier in gain of +2 configuration. The gain error is ±2% maximum. Figure 22 shows the amplifier in gain of -1 configuration. For gain of +1, IN+ and IN- should be connected together as shown in Figure 23. This configuration avoids the effects of any parasitic capacitance on the IN- pin. Since the internal feedback and gain resistors change with temperature and process, external resistor should not be used to adjust the gain settings.

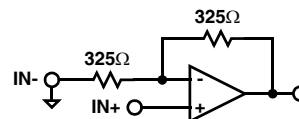


FIGURE 21. $A_v = +2$

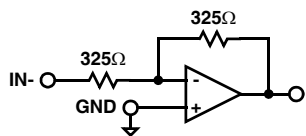


FIGURE 22. $A_V = -1$

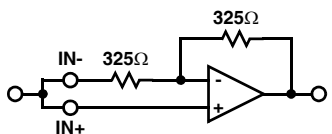


FIGURE 23. $A_V = +1$

Supply Voltage Range and Single-Supply Operation

The EL5108 and EL5308 have been designed to operate with supply voltages having a span of greater than or equal to 5V and less than 12V. In practical terms, this means that they will operate on dual supplies ranging from $\pm 2.5V$ to $\pm 5V$. With single-supply, they will operate from 5V to 10V.

As supply voltages continue to decrease, it becomes necessary to provide input and output voltage ranges that can get as close as possible to the supply voltages. The EL5108 and EL5308 have an input range which extends to within 2V of either supply. So, for example, on $\pm 5V$ supplies, the input range is about $\pm 3V$. The output range is also quite large, extending to within 1V of the supply rail. On a $\pm 5V$ supply, the output is therefore capable of swinging from -4V to +4V. Single-supply output range is larger because of the increased negative swing due to the external pull-down resistor to ground. Figure 24 shows an AC-coupled, gain of +2, +5V single supply circuit configuration.

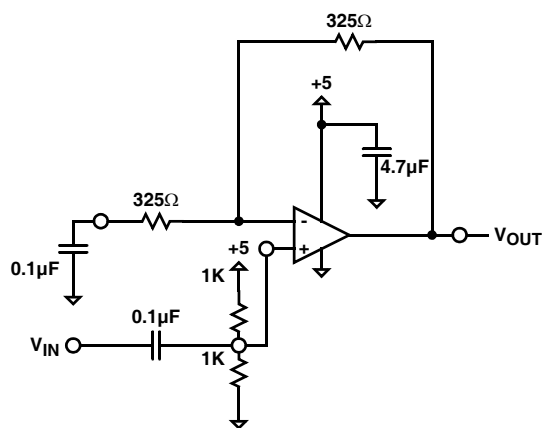


FIGURE 24.

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω , because of the change in output current with DC level. Previously, good differential gain could only be achieved by running high idle currents through the output transistors (to reduce variations in output impedance). Special circuitry has been incorporated in the EL5108 and EL5308 to reduce the variation of output impedance with current output. This results in dG and dP specifications of 0.01% and 0.01° , while driving 150Ω at a gain of 2.

Output Drive Capability

In spite of its low 3.5mA of supply current per amplifier, the EL5108 and EL5308 are capable of providing a maximum of $\pm 130mA$ of output current.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back-termination series resistor will decouple the EL5108 and EL5308 from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. In these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output to eliminate most peaking.

Current Limiting

The EL5108 and EL5308 have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

With the high output drive capability of the EL5108 and EL5308, it is possible to exceed the $125^\circ C$ Absolute Maximum junction temperature under certain very high load current conditions. Generally speaking when R_L falls below about 25Ω , it is important to calculate the maximum junction temperature (T_{JMAX}) for the application to determine if power supply voltages, load conditions, or package type need to be modified for the EL5108 and EL5308 to remain in the safe operating area. These parameters are calculated as follows:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} \times n \times PD_{MAX})$$

where:

T_{MAX} = Maximum ambient temperature

θ_{JA} = Thermal resistance of the package

n = Number of amplifiers in the package

PD_{MAX} = Maximum power dissipation of each amplifier in the package

PD_{MAX} for each amplifier can be calculated as follows:

$$PD_{MAX} = (2 \times V_S \times I_{SMAX}) + \left[(V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \right]$$

where:

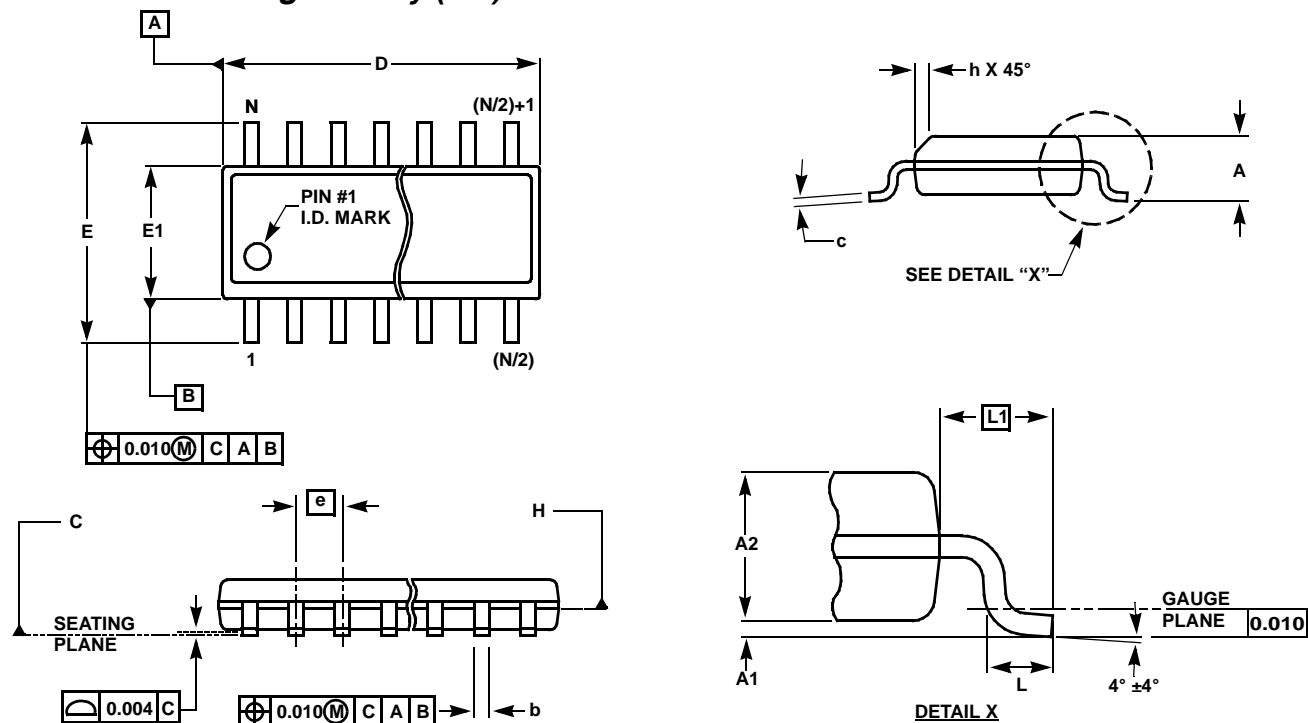
V_S = Supply voltage

I_{SMAX} = Maximum supply current of 1A

V_{OUTMAX} = Maximum output voltage (required)

R_L = Load resistance

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

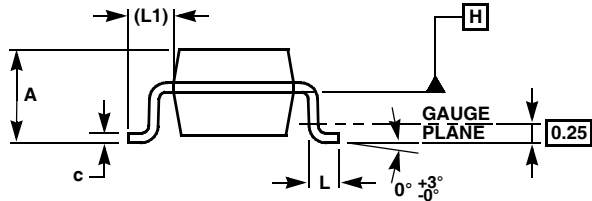
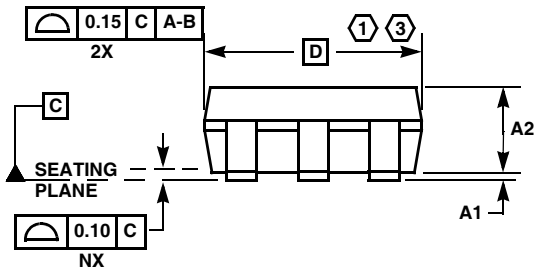
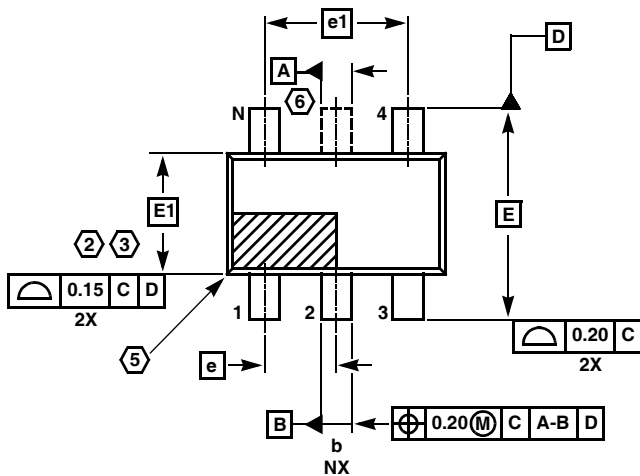
SYMBOL	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	TOLERANCE	NOTES
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. L 2/01

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

SOT-23 Package Family



MDP0038

SOT-23 PACKAGE FAMILY

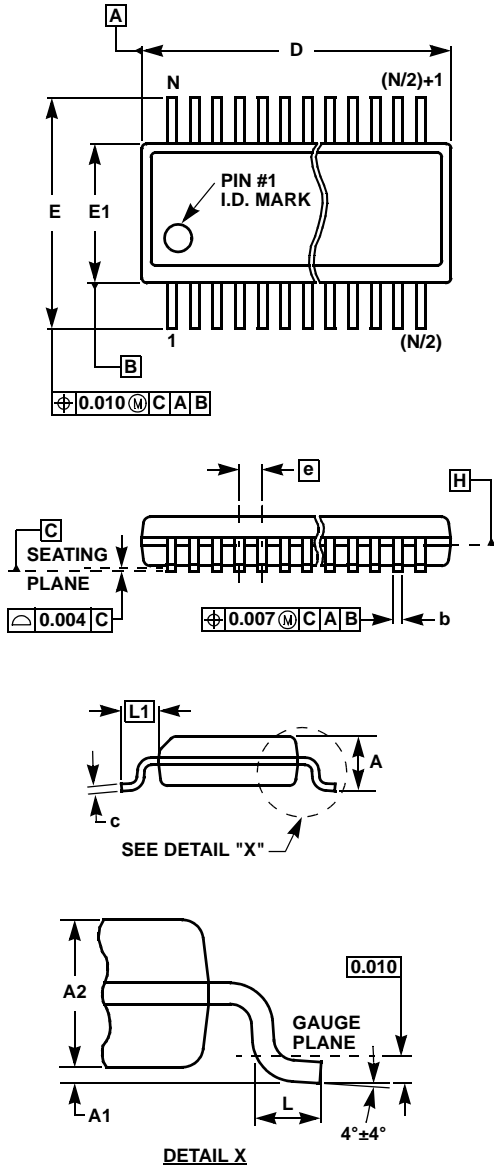
SYMBOL	SOT23-5	SOT23-6	TOLERANCE
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. E 3/00

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

Quarter Size Outline Plastic Packages Family (QSOP)



MDP0040

QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY

SYMBOL	QSOP16	QSOP24	QSOP28	TOLERANCE	NOTES
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	±0.002	-
A2	0.056	0.056	0.056	±0.004	-
b	0.010	0.010	0.010	±0.002	-
c	0.008	0.008	0.008	±0.001	-
D	0.193	0.341	0.390	±0.004	1, 3
E	0.236	0.236	0.236	±0.008	-
E1	0.154	0.154	0.154	±0.004	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	±0.009	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

Rev. E 3/01

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com