# dsPIC33FJXXXGPXXX/ dsPIC33FJXXXMCXXX

# dsPIC33F Rev. A2 Silicon Errata

## dsPIC33FJXXXGPXXX, dsPIC33FJXXXMCXXX (Rev. A2) Silicon Errata

The dsPIC33F devices (Rev. A2) you received were found to conform to the specifications and functionality described in the following documents:

- DS70165 – "*dsPIC33F Family Data Sheet*"
- DS70157 – "*dsPIC30F/33F Programmer's Reference Manual*"
- DS70046 – *"dsPIC30F Family Reference Manual"*

The exceptions to the specifications in the documents listed above are described in this section. The specific devices for which these exceptions are described are listed below:

- dsPIC33FJ64GP206
- dsPIC33FJ64GP306
- dsPIC33FJ64GP310
- dsPIC33FJ64GP706
- dsPIC33FJ64GP708
- dsPIC33FJ64GP710
- dsPIC33FJ128GP206
- dsPIC33FJ128GP306
- dsPIC33FJ128GP310
- dsPIC33FJ128GP706
- dsPIC33FJ128GP708
- dsPIC33FJ128GP710
- dsPIC33FJ256GP506
- dsPIC33FJ256GP510
- dsPIC33FJ256GP710
- dsPIC33FJ64MC506
- dsPIC33FJ64MC508
- dsPIC33FJ64MC510
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- dsPIC33FJ64MC710
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- dsPIC33FJ128MC706
- dsPIC33FJ128MC708
- dsPIC33FJ128MC710
- dsPIC33FJ256MC510
- dsPIC33FJ256MC710

dsPIC33F Rev. A2 silicon is identified by performing a "Reset and Connect" operation to the device using MPLAB® ICD 2 with MPLAB IDE v7.40 or later. The output window will show a successful connection to the device specified in *Configure>Select Device*.

The errata described in this section will be addressed in future revisions of silicon.

### Silicon Errata Summary

The following list summarizes the errata described in further detail through the remainder of this document:

1. Doze Mode

   When Doze mode is enabled, any writes to a peripheral SFR can cause other updates to that register to cease to function for the duration of the current CPU clock cycle.

2. 12-bit Analog-to-Digital Converter (ADC) Module

   For this revision of silicon, the 12-bit ADC module INL, DNL and signal acquisition time parameters are not within the published data sheet specifications.

3. 10-bit ADC Module

   For this revision of silicon, the 10-bit ADC module DNL, conversion speed and signal acquisition time parameters are not within the published data sheet specifications.

4. DMA Module: Interaction with `EXCH` Instruction

   The `EXCH` instruction does not execute correctly when one of the operands contains a value equal to the address of the DMAC SFRs.

5. `DISI` Instruction

   The `DISI` instruction will not disable interrupts if a `DISI` instruction is executed in the same instruction cycle that the `DISI` counter decrements to zero.

6. Motor Control PWM

   There is a glitch in the PWMxL signal in Single-Shot mode with complementary output. Another glitch occurs when resuming from a Fault condition in Free-Running mode with complementary output.

7. Output Compare Module

   The output compare module will produce a glitch on the output when an I/O pin is initially set high and the module is configured to drive the pin low at a specified time.

8. Output Compare Module in PWM Mode

   The output compare module will miss one compare event when the duty cycle register value is updated from 0x0000 to 0x0001.

9. SPI Module in Frame Master Mode

   The SPI module will fail to generate frame synchronization pulses in Frame Master mode.

10. SPI Module in Slave Select Mode

    The SPI module Slave Select functionality will not work correctly.

11. SPI Module

    The SMP bit does not have any effect when the SPI module is configured for a 1:1 prescale factor in Master mode.

12. ECAN™ Module

    ECAN transmissions may be incorrect if multiple transmit buffers are simultaneously queued for transmission.

13. ECAN Module

    Under specific conditions, the first five bits of a transmitted identifier may not match the value in the transmit buffer ID register.

14. ECAN Module Loopback Mode

    The ECAN module (ECAN1 or ECAN2) does not function correctly in Loopback mode.

15. $I^2C$™ Module

    The bus collision status bit does not get set when a bus collision occurs during a Restart or Stop event.

16. INT0, ADC and Sleep/Idle Mode

    ADC event triggers from the INT0 pin will not wake-up the device from Sleep or Idle mode if the SMPI bits are non-zero.

17. Doze Mode and Traps

    The address error trap, stack error trap, math error trap and DMA error trap will not wake-up a device from Doze mode.

18. JTAG Programming

    JTAG programming does not work.

The following sections will describe the errata and work around to these errata, where they may apply.

## 1. Module: Oscillator: Doze Mode

Enabling Doze mode slows down the CPU but allows peripherals to run at full speed. When the CPU clock is slowed down by enabling Doze mode (CLKDIV<11> = 1), any writes to a peripheral SFR can cause other updates to that register to cease to function for the duration of the current CPU clock cycle. This is only an issue if the CPU attempts to write to the same register as a peripheral while in Doze mode.

For instance, if the ADC module is active and Doze mode is enabled, the main program should avoid writing to ADCCONx registers because these registers are being used by the ADC module. If the CPU does make writes before the ADC module does, then any attempts by the ADC module to write to these registers will fail.

**Work around**

In Doze mode, avoid writing code that will modify SFRs which may be written to by enabled peripherals.

## 2. Module: 12-bit ADC

When the ADC module is configured for 12-bit operation, the specifications in the data sheets are not met.

**Work around**

Implement the ADC module as an 11-bit ADC with a maximum conversion rate of 300 Ksps.

1. The specifications provided below reflect 11-bit ADC operation. RIN source impedance is recommended as 200 ohms and sample time is recommended as 3 TAD to ensure compatibility on future enhanced ADC modules. Missing codes are possible every $2^7$ codes.
2. When used as a 10-bit ADC, the INL is <±2 LSBs, and DNL is <±1 LSB with no missing codes. Maximum conversion rate is 300 Ksps.

**TABLE 1: ADC PERFORMANCE (11-BIT OPERATION)**

| Param No. | Symbol | Min | Typical | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| AD17 | RIN | — | — | 200 | Ohm | 12-bit |
| **ADC Accuracy – Measurements taken with External VREF+/VREF-** | | | | | | |
| AD20a | Nr | — | 12 bits | — | Bits | |
| AD21a | INL | -2 | — | 2 | LSB | |
| AD22a | DNL | -1.5 | — | 1 | LSB | |
| AD23a | GERR | 1 | 5 | 10 | LSB | |
| AD24a | EOFF | 1 | 3 | 6 | LSB | |
| **ADC Accuracy – Measurements taken with Internal VREF+/VREF-** | | | | | | |
| AD21aa | INL | -2 | — | 2 | LSB | |
| AD22aa | DNL | -1.5 | — | 1 | LSB | |
| AD23aa | GERR | 5 | 10 | 20 | LSB | |
| AD24aa | EOFF | 3 | 6 | 15 | LSB | |
| **Dynamic Performance** | | | | | | |
| AD33a | FNYQ | — | — | 150 | KHz | |
| AD34a | ENOB | 9.5 | 9.6 | 10.4 | Bits | |
| **ADC Conversion Rate** | | | | | | |
| AD56a | FCNV | — | — | 300 | Ksps | |
| AD57a | TSAMP | — | 3 TAD | — | — | |

### 3. Module: 10-bit ADC

When the ADC module is configured for 10-bit operation, the specifications in the data sheet are not met for operation above 500 Ksps.

For 500 Ksps, the module meets specifications except for Gain and Offset parameters AD23bb and AD24bb.

For 600 Ksps operation, the module specifications are shown in Table 2.

**Work around**

None. Future versions of the silicon will support the ADC performance stated in the data sheet.

**TABLE 2: 600 KSPS OPERATION**

| Param No. | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| AD17 | RIN | — | — | 200 | Ohm | 10-bit |
| **ADC Accuracy – Measurements taken with External VREF+/VREF-** | | | | | | |
| AD20b | Nr | — | 10 bits | — | Bits | |
| AD21b | INL | -2 | — | 2 | LSB | |
| AD22b | DNL | -1.5 | — | 2 | LSB | |
| AD23b | GERR | 1 | 3 | 6 | LSB | |
| AD24b | EOFF | 1 | 2 | 5 | LSB | |
| **ADC Accuracy – Measurements taken with Internal VREF+/VREF-** | | | | | | |
| AD21bb | INL | -2 | — | 2 | LSB | |
| AD22bb | DNL | -1.5 | — | 2 | LSB | |
| AD23bb | GERR | 1 | 6 | 12 | LSB | |
| AD24bb | EOFF | 2 | 5 | 10 | LSB | |
| **Dynamic Performance** | | | | | | |
| AD33b | FNYQ | — | — | 300 | KHz | |
| AD34b | ENOB | 8.5 | 9.7 | 9.8 | Bits | |
| **ADC Conversion Rate** | | | | | | |
| AD56b | FCNV | — | — | 600 | Ksps | |
| AD57b | TSAMP | — | 3 TAD | — | — | |

### 4. Module: DMA Module: Interaction with EXCH Instruction

The EXCH instruction does not execute correctly when either of the two operands is numerically equal to the address of any of the DMAC SFRs for this revision of silicon.

**Work around**

If writing source code in assembly, the recommended fix is to replace:

```
EXCH Wsource, Wdestination
```

with:

```
PUSH Wdestination
MOV Wsource, Wdestination
POP Wsource
```

If using the MPLAB C30 C compiler, check the disassembly listing (*View>Disassembly Listing*) for the EXCH instruction. If used, make sure the operands are not equivalent to the DMA SFRs' addresses.

### 5. Module: DISI Instruction

When a user executes a DISI #7, for example, this will disable interrupts for 7 + 1 cycles (7 + the DISI instruction itself). In this case, the DISI instruction uses a counter which counts down from 7 to 0. The counter is loaded with 7 at the end of the DISI instruction.

If the user code executes another DISI on the instruction cycle where the DISI counter has become zero, the new DISI count is loaded, but the DISI state machine does not properly re-engage and continue to disable interrupts. At this point, all interrupts are enabled. The next time the user code executes a DISI instruction, the feature will act normally and block interrupts.

In summary, it is only when a DISI execution is coincident with the current DISI count = 0, that the issue occurs. Executing a DISI instruction before the DISI counter reaches zero will not produce this error. In this case, the DISI counter is loaded with the new value, and interrupts remain disabled until the counter becomes zero.

**Work around**

When executing multiple DISI instructions within the source code, make sure that subsequent DISI instructions have at least one instruction cycle between the time that the DISI counter decrements to zero and the next DISI instruction. Alternatively, make sure that subsequent DISI instructions are called before the DISI counter decrements to zero.

### 6. Module: Motor Control PWM

Devices in the motor control family have a glitch in the PWMxL signal under certain conditions. The glitch is a brief high pulse during the low portion of the duty cycle. This error occurs when the module is configured in Single-Shot mode (PTMOD<1:0> = 01) with complementary output. It also occurs when resuming from a Fault condition in Free-Running mode (PTMOD<1:0) = 00) with complementary output.

**Work around**

None.

### 7. Module: Output Compare Module

A glitch will be produced on an output compare pin under the following conditions:

- The user software initially drives the I/O pin high using the output compare module or a write to the associated PORT register.
- The output compare module is configured and enabled to drive the pin low at some later time (OCxCON = 0x0002 or OCxCON = 0x0003).

When these events occur, the output compare module will drive the pin low for one instruction cycle (TCY) after the module is enabled.

**Work around**

None. However, the user may use a timer interrupt and write to the associated PORT register to control the pin manually.

### 8. Module: Output Compare Module in PWM Mode

The output compare module will miss a compare event when the current duty cycle register (OCxRS) value is 0x0000 (0% duty cycle) and the OCxRS register is updated with a value of 0x0001. The compare event is missed only the first time a value of 0x0001 is written to OCxRS, and the PWM output remains low for one PWM period. Subsequent PWM high and low times occur as expected.

**Work around**

None. If the current OCxRS register value is 0x0000, avoid writing a value of 0x0001 to OCxRS. Instead, write a value of 0x0002; however, in this case the duty cycle will be slightly different from the desired value.

### 9. Module: SPI Module in Frame Master Mode

The SPI module will fail to generate frame synchronization pulses when configured in the Frame Master mode (FRMEN = 1, SPIFSD = 0). However, the module functions correctly in Frame Slave mode.

**Work around**

If DMA is not being used, manually drive the $\overline{SSx}$ pin (x = 1 or 2) high using the associated PORT register, and then drive it low after the required 1 bit-time pulse width. This operation needs to be performed when the transmit buffer is written.

If DMA is being used, and if no other peripheral modules are using DMA transfers, use a timer interrupt to periodically generate the frame synchronization pulse (using the method described above) after every 8 or 16 bit periods (depending on the data word size, configured using the MODE16 bit).

### 10. Module: SPI Module in Slave Select Mode

The SPI module Slave Select functionality (enabled by setting SSEN = 1) will not function correctly. Whether the $\overline{SSx}$ pin (x = 1 or 2) is high or low, the SPI data transfer will be completed and an interrupt will be generated.

**Work around**

If DMA is not being used, manually poll the $\overline{SSx}$ pin state in the SPI interrupt by reading the associated LAT bit:

- If the LAT bit is '0', then perform the required data read/write.
- If the LAT bit is '1', then clear the SPI interrupt flag (SPIxIF), perform a dummy read of the SPIxBUF register, and return from the Interrupt Service Routine.

If DMA is being used, there is no work around.

### 11. Module: SPI Module

The SMP bit (SPIxCON1<9>, where x = 1 or 2) does not have any effect when the SPI module is configured for a 1:1 prescale factor in Master mode. In this mode, whether the SMP bit is set or cleared, the data is always sampled at the end of data output time.

**Work around**

If sampling at the middle of data output time is required, then configure the SPI module to use a clock prescale factor other than 1:1 using the PPRE<1:0> and SPRE<2:0> bits in the SPIxCON1 register.

### 12. Module: ECAN Module

If multiple ECAN transmit buffers are queued for transmission (multiple TXREQ bits are set to '1' simultaneously), then the message transmissions from the enabled buffers may interfere with one another. As a result, incorrect ID and data transmissions will occur intermittently.

**Work around**

Enable only one transmit buffer for transmission at any given time. In the user application, this can be ensured by checking that all other TXREQn bits are clear before setting the TXREQn bit corresponding to the buffer that is to be transmitted.

### 13. Module: ECAN Module

Under specific conditions, the first five bits of a transmitted identifier may not match the value in the transmit buffer SID. If the ECAN module detects a Start-of-Frame (SOF) in the third bit of interframe space and if a message to be transmitted is pending, the first five bits of the transmitted identifier may be corrupted.

**Work around**

None.

### 14. Module: ECAN Module Loopback Mode

The ECAN module (ECAN1 or ECAN2) does not function correctly in Loopback mode.

**Work around**

Do not use Loopback mode.

### 15. Module: $I^2C$ Module

The Bus Collision Status bit (BCL) does not get set when a bus collision occurs during a Restart or Stop event. However, the BCL bit gets set when a bus collision occurs during a Start event.

**Work around**

None.

### 16. Module: INT0, ADC and Sleep/Idle Mode

ADC event triggers from the INT0 pin will not wake-up the device from Sleep or Idle mode if the SMPI bits are non-zero. This means that if the ADC is configured to generate an interrupt after a certain number of INT0 triggered conversions, the ADC conversions will not be triggered and the device will remain in Sleep. The ADC will perform conversions and wake-up the device only if it is configured to generate an interrupt after each INT0 triggered conversion (SMPI<3:0> = 0000).

**Work around**

None. If ADC event trigger from the INT0 pin is required, initialize SMPI<3:0> to '0000' (interrupt on every conversion).

### 17. Module: Doze Mode and Traps

The address error trap, stack error trap, math error trap and DMA error trap will not wake-up a device from Doze mode.

**Work around**

None.

### 18. Module: JTAG Programming

JTAG programming does not work.

**Work around**

None.

## APPENDIX A: REVISION HISTORY

Revision A (6/2006)

- Initial release of the document.

Revision B (12/2006)

- Added errata 7, 8, 9, 10, 11, 12, 13, 14, 15, 16 and 17.

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