Design Idea DI-67

TOPSwitch®-GX Isolated, Power Factor Corrected (PFC), 17 W LED Driver

Application	Device	Power Output	Input Voltage	Output Current	Topology
LED Arrays	TOP246F	17.6 W max	108-132 VAC 60 Hz	700 mA (16-24 V)	Flyback

Design Highlights

- 700 mA of output current regulated to within ± 5%
- Power factor: > 0.98, THD: ≤ 9.6%
- No output current overshoot at power-on
- Temperature range: -40 °C to +80 °C
- Harmonics comply with IEC61000-3-2, Edition 2.1
- Conducted EMI complies with CISPR-22 B

Operation

This low-cost, TOP246F based PFC LED Driver takes advantage of built-in *TOPSwitch-GX* features. This supply is current (not voltage) regulated, except in the case of no-load. Without a load, the output voltage is limited to about 30 V (max), by R6 and VR2. Configured as a flyback converter, this circuit operates in the discontinuous conduction mode. It can deliver an average of 700 mA (1 A at the peak of output ripple) over a 16 V to 24 V range, which makes it ideal for driving high current LED arrays, such as the Luxeon 12 UP LED Ring.

The DC input capacitor (C3, 100 nF) was sized so that its voltage approaches zero at the AC input zero crossings (see the middle waveform of Figure 2).

A 220 µF capacitor (C6) was chosen for the bias supply to minimize the 120 Hz ripple current into the current source (Q1), which provides control current to U1. The output rectifier (D9) must be rated for an average of 3.5 A. Capacitor C7's value (680 µF) sets the magnitude of the output ripple current to 600 mA peak to peak, at 120 Hz.

Resistors R7, R8, R9 and U2's LED set the 700 mA average current limit. The U2 phototransistor drives the current source (Q1) and the PFC-loop filter capacitor (C8, 100 µF). Capacitor C8 was sized to provide the low loop bandwidth necessary for high power-factor. R4 is the power-off discharge path for C6 and C8.

The CONTROL pin bypass capacitor (C5, 1 µF) is just large enough to allow smooth start-up of the output load current, and yet small enough to prevent output current overshoot. A larger value of C5 would increase start-up delay time.

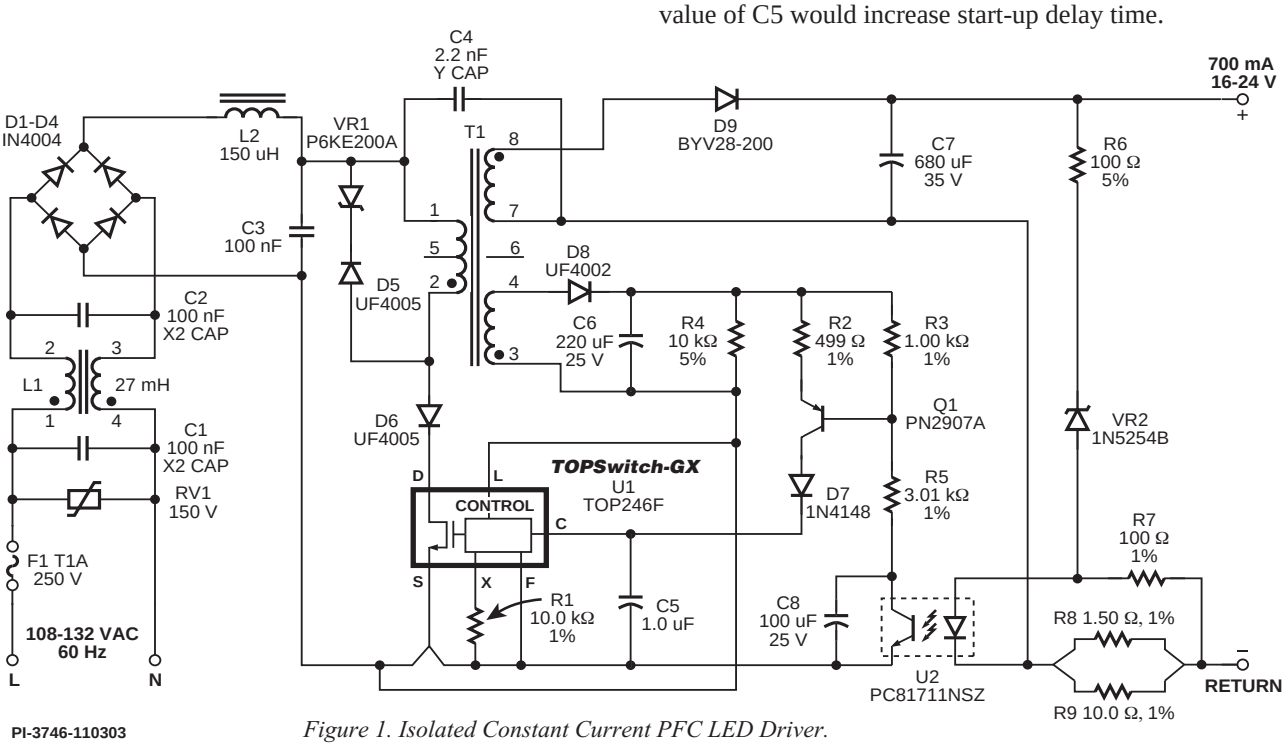

Figure 1. Isolated Constant Current PFC LED Driver.

Key Design Points

- To have high power factor, a constant duty factor must be maintained over the 8.33 ms half cycle period. Therefore, the bias supply voltage and the U1 CONTROL pin current must remain extremely constant. The values of C6 and C8 must be chosen accordingly.
- Decreasing the value of C8 will reduce the turn-on delay time, but will also degrade the power factor.
- Because low-cost is the goal of this low-loop-gain design, the tolerance of the output current depends on the CTR of the opto-coupler and the (unregulated) value of the bias voltage. The restricted AC input voltage range allows using the forward (not flyback) configuration for the bias winding. If the AC input voltage range is extended, voltage regulation of the bias supply circuit will be required.

TRANSFORMER PARAMETERS	
Core	EF-20 or Equivalent A_{LG} of 1570 nH/T^2
Bobbin	Miles-Platts EF0700 EF20 8 Pin Horizontal
Winding Details	Primary: 70T, 2 layers, 29 AWG Secondary: 13T, 2 x 32 AWG Triple Insulated Wire Bias: 9T, 2 x 23 AWG
Winding Order (pin numbers)	Primary: 2-5, tape Secondary: 8-7, tape Primary: 5-1, tape Bias: 3-4, tape 3 layers
Primary Inductance	350 µH ±10%
Primary Resonant Frequency	2.0 MHz (Min)
Leakage Inductance	10 µH (Max)

Table 1. Transformer Construction Information.

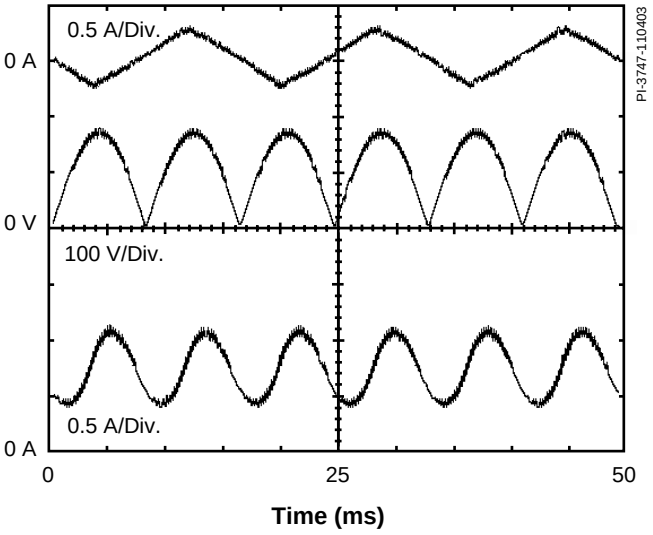

Figure 2. PFC LED Driver Waveforms.
Top: Input Current at 120 VAC 60 Hz.
Middle: C3 Capacitor Voltage.
Bottom: Output Current (with 20 V LED Load).

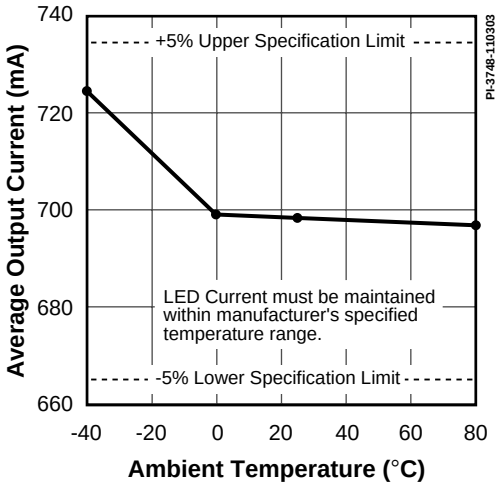

Figure 3. PFC Driver Current vs. Temperature.

Power Integrations **5245 Hellyer Avenue** **San Jose, California 95138**

MAIN PHONE NUMBER +1 408-414-9200
APPLICATIONS HOTLINE +1 408-414-9660
APPLICATIONS FAX +1 408-414-9760

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