



Low-Voltage, Low r_{ON} Quad SPST Analog Switch

FEATURES

- Low Voltage Operation (1.8 V to 5.5 V)
- Low On-Resistance - $r_{DS(on)}$: 1.0 Ω
- Fast Switching - 14 ns t_{ON}
- Low Charge Injection - Q_{INJ} : 1 pC
- Low Power Consumption
- TTL/CMOS Compatible
- TSSOP-16 and QFN-16 Packages

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

APPLICATIONS

- Cellular Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- Sample and Hold Circuits

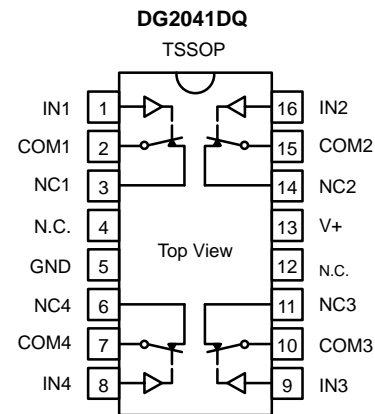
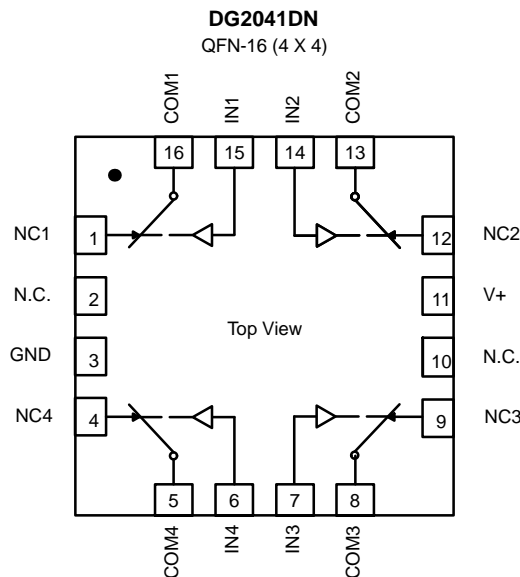
DESCRIPTION

The DG2041/2042/2043 are quad single-pole/single-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, fast switching, low on-resistance ($r_{DS(on)}$: 1.0 Ω @ 2.7 V) and small physical size, the DG2041/2042/2043 are ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG2041/2042/2043 are built on Vishay Siliconix's new high density low voltage process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION—DG2041

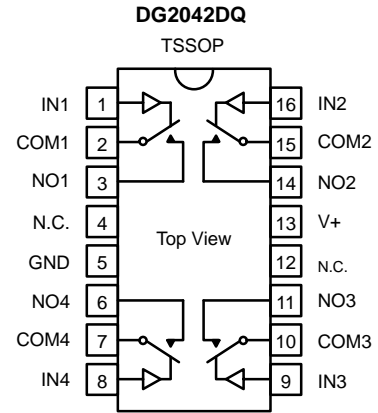
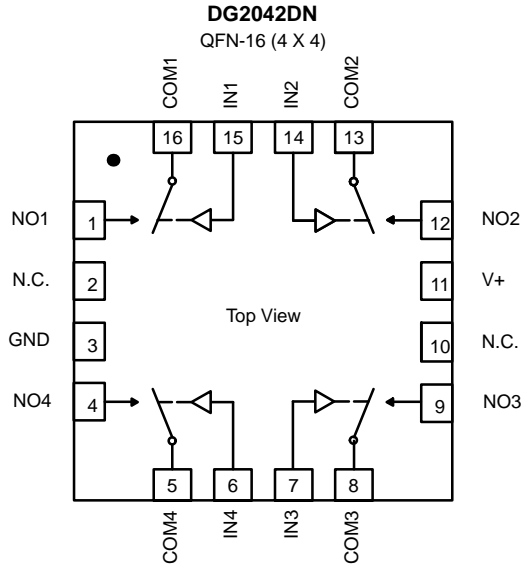


TRUTH TABLE DG2041	
Logic	Switch
0	On
1	Off

Switches Shown for Logic "0" Input



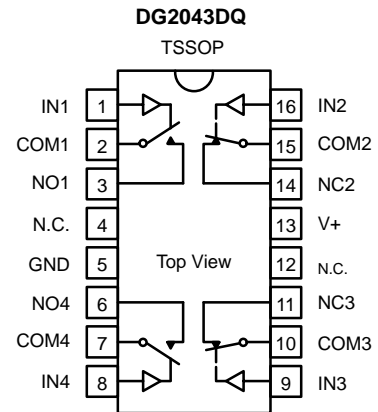
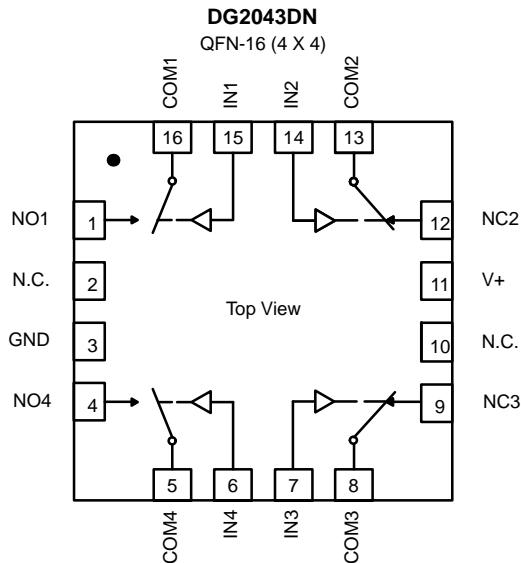
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION—DG2042



TRUTH TABLE DG2042	
Logic	Switch
0	Off
1	On

Switches Shown for Logic "0" Input

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION—DG2043



TRUTH TABLE DG2043		
Logic	Switches 1, 4	Switches 2, 3
0	Off	On
1	On	Off

Switches Shown for Logic "0" Input



ORDERING INFORMATION		
Temp Range	Package	Part Number
-40 to 85°C	TSSOP-16	DG2041DQ
		DG2042DQ
		DG2043DQ
	QFN-16 (4x4 mm)	DG2041DN
		DG2042DN
		DG2043DN

ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+	-0.3 to +6 V
IN, COM, NC, NO ^a	-0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal)	±50 mA
Peak Current (Pulsed at 1 ms, 10% duty cycle)	±200 mA
Storage Temperature (D Suffix)	-65 to 150°C
Power Dissipation (Packages) ^b	
TSSOP-16 ^c	450 mW
QFN-16 (4 x 4 mm) ^d	1880 mW

Notes:

- a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC Board.
- c. Derate 5.6 mW/°C above 70°C
- d. Derate 23.5 mW/°C above 70°C
- e. Manual soldering with soldering iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS (V+ = 2.0 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2.0 V, V _{IN} = 0.4 or 1.6 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0		V+	V
On-Resistance	r _{ON}	V+ = 2.0 V, V _{COM} = 0.2 V/1.2 V, I _{NO} , I _{NC} = 10 mA	Room Full ^d		3.0	6.3 6.3	Ω
r _{ON} Flatness ^d	r _{ON} Flatness	V+ = 2.0 V, V _{COM} = 0 to V+, I _{NO} , I _{NC} = 10 mA	Room			4.2	
r _{ON} Match Between Channels	Δ r _{ON}		Room			0.4	
Switch Off Leakage Current ^f	I _{NO(off)} , I _{NC(off)}	V+ = 2.2 V V _{NO} , V _{NC} = 0.2 V/2.0 V, V _{COM} = 2.0 V/0.2 V	Room Full ^d	-1 -10		1 10	nA
	I _{COM(off)}		Room Full ^d	-1 -10		1 10	
Channel-On Leakage Current ^f	I _{COM(on)}	V+ = 2.2 V, V _{NO} , V _{NC} = V _{COM} = 0.2 V/2.0 V	Room Full ^d	-1 -10		1 10	
Digital Control							
Input High Voltage	V _{INH}		Full	1.6			V
Input Low Voltage	V _{INL}		Full			0.4	
Input Capacitance ^d	C _{in}		Full		4		pF
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	-1		1	μA



SPECIFICATIONS (V+ = 2.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2.0 V, VIN = 0.4 or 1.6 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _{NO} or V _{NC} = 1.5 V, R _L = 300 Ω, C _L = 35 pF Figures 1 and 2	Room Full ^d		30	81 82	ns
Turn-Off Time	t _{OFF}		Room Full ^d		22	41 42	
Break-Before-Make Time Delay	t _D	V _{NO} or V _{NC} = 1.5 V, R _L = 300 Ω, C _L = 35 pF (DG2043 Only)	Room	5			
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω, Figure 2	Room		1		pC
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		-63		dB
Crosstalk ^d	X _{TALK}		Room		-95		
NO, NC Off Capacitance ^d	C _{NO(off)} , C _{NC(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room		24		pF
Channel-On Capacitance ^d	C _{ON}		Room		48		
Power Supply							
Power Supply Current ^d	I+	V _{IN} = 0 or V+			0.001	1.0	μA

SPECIFICATIONS (V+ = 3.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, VIN = 0.4 or 2.0 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0		V+	V
On-Resistance	r _{ON}	V+ = 2.7 V, V _{COM} = 0.7 V/1.5 V, I _{NO} , I _{NC} = 10 mA	Room Full		1.6	2.1 2.2	Ω
r _{ON} Flatness ^d	r _{ON} Flatness	V+ = 2.7 V, V _{COM} = 0 to V+, I _{NO} , I _{NC} = 10 mA	Room			0.7	
r _{ON} Match Between Channels	Δ r _{ON}		Room			0.3	
Switch Off Leakage Current ^f	I _{NO(off)} , I _{NC(off)}	V+ = 3.3 V V _{NO} , V _{NC} = 0.3 V/3.0 V, V _{COM} = 3.0 V/0.3 V	Room Full	-1 -10		1 10	nA
	I _{COM(off)}		Room Full	-1 -10		1 10	
Channel-On Leakage Current ^f	I _{COM(on)}	V+ = 3.3 V, V _{NO} , V _{NC} = V _{COM} = 0.3 V/3.0 V	Room Full	-1 -10		1 10	
Digital Control							
Input High Voltage ^d	V _{INH}		Full	1.6			V
Input Low Voltage	V _{INL}		Full			0.4	
Input Capacitance ^d	C _{in}		Full		4		pF
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	-1		1	μA



SPECIFICATIONS (V+ = 3.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, VIN = 0.4 or 2.0 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Dynamic Characteristics							
Turn-On Time ^d	t _{ON}	V _{NO} or V _{NC} = 2.0 V, R _L = 300 Ω, C _L = 35 pF Figure 1 and 2	Room Full		19	51 52	ns
Turn-Off Time ^d	t _{OFF}		Room Full		17	36 37	
Break-Before-Make Time Delay	t _D	V _{NO} or V _{NC} = 2.0 V, R _L = 300 Ω, C _L = 35 pF (DG2043 Only)	Room	2			
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω, Figure 2	Room		3		pC
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		-63		dB
Crosstalk ^d	X _{TALK}		Room		-94		
NO, NC Off Capacitance ^d	C _{NO(off)} , C _{NC(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room		25		pF
Channel-On Capacitance ^d	C _{ON}		Room		49		
Power Supply							
Power Supply Current	I+	V _{IN} = 0 or V+			0.001	1.0	μA

SPECIFICATIONS (V+ = 5.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, VIN = 0.8 or 2.4 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0		V+	V
On-Resistance	r _{ON}	V+ = 4.5 V, V _{COM} = 0.7 V/2.5 V, I _{NO} , I _{NC} = 10 mA	Room Full		1.0	1.5 1.6	Ω
r _{ON} Flatness ^d	r _{ON} Flatness	V+ = 4.5 V, V _{COM} = 0 to V+, I _{NO} , I _{NC} = 10 mA	Room			0.7	
r _{ON} Match Between Channels	Δ r _{ON}		Room			0.3	
Switch Off Leakage Current	I _{NO(off)} , I _{NC(off)}	V+ = 5.5 V V _{NO} , V _{NC} = 1 V/4.5 V, V _{COM} = 4.5 V/1 V	Room Full	-1.0 -10		1.0 10	nA
	I _{COM(off)}		Room Full	-1.0 -10		1.0 10	
Channel-On Leakage Current	I _{COM(on)}	V+ = 5.5 V, V _{NO} , V _{NC} = V _{COM} = 1 V/4.5 V	Room Full	-1.0 -10		1.0 10	
Digital Control							
Input High Voltage	V _{INH}		Full	2.4			V
Input Low Voltage	V _{INL}		Full			0.8	
Input Capacitance	C _{in}		Full		4		pF
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	-1		1	μA



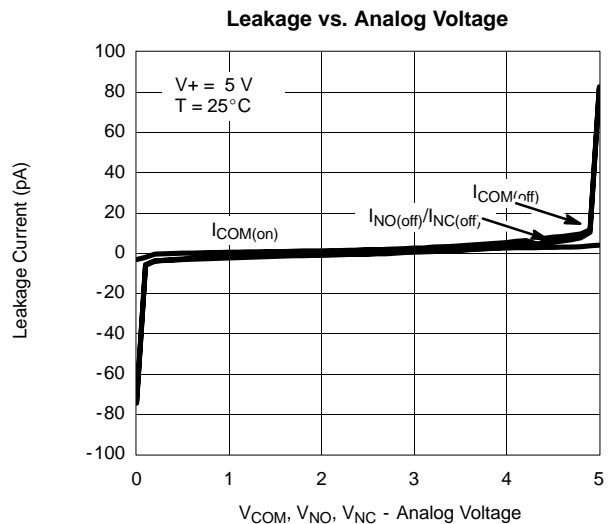
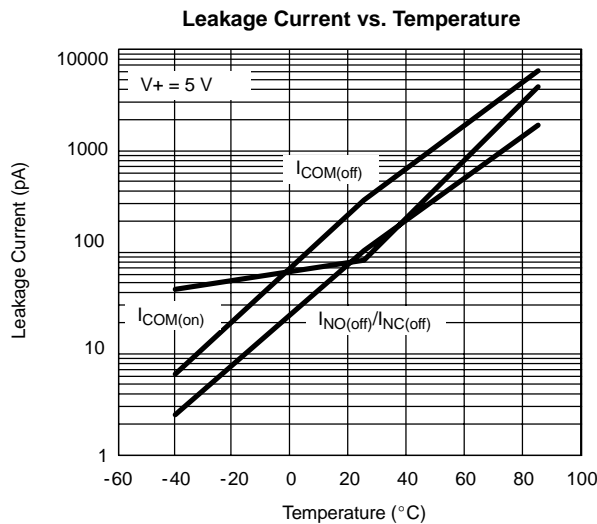
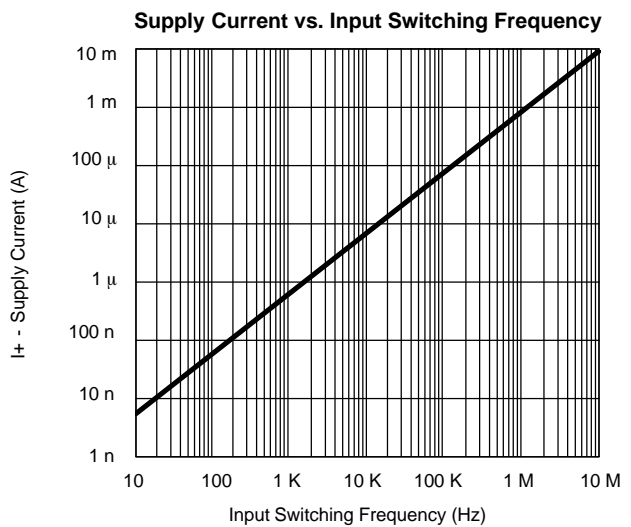
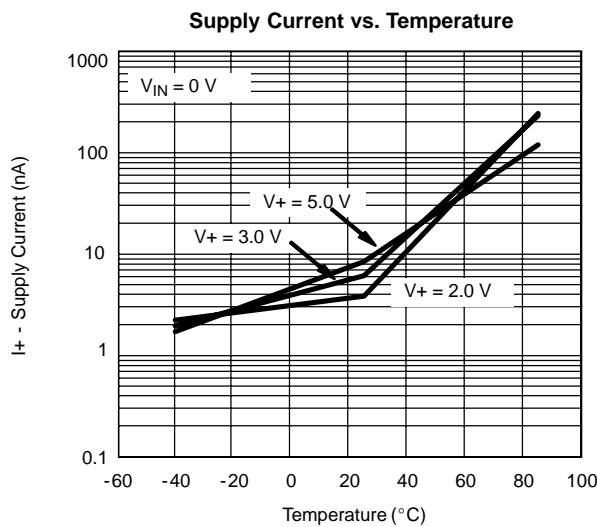
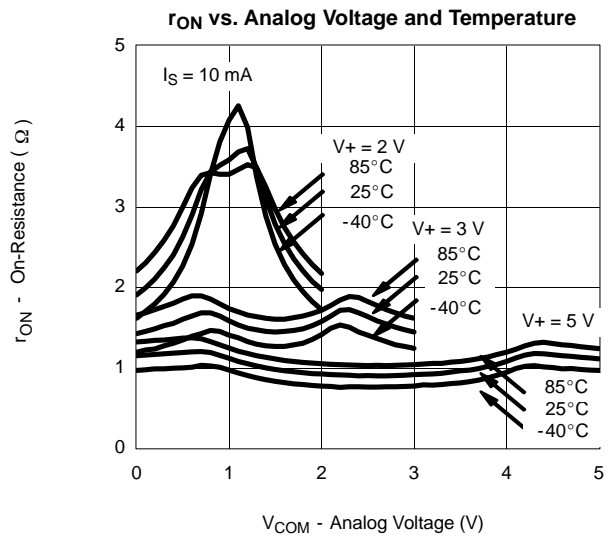
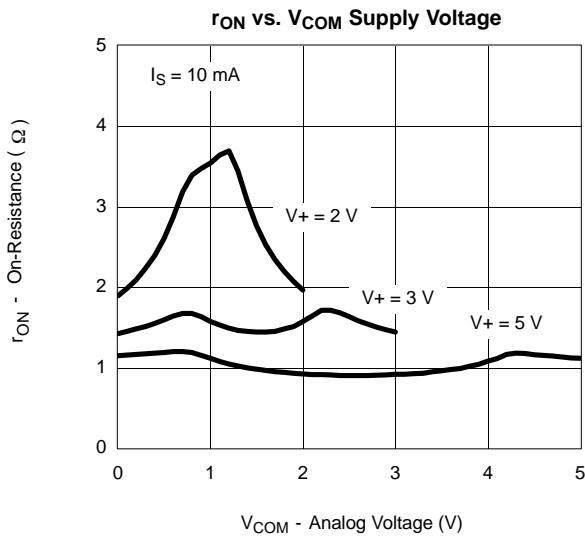
SPECIFICATIONS (V+ = 5.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, VIN = 0.8 or 2.4 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Dynamic Characteristics							
Turn-On Time ^d	t _{ON}	V _{NO} or V _{NC} = 3 V, R _L = 300 Ω, C _L = 35 pF Figure 1 and 2	Room Full		13 42 43	ns	
Turn-Off Time ^d	t _{OFF}		Room Full		19 32 33		
Break-Before-Make Time Delay	t _D	V _{NO} or V _{NC} = 3 V, R _L = 300 Ω, C _L = 35 pF (DG2043 Only)	Room	1			
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω, Figure 2	Room		3	pC	
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		-63	dB	
Crosstalk ^d	X _{TALK}		Room		-93		
Source-Off Capacitance ^d	C _{NO(off)} , C _{NC(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room		26	pF	
Channel-On Capacitance ^d	C _{ON}		Room		49		
Power Supply							
Power Supply Current	I+	V _{IN} = 0 or V+			0.001 1.0	μA	

Notes:

- a. Room = 25°C, Full = as determined by the operating suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for design aid only, not guaranteed nor subject to production testing.
- d. Guarantee by design, nor subjected to production test.
- e. V_{IN} = input voltage to perform proper function.
- f. Guaranteed by 5-V leakage testing, not production tested.



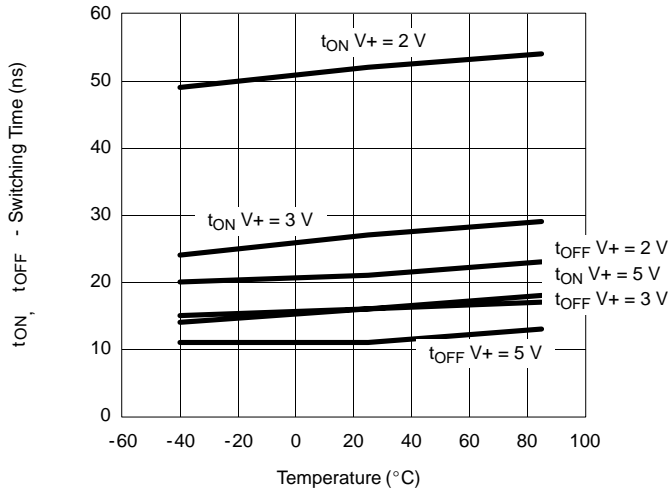
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



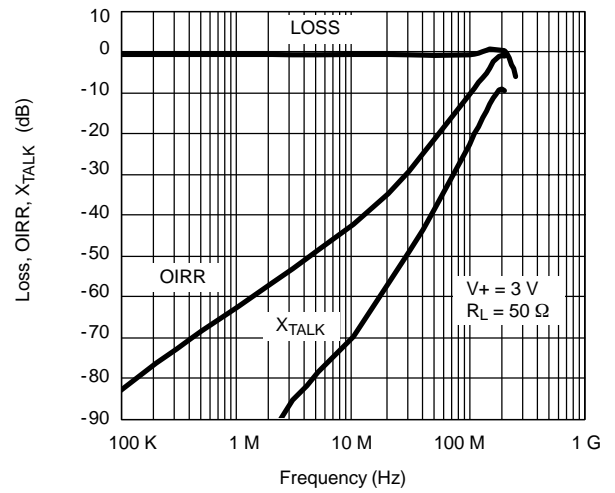


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

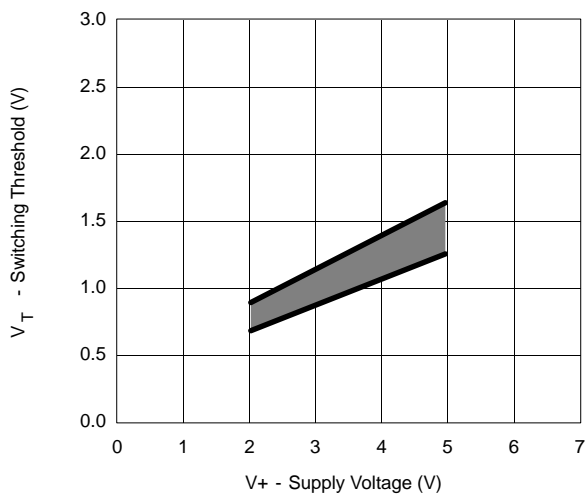
Switching Time vs. Temperature and Supply Voltage



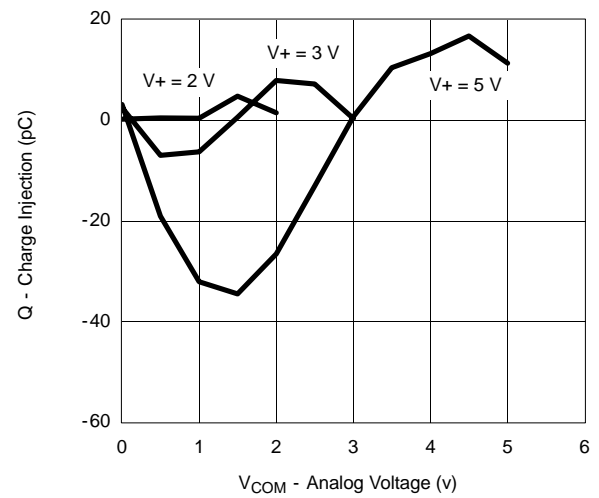
Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

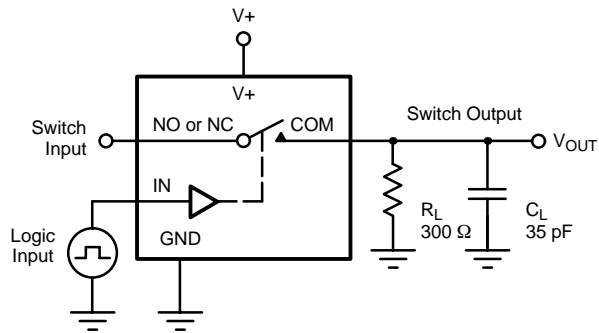


Switching Threshold vs. Supply Voltage



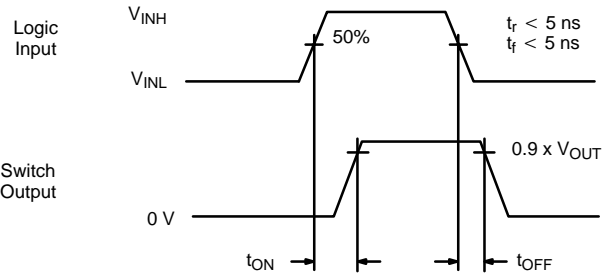
Charge Injection vs. Analog Voltage



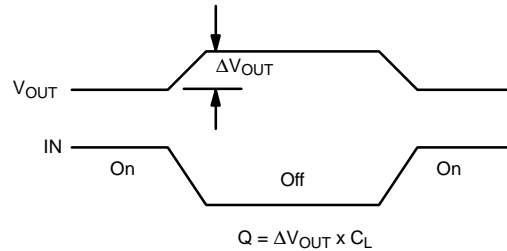
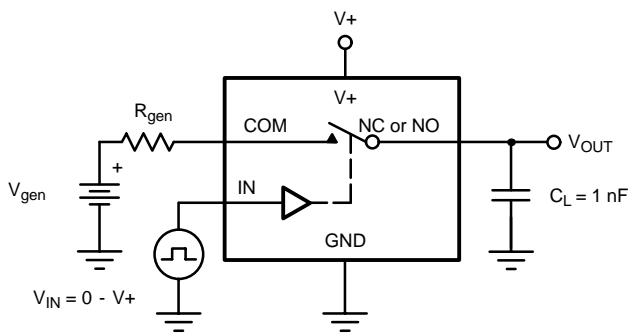
TEST CIRCUITS


C_L (includes fixture and stray capacitance)

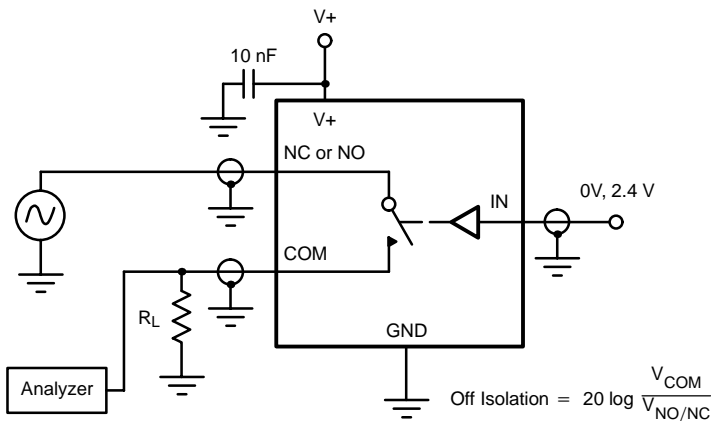
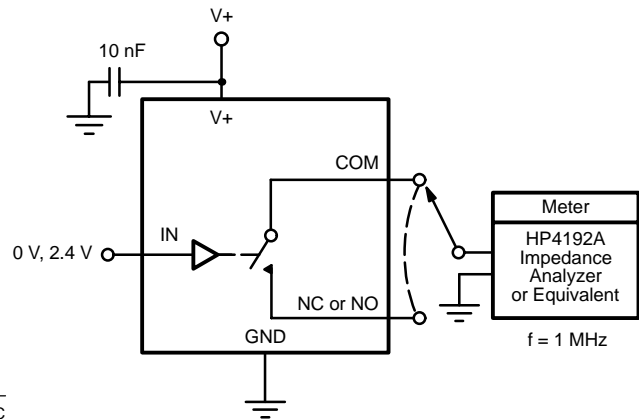
$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
 Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time


IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 2. Charge Injection

FIGURE 3. Off-Isolation

FIGURE 4. Channel Off/On Capacitance