CS22250 Data Sheet

Wireless 10BT Controller

1 Introduction

The Cirrus Logic CS22250 Wireless Network Controller enables high speed, 11 Mbps digital wireless data connectivity for wireless Ethernet bridge, access points, and other broadband applications.

The CS22250 is a highly integrated single-chip Ethernet bridge solution for wireless networks supporting video, audio, voice, and data traffic. The programmable controller executes Cirrus Logic's Whitecap™2 networking protocol that provides Wi-Fi™ (802.11b) compliance, multimedia and a foundation for quality of service (QoS) applications, and Ethernet to wireless bridging. The device includes several high performance components including an ARM7TDMI RISC processor core, a Forward Error Correction (FEC) codec, and a wireless radio MAC supporting up to 11 Mbps throughput. The CS22250 utilizes state of the art 0.18um CMOS process and is housed in a 208 FPBGA compact package, offering low-lead inductance suitable for highly integrated radio applications. The core is powered at 1.8 V with 3.3V I/O to reduce overall power consumption. In addition, the CS22250 supports various power management modes for host, MAC, baseband, and radio interfaces.

The CS22250 is designed to provide integrated low cost IEEE 802.3 standard compliant system solutions. The controller also incorporates a high-speed parallel interface, which can be used to interface with other ASICs (eg: HNPA 2.0 Network controller) to implement a variety of other wireless LAN bridging products.

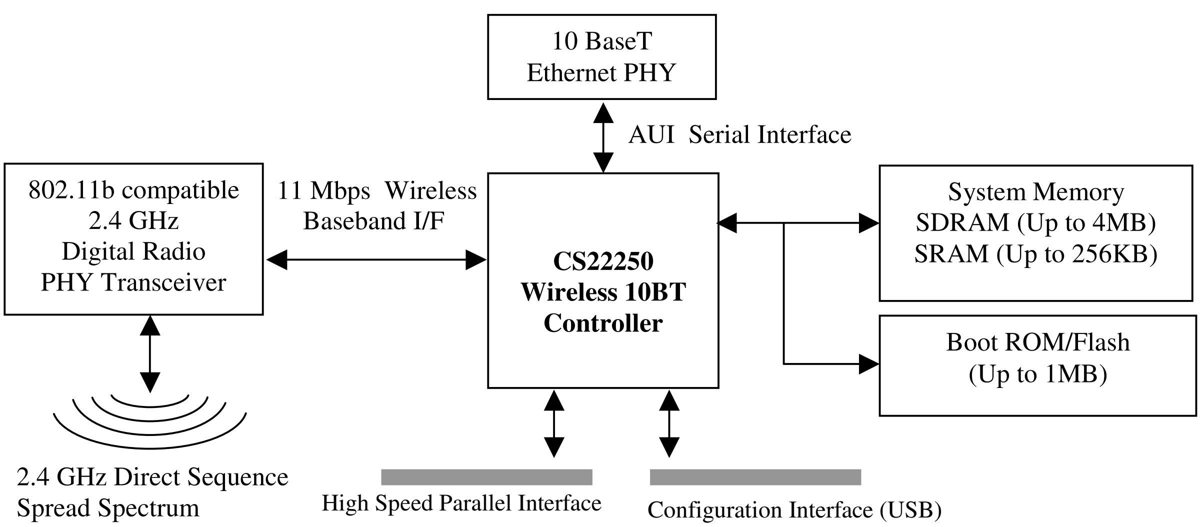


Figure 1. Example System Block Diagram

2 Features

Embedded ARM Core and System Support Logic
- High Performance ARM7TDMI RISC processor core up to 77MHz
- 4KB integrated, one-way set associative, unified, write through cache
- Individual interrupt for each functional block
- Two 23-bit programmable (periodic or one-shot) general purpose timers
- 8 Dword (32-bits) memory write and read buffers for high system performance
- Abort cycle detection and reporting for debugging
- ARM performance monitoring function for system fine-tuning
- Programmable performance improvement logic based on system configuration.

Enhanced Memory Controller Unit
- Programmable memory controller unit supporting SDRAM /async SRAM/boot ROM/Flash interface
- 16-bit data bus with 12-bit address supporting up to 4MB and up to 103 MHz (100/133MHz SDRAM)
- 8-bit data bus with addressing support up to 1MB of boot ROM/Flash
- Programmable SDRAM timing and size parameters, such as CAS latencies and number of banks, columns and rows
- Flexible independent DMA engines for Ethernet MAC, Digital Radio and External Bus functional units

FEC codec
- High performance Reed-Solomon coding for error correction (255:239 block coding)
- Reduces error probability of a typical 10e-3 error rate environment to 10e-9
- Programmable rate FEC engine to optimize channel efficiency
- Low latency, fully pipelined hardware encoding and decoding. Supports byte-wise single cycle throughput up to 77MHz, with a sustain rate of 77MBps
- Double buffering (63 Dword read/write buffer) to enhance system performance

Digital Wireless Radio MAC
- Glue-less interface to 802.11b radio baseband transceiver
- 11Mbps data rate
- 32 Dword transmit/receive FIFO
- Supports clear channel assessment (CCA)

Ethernet Interface
- IEEE802.3 Ethernet MAC controller
- Two independent full-duplex DMA channels transfer between Ethernet interface to system memory
- Standard 7-pin serial interfaces to AUI or Twisted Pair 10-BaseT
- Standard half-duplex CSMA/CD and full-duplex operation

USB Device Configuration Interface
- USB 1.1 compliant

2 Features and Benefits

Power Management

- ACPI compliant
- Programmable sleep timer for ARM core and system power management
- Independent power management control for individual functional blocks
- Supports variable rate radio transmit, receive and standby radio power modes

Clock and PLL Interface

- Single 44MHz crystal oscillator reference clock
- Internal PLL to generate internal and on board clocks

Chip Processing and Packaging

- 208 FPBGA package and 0.18um state of the art CMOS process
- 1.8 V core for low power consumption. 3.3V I/O

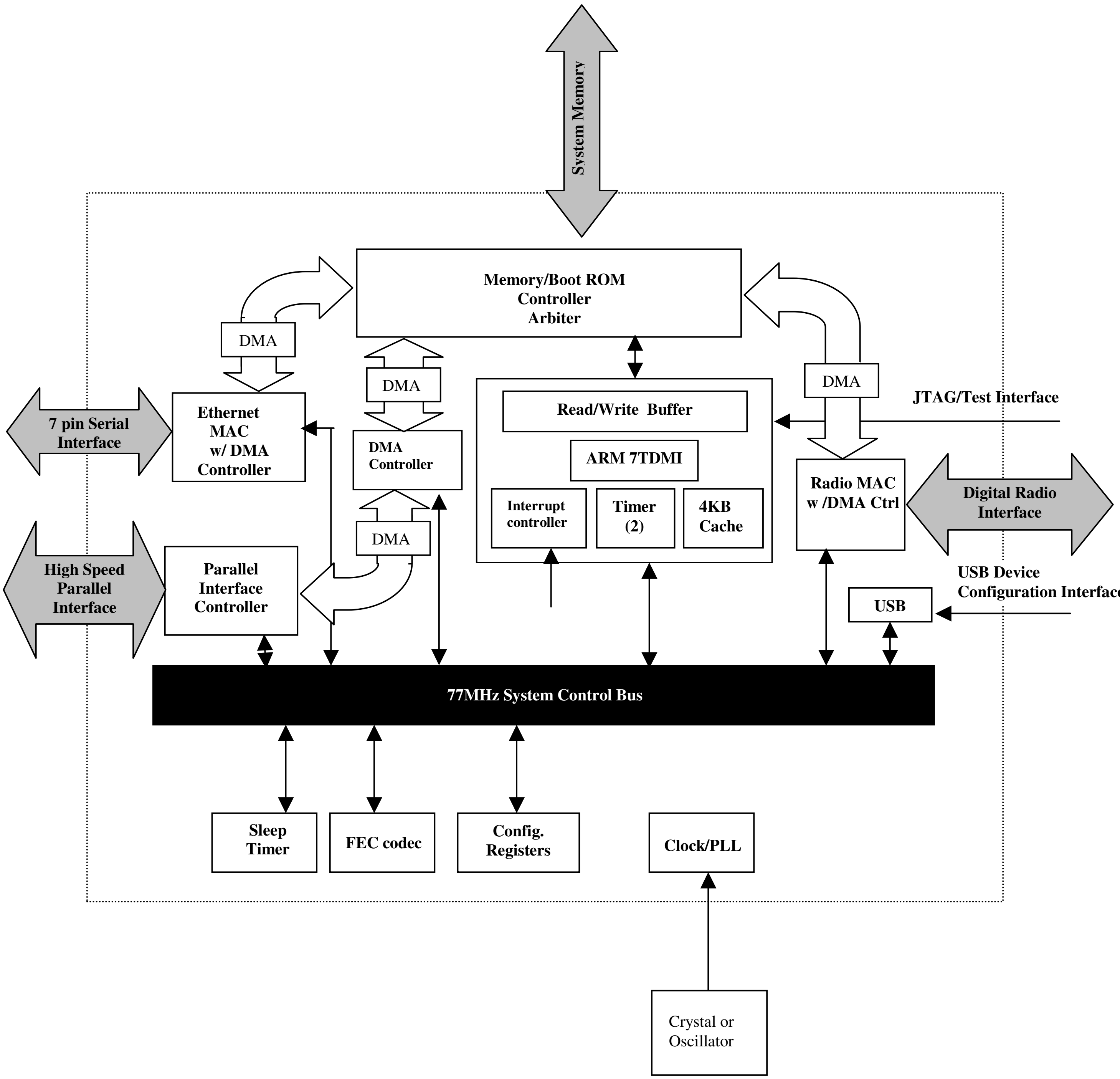
High Speed Parallel Interface

- Multi-purpose 32bit bus for connecting with other high speed devices
- Supports operations at ½ the speed of the ARM clock (up to 38MHz)
- Two independent full-duplex DMA channels transfer between external devices to ARM system memory
- Supports one external interrupt pin to the ARM core

IMPORTANT NOTICE

3 Functional Description

Figure 2. Block Diagram of Major Functional Units



3.1 Embedded ARM core and System Support Logic

The processing elements of the CS22250 include the ARM7TDMI core and its associated system control logic. The ARM processor and system controller consist of a memory management unit, 4-KB write through cache controller, 20 IRQ and 4 FIRQ interrupt controller, and 2 general purpose timers. The ARM processor and integrated system support logic provide the necessary execution engine to support a real time multi-tasking operating system, the network protocol stack, and firmware services.

Memory Management Unit The ARM instructions and data are fetched from system memory per “cache-line” (4/8 – Dwords /Programmable) when caching is turned on. During a cache line fill, critical word data, i.e., the access that caused the miss, is forwarded to the ARM and also written into the data RAM cache. The non-critical words in the line fetched following the critical word are then written to the cache on a Dword basis, as they become available.

Memory writes are posted to dual 4-Dwords (32-bit) memory write posting buffers. Write posts use the sequential addressing feature on the memory bus. With dual buffering, an out-of-sequence write will post to one write buffer while the other buffer is flushed to memory.

There is one 8Dword read buffer in the MEM block. The buffer is used for both cacheable and non-cacheable memory space.

Interrupt Controller

The Interrupt Controller provides two interrupt channels to the ARM processor. One interrupt channel is presented to the ARM on its *nFIQ* and the other channel is presented on its *nIRQ* pin. These are referred to as the FIQ channel and the IRQ channel. Both channels operate in identical but independent fashion. The FIQ channel has a higher priority on the ARM processor than the IRQ channel.

The Interrupt Controller includes a CONTROL register for each logical interrupt in the ARM Complex. The CONTROL register serves the following main purposes:

- Provides the mapping between the EXT_INT inputs (physical interrupts) and the logical interrupt
- Selects the particular type of signaling expected on the EXT_INT inputs: level, edge, active level high/low, etc.
- Enables or disables a logical interrupt

3.2 Digital Wireless Radio Interface

The CS22250 digital radio MAC I/F supports multiple radio baseband and RF interfaces. The baseband registers can be programmed during the configuration time using the control port interface. The MAC also provides the capability of programming the signal, service and length on a per packet basis without ARM intervention. This significantly improves the performance of the system.

There are three primary digital interface ports for the CS22250 that are used for configuration and during normal operation.

These ports are:

- The Control Port, which is used to configure, set power consumption modes, write and/or read the status of the radio base band registers
- The TX Port, which is used to output the data that needs to be transmitted from the network processor
- The RX Port, which is used to input the received demodulated data to the network processor

3.3 FEC Codec

The FEC codec performs Reed-Solomon code encoding to protect the data before it is transmitted to a noisy channel. It is a similar code as employed by the digital broadcast industry, such as ITU-T J.83 for DVB. The RS(255, 239) code implemented by the CS22250 can reduce error probability to 1/10e-9 in a typical 1/10e-3 error rate environment. The encoder/decoder can be programmed to vary the coding block length (*N*) and correctable error (*t*) to optimize the tradeoff between channel utilization and data protection. The range of *N* is currently set from 20 to 255, and the *t* is 8. The symbol size is fixed at 8 bits.

Coding parameters can be set real time, allowing maximum flexibility for the system to adjust the FEC setting, such as block size, in order to optimize channel efficiency. The encoder also has a very low latency of two cycles. Both the encoder and decoder are fully pipelined in structure to achieve single cycle throughput. The FEC can be disabled in firmware.

3.4 High Speed Parallel Interface

This optional connectivity interface is the extension of the ARM control bus brought outside of the CS22250 chip. In order to reduce the pin count, address and data are multiplexed in a 32-bit address/data External Control Bus. For ease of connecting other devices to the CS22250, this bus runs at half the speed of the internal ARM control bus. The external control Bus interface exchanges data with the main memory via DMAC (DMA controller block). This functional block supports two DMA engines for full duplex operation. Moreover, one external interrupt pin is supported.

3.5 Programmable Memory Controller

The CS22250 incorporates a general-purpose memory controller. The memory controller supports both SDRAM/async SRAM memory interface and a FLASH memory interface.

In the RAM configuration, the system memory interface supports up to 4-Mbyte of 16-bit SDRAM running at frequency up to 103 MHz single-state access cycles or 256KB of 16 bit async SRAM. The memory controller provides programming of SDRAM parameters such as CAS latency, refresh rate etc; these registers are located in miscellaneous configuration registers. The CS22250 memory controller supports power saving feature of the SDRAM by toggling the Clock Enable (CKE) signal. When there are no pending memory requests from any internal requester, the CS22250 will keep CKE low to cause the SDRAM to stay in power down mode. Once a memory request is active, the CS22250 will assert CKE high to cause the SDRAM to come out of power down mode. Typicallythis can reduce memory power consumption by up to 50%.

In ROM configuration, firmware for CS22250 is stored in non-volatile memory and is accessed through the Boot ROM interface. The maximum addressable ROM space supported is 1MB. ROM read/write and output enable are shared with RAM control pins.

3.6 Ethernet MAC Controller

The Ethernet MAC controller interface allows the Cirrus Logic CS22250 to provide connectivity to an Ethernet local area network. The controller can be used to interface with a cable or xDSL modem to share high speed internet multimedia and data traffic in a wireless home network. The Ethernet MAC controller is fully compliant with the IEEE 802.3 standard. The controller supports both half-duplex CSMA/CD and full-duplex operation at 10Mbps.

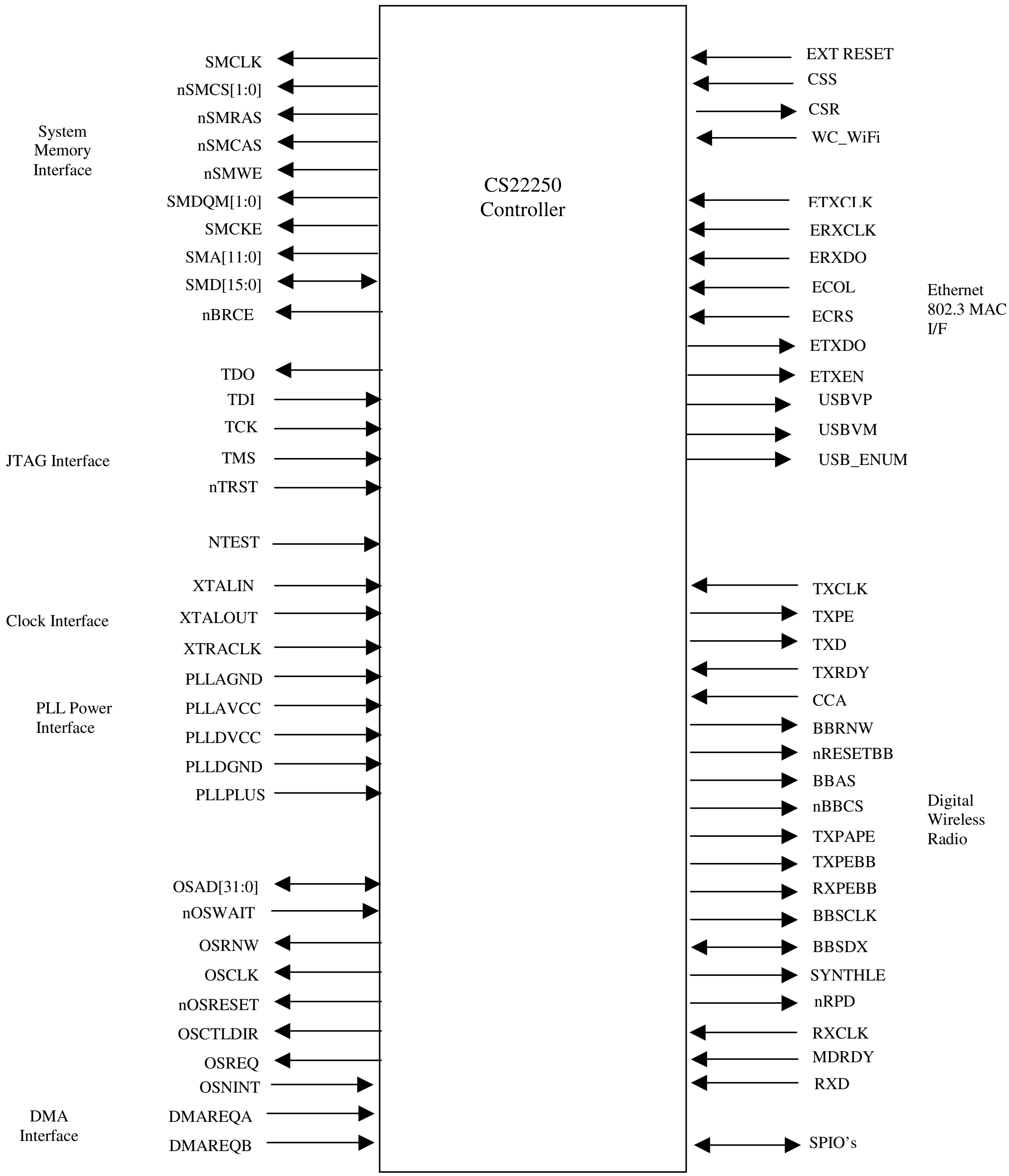
The Ethernet MAC incorporates two power safe modes. The first disable mode disables the entire MAC core including clocks. The second is a partial sleep mode, which only disables transmit logic. In this mode, the entire MAC is powered upon receiving an Ethernet packet. The Ethernet MAC uses two independent DMA controllers to support full duplex operations with the system memory. The DMA controller is programmed and configured by the ARM.

3.7 USB Configuration Interface

The USB interface is a device interface that allows for bridge configuration from a USB-enabled PC. Switching between normal and configuration modes is controlled by external logic.

4 Pinout and Signal Descriptions

Figure 3. CS22250 Logical Pin Groupings



This section provides detailed information on the CS22250 signals. The signal descriptions are useful for hardware designers who are interfacing the CS22250 with other devices.

System Memory Interface

The system memory interface supports standard SDRAM interface, Async SRAM and FLASH. There are a total of 37 signals in this interface.

SMCLK Output

System mem clock for SDRAM. Currently the interface supports 103 MHz for a maximum bandwidth of 200Mbytes/sec.

nSMCS0 Output

Chip select bit 0. This signal is used to select or deselect the SDRAM for command entry. When SMNCS is low it qualifies the sampling of nSMRAS, nSMCAS and nSMWE. Also, used as testmode(2) when NTEST pin is '0'.

nSMCS1 Output

Chip select bit 1.

NBRCE Output

Chip select for ROM access. This signal is used to select or deselect the boot ROM memory. Also used during reset to latch in the strap value for Ethernet; if set to a '1' implies Ethernet functional unit block is ‘enable’.

NSMRAS Output

Row address select. Used in combination with nSMCAS, nSMWE and nSMCS to specify which SDRAM page to open for access. Also used during reset to latch in the strap value for clk_bypass; if set to a '1' implies bypassing clock module; whatever clk is applied on the input clock is used for memclk and ctlclk. Also shared as the ROMOE signal.

NSMCAS Output

Column address select. Used in combination with nSMRAS, nSMWE and nSMCS to specify which piece of data to access in selected page. Also used during reset to latch in the strap value for same_freq; if set to a '1' implies internal mem_clk and arm_clk are running at the same frequency and 180 degrees out of phase.

NSMWE Output

Write Enable. Used in combination with nSMRAS, nSMCAS, and nSMWE to specify whether the current cycle is a read or a write cycle. Also used during reset to latch in the strap value for tst_bypass; if set to a '1' implies PLL bypass. Also shared as the ROMWE to do flash programming.

SMDQM[1:0] Output

Data mask bit 1:0. These signals function as byte enable lines masking unwanted bytes on memory reads and write. Also used as testmode(1:0) when NTEST pin is '0'.

SMCKE Output

Clock enable. SMCKE is used to enable and disable clocking of internal RAM logic.

SMA0 Output

Address bit0. The address bus specifies either the row address or column address. Also shared as boot-rom address bit0. This pin should have a pull-down.

SMA1 Output

Address bit1. Also shared as boot-rom address bit1. This pin should have a pull-down.

SMA2 Output

Address bit2. Also shared as boot-rom address bit2. This pin should have a pull-down.

SMA3 Output

Address bit3. Also shared as boot-rom address bit3. Also used during reset to latch in the strap value for ossel; if set to a '1' implies optslot mode.

SMA4 Output

Address bit4. Also shared as boot-rom address bit4. Also used during reset to latch in the strap value for romcfg. This pin should be pull down.

SMA5 Output

Address bit5. Also shared as boot-rom address bit5. Also used during reset to latch in the strap value for test_rst_enb; if set to a '0' implies normal operation mode.

SMA6 Output

Address bit6. Also shared as boot-rom address bit6. Also used during reset to latch in the strap value for freq_sel(0). Freq_sel(2:0) is used to select the multiplication factor for the internal PLL (000=1x and 111=8x).

SMA7 Output

Address bit7. Also shared as boot-rom address bit7. Also used during reset to latch in the strap value for freq_sel(1). Freq_sel(2:0) is used to select the multiplication factor for the internal PLL (000=1x and 111=8x).

SMA8 Output

Address bit8. Also shared as boot-rom address bit8. Also used during reset to latch in the strap value for freq_sel(2). Freq_sel(2:0) is used to select the multiplication factor for the internal PLL (000=1x and 111=8x).

SMA9 Output

Address bit9. Also shared as boot-rom address bit9. Also used during reset to latch in the strap value for sdram_delay(0). Sdram_delay(2:0) is used to select the delay factor for the internal memory clock (000=0ns and 111=1.75ns with each .25ns increments).

SMA10 Output

Address bit10. Also shared as boot-rom address bit10. Also used during reset to latch in the strap value for sdram_delay(1). Sdram_delay(2:0) is used to select the delay factor for the internal memory clock (000=0ns and 111=1.75ns with each .25ns increments).

SMA11 Output

Address bit11. Also shared as boot-rom address bit11. Also used during reset to latch in the strap value for sdram_delay(2). Sdram_delay(2:0) is used to select the delay factor for the internal memory clock (000=0ns and 111=1.75ns with each .25ns increments).

SMD[7:0] Bidirectional

Data bus. The data bus contains the data to be written to memory on a write cycle and the read return data on a read cycle.

SMD[15:8] Bidirectional

Shared data bus. The data bus contains the data to be written to RAM memory on a write cycle and the read return data on a read cycle. Data bit [15:8] is also shared as boot ROM address bit [19:12].

Digital Wireless Radio Interface

All Radio input buffers are Schmitt triggered input buffers. There are a total of 25 signals in this interface.

TXCLK Input

Transmit clock is a clock input from the radio baseband processor. This signal is used to clock out the transmit data on the rising edge of TXCLK.

TXPEBB Output

Baseband transmit power enable is an output from the MAC to the radio baseband processor. When active, the baseband processor transmitter is configured to be operational, otherwise the transmitter is in standby mode.

TXD Output

It is the serial data output from the MAC to the radio baseband processor. The data is transmitted serially with the LSB first. The data is driven by the MAC on the rising edge of TXCLK and is sampled by the radio baseband processor on the falling edge of TXCLK and rising edge of TXCLK.

TXRDY Input

Transmit data ready is an input to the MAC from the radio baseband processor to indicate that the radio baseband processor is ready to receive the data packet over the TXD signal. The signal is sampled by the MAC on the rising edge of TXCLK.

CCA Input

Clear channel assessment is an input from the radio baseband processor to signal that the channel is clear to transmit. When this signal is a 0, the channel is clear to transmit. When this signal is a 1, the channel is not clear to transmit. This helps the MAC to determine when to switch from receive to transmit mode.

BBRNW Output

Baseband read/write is an output from the MAC to indicate the direction of the SD bus when used for reading or writing data. This signal has to be setup to the rising edge of BBSCLK for the baseband processor and is driven on the falling edge of BBSCLK.

NRESETBB Output

Baseband reset is an output of the MAC to reset the baseband processor.

BBAS Output

Baseband address strobe is used to envelop the address or the data on the BBSDX bus. A logic 1 envelops the address and a logic 0 envelops the data. This signal has to be setup to the rising edge of BBSCLK for the baseband processor and is driven on falling edge of BBSCLK.

NBBCS Output

Baseband chip select is an active low output to activate the serial control port. When inactive, the SD, BBSCLK, BBAS and BBRNW signals are 'don't cares'.

TXPAPE Output

Radio power amplifier power enable is a software controlled output. This signal is used to gate power to the power amplifier.

TXPE Output

Radio transmit power enable indicates if transmit mode is enabled. When low, this signal indicates receive mode.

RXPEBB Output

Baseband receive power enable is an output that indicates if the MAC is in receive mode. A output signal to baseband processor enables receive mode in baseband processor.

BBSCLK Output

Baseband serial clock is a programmable output generated by dividing ARM_CLK by 14 (default). This clock is used for the serial control port to sample the control and data signals.

BBSDX Bi-directional

Baseband serial data is a bi-directional serial data bus, which is used to transfer address and data to/from the internal registers of the baseband processor.

SYNTHLE Output

Synthesizer latch enable is an active high signal used to send data to the synthesizer. (Use with modular Cresta II Modular Radio only).

NRPD Output

Radio power down enable. This active low signal is used for power management purposes for the radio circuitry.

RXCLK Input

This is an input from base band processor. It is used to clock in received data from base band processor.

MDRDY Input

Receive data ready is an input signal from the baseband processor, indicating a data packet is ready to be transferred to the MAC. The signal returns to inactive state when there is no more receiver data or when the link has been interrupted. This signal is sampled on the falling edge of RXCLK and sampled at rising edge of RXCLK.

RXD Input

Receive data is an input from the baseband processor transferring demodulated header information and data in a serial format. The data is frame aligned with MD_RDY. This signal is sampled on the falling edge of RXCLK and sampled at rising edge of RXCLK.

DACAVCC Input

Analog power for DAC. 3.3V.

DACAGND Input

Analog ground for DAC.

RLQ Output

Radio link quality is based on packet error rate. Active low implies packet received without errors*. Note: lost packets arenot detected.*

PLL and Clock Interface

There are three clock pins and five PLL power pins for a total of 8 signals in this interface.

XTAL_CLKIN Input

44 MHz Reference clock input/crystal clock input.

XTALOUT Output

Reference crystal clock output.

XTRACLK Input

Second clock input to clock module. Use depending on clock module configuration setting. Refer to the clock section for more information.

PLLAGND Input

Analog PLL ground.

PLLAVCC Input

Analog PLL power. 3.3V input.

PLLDGND Input

Digital PLL ground.

PLLDVCC Input

Digital PLL power. This is 1.8V input.

PLLPLUS Input

Analog PLL ground.

Ethernet Interface

ETXCLK Input

Transmit clock. A 10 MHz clock input. This clock signal provides the reference sampling point for transmit data.

ETXDOOutput

Transmit data. This output signal is NRZ formatted and is transmitted to the Ethernet PHY layer.

ETXEN Output

Transmit enable. This signal is synchronous to ETXCLK. It enables data transmission.

ECOL Input

Collision signal. This input signal indicates whether a collision occurred in the network.

ECRS Input

Carrier detect. An input from the PHY layer thatindicates there is activity in the network.

ERXCLK Input

Receive clock. This is the reference receive clock from the PHY layer.

ERXDO Input

Receive data. It is synchronized with receive clock.

System Reset

EXT_RESET Input

The system must place the RESET signal in a high-Z state during card power up. The signal must remain high impedance for at least 1 msec after Vcc becomes valid.

CSS Input

(Clear Settings Set) Network security ID reset request.

CSR Output

(Clear Settings Reset) Network security ID reset successful.

External Control Bus

OSAD[31:0] Bi-directional

Multiplexed address and data bus on the external control bus to a shared 32-bit bus on the external control bus. Also, de-multiplexing of the data from external control bus to the internal control bus.

NOSWAIT Input

The wait bus is a single bit bus, which indicates the processing element addressed on the external control address space is not capable of completing the transfer on this cycle.

OSRNW Output

External control bus read/write.

OSCLK Output

External control bus clock. This clock is half the frequency of the internal control clock. External processing element clocks the input data to the OSAD bus on this clock edge.

NOSRESET Output

External control bus reset.

OSCTLDIR Output

External control bus direction control. The direction bus is a single bit bus, which indicates the direction of the tri-state drivers on the address/data bus. A logic '0' on this bus indicates the tri-state drivers are on source mode on the OS bus and a logic '1' on this bus indicates the tri-state drivers are on receive mode from the OS bus.

OSREQ Output

External control bus request. It indicates a transfer has been initiated, addressed to the external control bus address space. The external control bus FUB shall de-assert the transfer request on the next OS cycle, if the OS wait signal is not asserted by the processing element on the OS bus during the data phase.

OSNINT Input

This is the interrupt for external bus interface to the ARM core.

External DMA Interface

DMAREQA Input

DMA request channel A. When driven HIGH, this signal tells the DMA controller that an agent on the external control bus is requesting a DMA access.

DMAREQB Input

DMA request channel B. When driven HIGH, this signal tells the DMA controller that an agent on the external control bus is requesting a DMA access.

Debug Interface

TDO	Output

Test data output.

TDI — Input

Test data input. This input has integral pull-up.

TCK — Input

Test clock signal.

TMS — Input

Test mode select. This input has integral pull-up.

NTRST — Input

Test interface reset. This input has integral pull-up.

USB Interface

USBVP — Bi-directional

Differential USB data plus. For high-speed mode, this signal is pull up to 5 volt during IDLE state (see USB_ENUM).

USBVM — Bi-directional

Differential USB data minus.

USB_ENUM — Output

USB Enumeration. Indicates disconnect/connect event. USB_ENUM is used to pull the D+ line high, indicating to the host or hub a USB bus “full rate” connection is active.

Miscellaneous Interface

RSVD_0:2 (SPIO) Bi-directional

Special Purpose I/O reserved for supporting custom interfaces.
** Check with Cirrus Logic support for supported options and usage.*

NTEST Input

Chip test mode pin. Used in conjunction with SMNCS0, SMDQM[0:1]. Pull up for normal operation.

WC_WiFi Input

External Dual MAC mode switch control signal. Use for hardware switching between Whitecap2 Wi-Fi (802.11b) and multimedia modes. (WiFi = low).

Power and Ground

VCC (5V and 3.3V)[1] Input

5V inputs. There are a total of 3 pins.

VDD (3.3V) Input

3.3V inputs. There are a total of 20 pins.

VEE (1.8V) Input

1.8 inputs to the core. There are a total of 9 pins.

VSS Input

Ground. There are a total of 27 pins.

[1] 5V or 3.3V depending on desired configuration.

Figure 4. CS22250 208 pin FPBGA Pinout Diagram

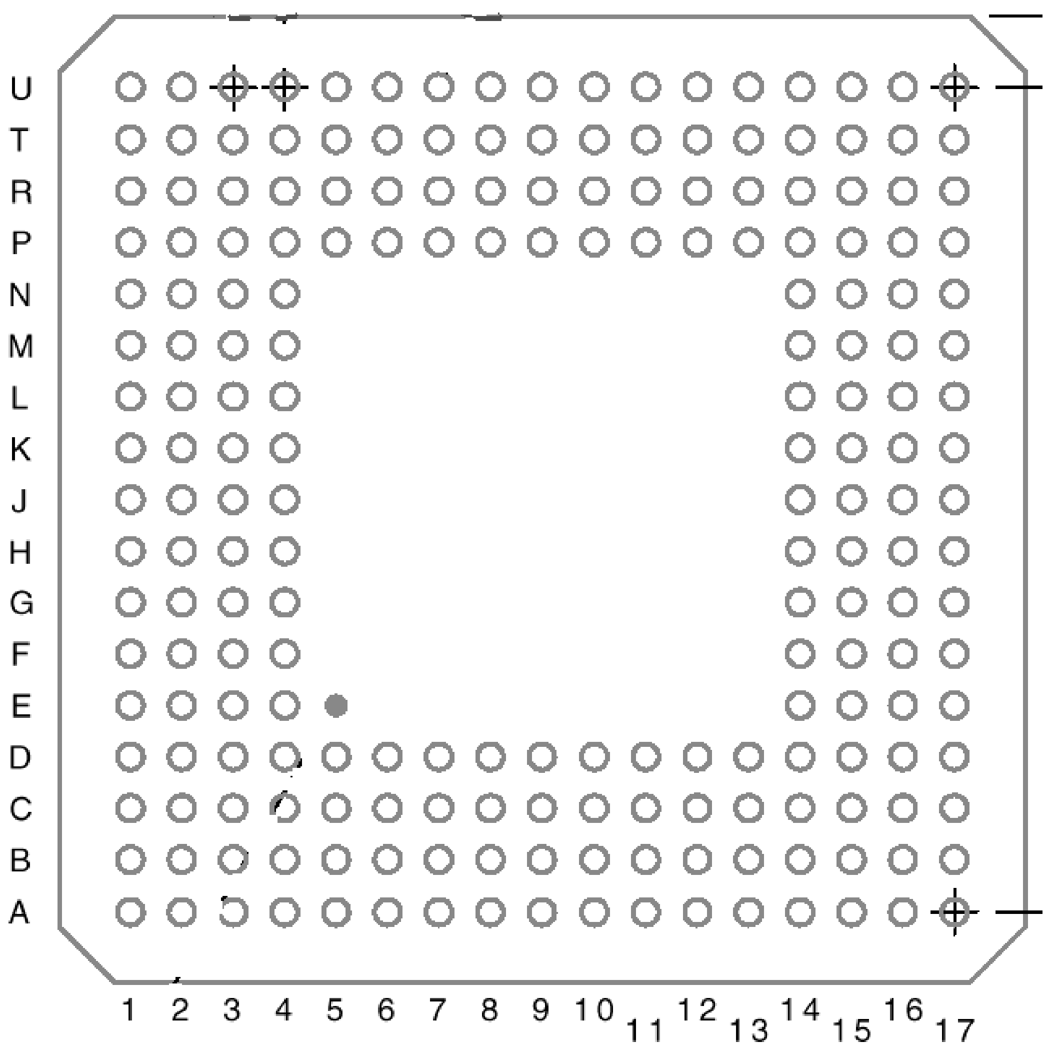


Table 1. Pin Listing by Name

ball	name	ball	name	ball	name	ball	name
H17	BBAS	B02	OSAD10	T16	SMA00	D15	TXD
K17	BBNCS	L04	OSAD11	U17	SMA01	E16	TXPAPE
H15	BBRNW	P03	OSAD12	P14	SMA02	B17	TXPE
J16	BBSCLK	P01	OSAD13	T17	SMA03	E15	TXPEBB
H14	BBSDX	N03	OSAD14	R17	SMA04	D16	TXRDY
T04	CAL/C3CS	N04	OSAD15	P15	SMA05	E14	USB_ENUM
C16	CCA	E01	OSAD16	N14	SMA06	B06	USBVM
U05	CSR	E03	OSAD17	P17	SMA07	D06	USBVP
P06	CSS	E02	OSAD18	N15	SMA08	A01	VCC
D11	DACAVDD	H02	OSAD19	M14	SMA09	J01	VCC
C13	DACAVSS	G04	OSAD20	M16	SMA10	T02	VCC
D12	RSVD	F01	OSAD21	M15	SMA11	A12	VDD
B12	RSVD	G01	OSAD22	U07	SMCKE	B04	VDD
A06	ECOL	F02	OSAD23	U11	SMCLK	B11	VDD
A02	ECRS	K03	OSAD24	T08	SMD00	B14	VDD
C04	ERXCLK	R02	OSAD25	R10	SMD01	C06	VDD
A03	ERXD0	L01	OSAD26	P11	SMD02	C15	VDD
B05	ETXCLK	M02	OSAD27	T11	SMD03	D09	VDD
A05	ETXD0	M03	OSAD28	R11	SMD04	E17	VDD
A04	ETXEN	M04	OSAD29	P12	SMD05	F04	VDD
H01	EXT_RESET	K02	OSAD30	R12	SMD06	G16	VDD
G15	MDRDY	F03	OSAD31	P13	SMD07	J15	VDD
A07	N/C	G03	OSCLK	U12	SMD08	K01	VDD
A13	N/C	D01	OSCTLDIR	R13	SMD09	N17	VDD
B08	N/C	U01	OSDMAREQ0	U13	SMD10	P16	VDD
C03	N/C	T03	OSDMAREQ1	U14	SMD11	R04	VDD
C07	N/C	L02	OSNINT	R14	SMD12	R08	VDD
C08	N/C	C02	OSNRESET	U15	SMD13	T01	VDD
C12	N/C	L03	OSNWAIT	U16	SMD14	T10	VDD
R05	N/C	H03	OSREQ	R15	SMD15	T12	VDD
T06	N/C	G02	OSRNW	U06	SMDQM00	T14	VDD
L15	NBRCE	A16	PLLAGND	T07	SMDQM01	U09	VDD
G14	NRESETBB	D14	PLLAVCC	P08	SMNCAS	A09	VEE
K14	NTEST	B15	PLLDGND	R06	SMNCS00	C09	VEE
C11	NTRST	A17	PLLDVCC	P07	SMNCS01	D07	VEE
D03	OSAD00	A15	PLLPLUS	L16	SMNRAS	J03	VEE
E04	OSAD01	F15	RLQ	L14	SMNWE	J04	VEE
D04	OSAD02	B16	RNPD	U03	SYNTH_LE1	J14	VEE
R03	OSAD03	B03	RSVD	P04	SYNTH_LE2	K16	VEE
R01	OSAD04	D05	RSVD_0	J17	SYNTHLE	R09	VEE
P02	OSAD05	U04	RSVD_1	A10	TCK	T09	VEE
N01	OSAD06	P05	RSVD_2	B10	TDI	A08	VSS
N02	OSAD07	G17	RXCLK	C10	TDO	A11	VSS
D02	OSAD08	F14	RXD	D10	TMS	A14	VSS
C01	OSAD09	F17	RXPEBB	D17	TXCLK	B01	VSS

ball	name	ball	name	ball	name	ball	name
B07	VSS	H16	VSS	N16	VSS	U02	VSS
B09	VSS	J02	VSS	P09	VSS	U08	VSS
C05	VSS	K04	VSS	P10	VSS	U10	VSS
C17	VSS	K15	VSS	R07	VSS	T05	WC_WiFi
D08	VSS	L17	VSS	R16	VSS	C14	XTALCLKIN
F16	VSS	M01	VSS	T13	VSS	D13	XTALOUT
H04	VSS	M17	VSS	T15	VSS	B13	XTRACLK

Table 2. Pin Listing by Ball

ball	name	ball	name	ball	name	ball	name
A01	VCC	C12	N/C	G16	VDD	N04	OSAD15
A02	ECRS	C13	DACAVSS	G17	RXCLK	N14	SMA06
A03	ERXD0	C14	XTALCLKIN	H01	EXT_RESET	N15	SMA08
A04	ETXEN	C15	VDD	H02	OSAD19	N16	VSS
A05	ETXD0	C16	CCA	H03	OSREQ	N17	VDD
A06	ECOL	C17	VSS	H04	VSS	P01	OSAD13
A07	N/C	D01	OSCTLDIR	H14	BBSDX	P02	OSAD05
A08	VSS	D02	OSAD08	H15	BBRNW	P03	OSAD12
A09	VEE	D03	OSAD00	H16	VSS	P04	SYNTH_LE2
A10	TCK	D04	OSAD02	H17	BBAS	P05	RSVD_2
A11	VSS	D05	RSVD_0	J01	VCC	P06	CSS
A12	VDD	D06	USBVP	J02	VSS	P07	SMNCS01
A13	N/C	D07	VEE	J03	VEE	P08	SMNCAS
A14	VSS	D08	VSS	J04	VEE	P09	VSS
A15	PLLPLUS	D09	VDD	J14	VEE	P10	VSS
A16	PLLAGND	D10	TMS	J15	VDD	P11	SMD02
A17	PLLDVCC	D11	DACAVDD	J16	BBSCLK	P12	SMD05
B01	VSS	D12	RSVD	J17	SYNTHLE	P13	SMD07
B02	OSAD10	D13	XTALOUT	K01	VDD	P14	SMA02
B03	RSVD	D14	PLLAVCC	K02	OSAD30	P15	SMA05
B04	VDD	D15	TXD	K03	OSAD24	P16	VDD
B05	ETXCLK	D16	TXRDY	K04	VSS	P17	SMA07
B06	USBVM	D17	TXCLK	K14	NTEST	R01	OSAD04
B07	VSS	E01	OSAD16	K15	VSS	R02	OSAD25
B08	N/C	E02	OSAD18	K16	VEE	R03	OSAD03
B09	VSS	E03	OSAD17	K17	BBNCS	R04	VDD
B10	TDI	E04	OSAD01	L01	OSAD26	R05	N/C
B11	VDD	E14	USB_ENUM	L02	OSNINT	R06	SMNCS00
B12	RSVD	E15	TXPEBB	L03	OSNWAIT	R07	VSS
B13	XTRACLK	E16	TXPAPE	L04	OSAD11	R08	VDD
B14	VDD	E17	VDD	L14	SMNWE	R09	VEE
B15	PLLDGND	F01	OSAD21	L15	NBRCE	R10	SMD01
B16	RNPD	F02	OSAD23	L16	SMNRAS	R11	SMD04
B17	TXPE	F03	OSAD31	L17	VSS	R12	SMD06
C01	OSAD09	F04	VDD	M01	VSS	R13	SMD09
C02	OSNRESET	F14	RXD	M02	OSAD27	R14	SMD12
C03	N/C	F15	RLQ	M03	OSAD28	R15	SMD15
C04	ERXCLK	F16	VSS	M04	OSAD29	R16	VSS
C05	VSS	F17	RXPEBB	M14	SMA09	R17	SMA04
C06	VDD	G01	OSAD22	M15	SMA11	T01	VDD
C07	N/C	G02	OSRNW	M16	SMA10	T02	VCC
C08	N/C	G03	OSCLK	M17	VSS	T03	OSDMAREQ1
C09	VEE	G04	OSAD20	N01	OSAD06	T04	CAL/C3CS
C10	TDO	G14	NRESETBB	N02	OSAD07	T05	WC_WiFi
C11	NTRST	G15	MDRDY	N03	OSAD14	T06	N/C

ball	name	ball	name	ball	name	ball	name
T07	SMDQM01	T14	VDD	U04	RSVD_1	U11	SMCLK
T08	SMD00	T15	VSS	U05	CSR	U12	SMD08
T09	VEE	T16	SMA00	U06	SMDQM00	U13	SMD10
T10	VDD	T17	SMA03	U07	SMCKE	U14	SMD11
T11	SMD03	U01	OSDMAREQ0	U08	VSS	U15	SMD13
T12	VDD	U02	VSS	U09	VDD	U16	SMD14
T13	VSS	U03	SYNTH_LE1	U10	VSS	U17	SMA01

5 Specifications

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
V_{EE}	Voltage at Core	-0.18 to 2.0	V
V_{DD}	DC Supply (I/O)	-0.3 to 3.9	V
V_{IN}	Input Voltage	-0.1 to Vdd + 0.3	V
I_{IN}	DC Input Current	+/- 10	µA
T_{STGP}	Storage Temperature Range	-40 to 125	°C

Table 4. Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD} Vee	DC Supply	3.15 to 3.60 (3V I/O) 1.6 to 2.0 (core)	V
XTALIN	Input frequency	44 or 48	MHz
F_{TCK}	JTAG clock frequency	0 to 10	MHz
T_A	Ambient Temperature	0 to +70	°C
T_J	Junction Temperature	0 to +105	°C

Notes:
1. The XTALIN & XTALOUT pins have minimal ESD protection.
2. This device may have ESD sensitivity above 500V HBM per JESD22-A114. Normal ESD precautions need to be followed.

Table 5. Capacitance

Symbol	Parameter	Value	Units
C_{IN}	Input Capacitance	3.4	pF
C_{OUT}	Output Capacitance	4.0	pF

Table 6. DC Characteristics

Symbol	Parameter	Condition	Min	Typ.	Max	Units
V_{IL}	Voltage Input Low		-0.50		0.3 * V_{DD}	V
V_{IH}	Voltage Input High		0.7 * V_{DD}		V_{DD} + 0.3	V
V_{OL}	Voltage Output Low	I_{OL} = 800 µA			V_{SS} + 0.1	V
V_{OH}	Voltage Output High	I_{OH} = 800 µA	V_{SS} - 0.1			V
I_{IL}	Input Leakage Current	V_{IN} = V_{SS} or V_{DD}	-10		10	µA
I_{OZ}	3-State Output Leakage Current	V_{OH} = V_{SS} or V_{DD}	-10		10	µA
I_{DD} I_{EE}	Dynamic Supply Current Note 1	V_{DD} = 3.3V V_{DD} = 1.8V		22 123		mA

5.1 AC Characteristics and Timing

Table 7. System Memory Interface Timings

Parameter	Parameter Description	Min	Max	Units
t_dSMD	SMCLK to SMD[31:0] output delay		7	ns
t_dSMA	SMCLK to SMA[11:0] output delay		4.7	ns
t_dSMDQM	SMCLK to SMDQM[3:0] output delay		5.1	ns
t_dSMNCS	SMCLK to SMNCS[1:0] output delay		4.1	ns
t_dSMNWE	SMCLK to SMNWE output delay		4.5	ns
t_dSMCKE	SMCLK to SMCKE output delay		4.3	ns
t_dSMNCAS	SMCLK to SMNCAS output delay		4.0	ns
t_dSMNRAS	SMCLK to SMNRAS output delay		5.0	ns
T_{per}SMCLK	SMCLK period	72	103	ns
T_{su}SMD	SMD[31:0] setup to SMCLK	1.0		ns
T_hSMD	SMD[31:0] hold from SMCLK	2.4		ns

Notes:

1. Outputs are loaded with 35pf on SMD, 25pf on SMA, SMDQM, SMNRAS, and SMNCAS and 20pf on SMCLK, SMNCS, and SMCKE.
2. An attempt has been made to balance the setup time needed by the SDRAM and the setup needed by CS22210 to read data. If there is a problem meeting setup on the SDRAM, there is a programmable delay line on SMCLK which can help meet the setup time. Care must be taken, however, not to violate the setup on the return read data. The delay can be increased by a multiple of 0.25ns by using the SMA[11:09] pins to selectively set the clock delay.

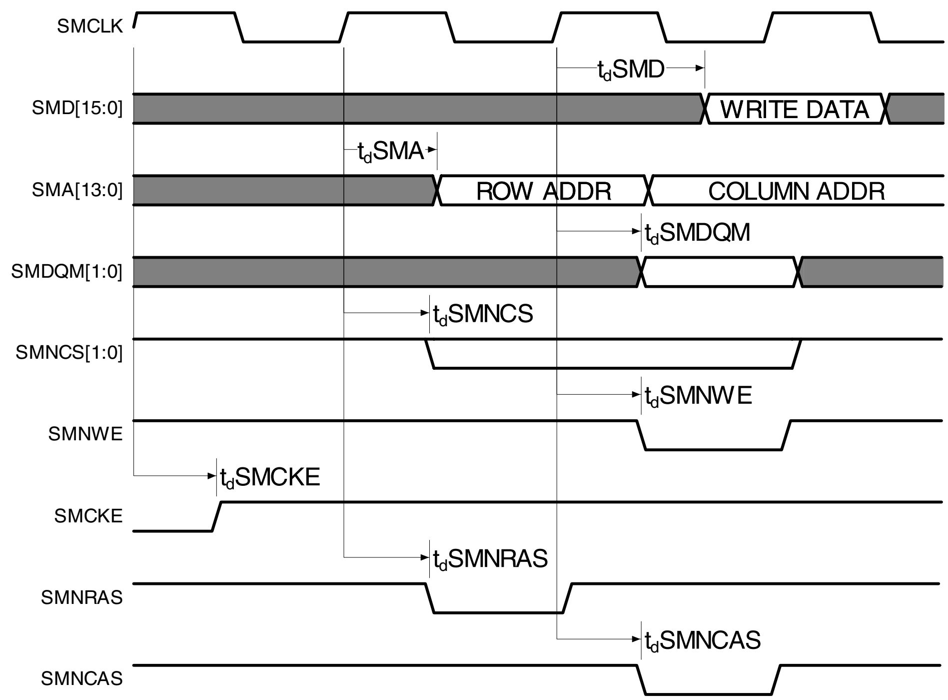


Figure 5. System Memory Interface 'Write' Timing Diagram

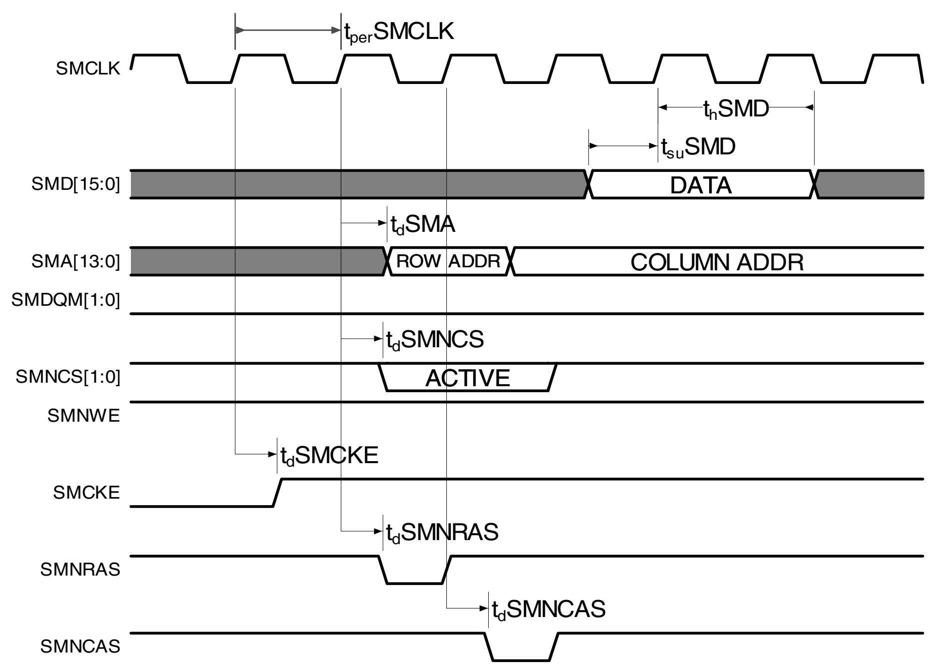


Figure 6. System Memory Interface 'Read' Timing Diagram

Table 8. ROM/Flash Memory Read Timing

Item	Symbol		
		Min	Max
Clock Period [1]	t_{per}SMCLK	72 MHz	103 MHz
$\overline{CE}$ to SMD Latched Data [2]	t_{id} SMD		221 ns
$\overline{OE}$ de-asserted to OE asserted [3]	t_f SMRAS	6(t_{per}SMCLK)	
ROM address to output delay [4]	t_{ACC}		220 ns
SMCLK to SMA output delay	t_d SMA		4.0 ns
SMCLK to BRCE output delay ($\overline{CE}$)	t_d BRCE		4.5 ns
SMCLK to SMRAS output delay ($\overline{OE}$)	t_d SMRAS		5.0 ns
SMD setup to SMCLK	t_{su} SMD	1.0 ns	
SMD hold from SMCLK	t_h SMD	2.4 ns	

1. The memclock timing is derived by bootstrap PLL settings. Synchronous modes at 77 MHz & 72 MHz are currently supported.
2. t_{id} SMD is based on the fm_romrdlat register settings – default is 09h max. (77Mhz ~ 17 times SMCLK = 221ns).
3. t_f SMRAS is the minimum time required before the next OE is active on the bus (6 times SMCLK). The ROM device must release the bus within this time frame (77MHz ~ 78 ns).
4. Based on default fm_romrdlat register settings (note: 09h translates to 11h) *see fm_romrdlat register settings for more information.*

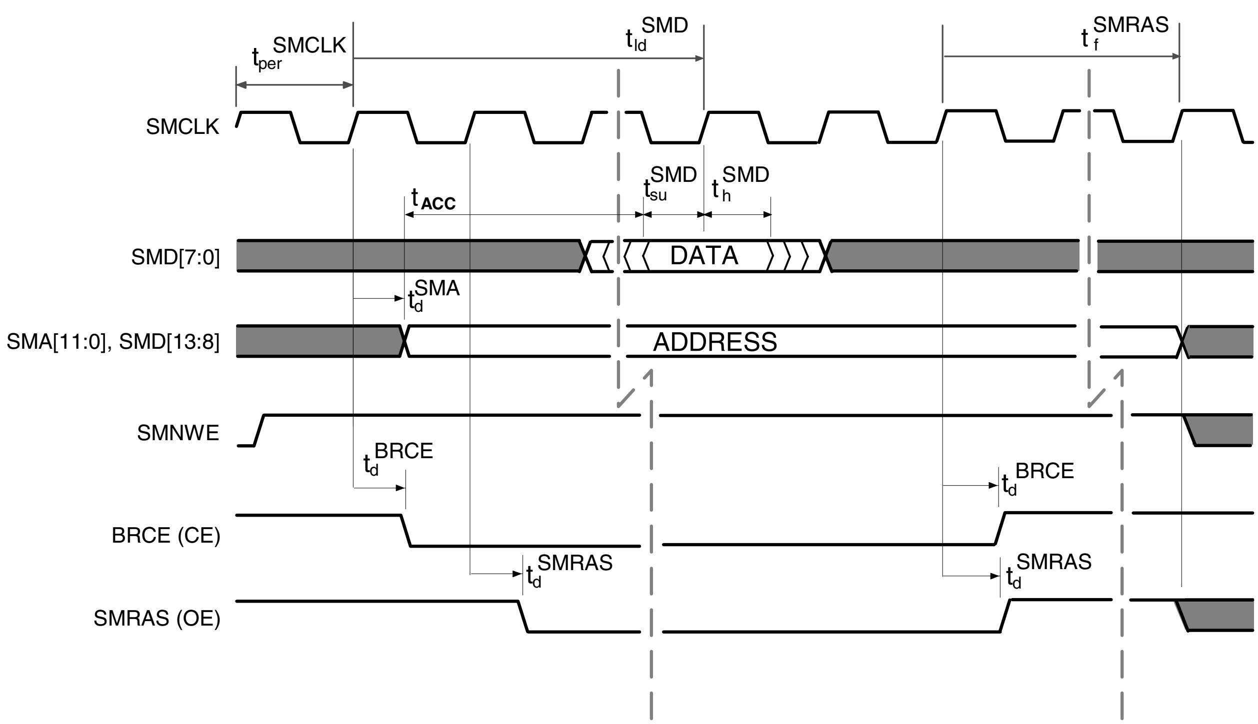


Figure 7. ROM Memory Interface 'Read' Timing Diagram

Table 9. USB Interface Timings

Parameter	Description	Min	Max	Units
USBVPX	Differential data positive	4	20	ns
USBVPM	Differential data negative	4	20	ns

Table 10. Radio MAC AC Timings – Intersil Modes

Parameter	Parameter Description	Min	Max	Units
t_dBBAS	BBAS output delay from falling BBSCLK		8.2	ns
t_dBBRNW	BBRNW output delay from falling BBSCLK		8.0	ns
t_dnBBCS	nBBCS output delay from falling BBSCLK		59.0	ns
t_dBBSDX	BBSDX output delay from falling BBSCLK		7.0	ns
T_{su}BBSDX	BBSDX setup to rising edge of BBSCLK	14.8		ns
T_hBBSDX	BBSDX hold from rising edge of BBSCLK	0.0		ns
t_dTXD	TXD output delay from rising TXCLK (SMAC Mode)		33.5	ns
t_dTXD	TXD output delay from rising TXCLK (RMAC Mode)		15.4	ns
T_{su}RXD	RXD setup to rising edge of RXCLK	1.0		ns
T_hRXD	RXD hold from rising edge of RXCLK	1.8		ns
T_{su}MDRDY	MDRDY setup to falling edge of RXCLK	2		ns
T_hMDRDY	MDRDY hold from falling edge of RXCLK	1		ns
t_dTXPEBB	TXPEBB output delay from rising TXCLK		15.0	ns
t_dRXPEBB	RXPEBB output delay from rising RXCLK		16.0	ns
T_{su}TXRDY	TXRDY setup to falling edge of TXCLK	6.5		ns
T_hTXRDY	TXRDY hold from falling edge of TXCLK	0		ns
T_{duty}RXCLK [2]	RXCLK period	See Note		ns
T_{duty}TXCLK [2]	TXCLK period	See Note		ns

Notes:

1. CCA signal is double synchronized to ARMCLKIN.
2. ARMCLK must be at least 4 times the TXCLK and RXCLK frequency.
3. Harris baseband (3824/3824A) generates RXCLK and TXCLK of 4 Mhz. the duty cycle varies between 33-40% with a high time of 90.9ns and low time that alternates between 136 and 182ns. The clock period varies between 227 and 272 ns, giving an effective period of 250ns.
4. TXD delay in 802.11b mode is the result of sampling the TXCLK with the ctlclk, therefore the maximum delay is equal to two ctlclk periods plus the flop-to-output delay. In this table, ctlclk is assumed to have a 13 ns period.
5. BBNCS output delay = [(1/ARMCLK freq)*ceiling(SER_CLK_DIV/2)] + 7ns, the specified value is based on ARMCLK of 77 Mhz and SER_CLK_DIV=8.

Table 11. Radio MAC AC Timings – RFMD Modes

Parameter	Parameter Description	Min	Max	Units
t_dBBRNW	BBRNW output delay from falling BBSCLK		6.7	ns
t_dnBBCS	nBBCS output delay from falling BBSCLK		110.79	ns
t_dBBSDX	BBSDX output delay from falling BBSCLK		7.0	ns
T_{su}BBSDX	BBSDX setup to rising edge of BBSCLK	14.5		ns
T_hBBSDX	BBSDX hold from rising edge of BBSCLK	0.0		ns
t_dTXD	TXD output delay from rising TXCLK (SMAC Mode)		33.5	ns
t_dTXD	TXD output delay from rising TXCLK (RMAC Mode)		15.4	ns
T_{su}RXD	RXD setup to rising edge of RXCLK	1.0		ns
T_hRXD	RXD hold from rising edge of RXCLK	1.8		ns
T_{su}MDRDY	MDRDY setup to falling edge of RXCLK	2		ns
T_hMDRDY	MDRDY hold from falling edge of RXCLK	1		ns
t_dTXPEBB	TXPEBB output delay from rising TXCLK		15.0	ns
t_dRXPEBB	RXPEBB output delay from rising RXCLK		16.0	ns
T_{su}TXRDY	TXRDY setup to falling edge of TXCLK	6.5		ns
T_hTXRDY	TXRDY hold from falling edge of TXCLK	0		ns

Notes:

1. CCA signal is double synchronized to ARMCLKIN.
2. ARMCLK must be at least 4 times the TXCLK and RXCLK frequency.
3. TXD delay in 802.11b mode is the result of sampling the TXCLK with the ctlclk, therefore the maximum delay is equal to two ctlclk periods plus the flop-to-output delay. In this table, ctlclk is assumed to have a 13 ns period.
4. BBNCS output delay = [(1/ARMCLK freq)*ceiling(SER_CLK_DIV/2)] + 7ns, the specified value is based on ARMCLK of 77 Mhz and SER_CLK_DIV=8.

Table 12. Package Specifications

Symbol	Parameter	Value	Units
θ_{JC}	Junction-to-Case Thermal Resistance	2.5	°C/W
θ_{JA}	Junction-to-Open Air Thermal Resistance	26.9	°C/W
T_{J_MAX}	Max Junction Temperature	105	°C

Notes:

1. ARMCLK / MEMCLK = 77MHz

6 Packaging

The CS22250 controller is available in a 208 Fine Pitch Ball Grid Array (FPBGA) package. Figure 8 contains the package mechanical drawing.

Figure 8. CS22250 FPBGA-pin Mechanical Drawing