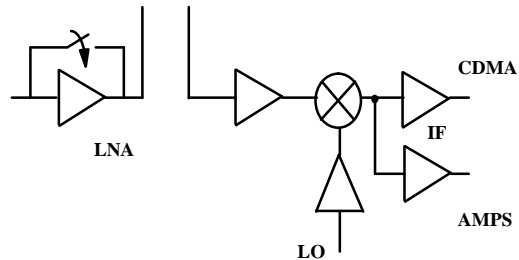# TriQuint ® SEMICONDUCTOR

CMH82

Preliminary Datasheet

- High-Linearity, Cellular LNA/Mixer IC for use in TDMA and CDMA Mobile Phones
- Integrated bypass switch for LNA
- GaAs PHEMT Process
- Leadless 3.5 x 3.5 mm. SMT package
- LO Input power range: -12.0 to 0 dBm
- Operating voltage range: 2.7 to 4 V
- Total current consumption: 20 mA
- Adjustable Mixer Gain and IP3

ESD: **E**lectro**s**tatic **d**ischarge sensitive device
      Observe handling Precautions!

Type	Marking	Ordering code (tape and reel)	Package
CMH82	**H82**	**TBD**	**VQFN-20**

Maximum Ratings	Symbol	Value		Unit
		min	max	
Supply Voltage	V_{DD}	0	4	V
DC-Voltage at RF Ports	V_{RF}	- 0.3	0.3	V
DC-Voltage at GND Ports	V_{GND}	- 0.3	0.3	V
DC-Voltage at CNTL Ports	V_{CNTL}	0	$0.3 + V_{DD}$	V
Power into LO Input	$P_{in,LO}$		10	dBm
Operating Temperature	T_a	-40	85	°C
Channel Temperature	T_{Ch}		150	°C
Storage Temperature	T_{stg}	-55	150	°C

Thermal Resistance			
Channel to Soldering Point (GND)	R_{thChS}	102	°C /W

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Electrical Characteristics

Parameter,	min	typ	max	Unit
RF - Frequency	869	-	894	MHz
LO - Frequency [1]	919	-	1194	MHz
IF Frequency range	50	-	300	MHz
LO Power Input	-12.0	-	0.0	dBm
Supply Voltage (Vdd)	2.7	-	4.0	V
High Logic Level (H)	2.4	2.7	$0.3 + V_{DD}$	V
Low Logic Level (L)	0.0	-	0.3	V

1) Low-side LO can be achieved using external tuning

<u>LNA</u> – Performance of LNA:

Test conditions: T_a = 25°C, V_{DD}= 2.7 V, f_{RF} = 869 - 894 MHz

Mode – High Gain, High Linearity	min	typ	max	Unit
Operating Current		6.5		mA
Noise Figure		1.1		dB
Gain		12.5		dB
Input / Output return loss		10		dB
3rd Order Input Intercept Point		10.0		dBm
Mode – High Gain, Reduced Current	**min**	**typ**	**max**	**Unit**
Operating Current		4.5		mA
Noise Figure		1.2		dB
Gain		12.3		dB
Input / Output return loss		10		dB
3rd Order Input Intercept Point		8.0		dBm
Mode – Low Gain, By-Pass Mode	**min**	**typ**	**max**	**Unit**
Operating Current		0		mA
Noise Figure		4.5		dB
Gain		-4.5		dB
Input / Output return loss		10		dB
3rd Order Input Intercept Point		25		dBm

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MIXER - Electrical Characteristics of Mixer section

Test conditions: T_a = 25°C; V_{DD}= 2.7V, P_{LO} = -10 dBm, $f_{LO} = f_{RF} + f_{IF}$, f_{IF} = 85MHz

Mode – High Gain, High Linearity CDMA	min	typ	max	Unit
Operating Current		13.5		mA
Conversion Gain[1]		15.5		dB
Noise Figure		4.5		dB
3rd Order Input Intercept Point		6.5		dBm
RF Input return loss		10		dB
LO Input return loss		10		dB
IF Output Impedance [2]		695+j*135		Ω
Mode – Reduced Current CDMA	**min**	**typ**	**max**	**Unit**
Operating Current		11.0		mA
Conversion Gain[1]		15.2		dB
Noise Figure		4.7		dB
3rd Order Input Intercept Point		4.5		dBm
RF Input return loss		10		dB
LO Input return loss		10		dB
IF Output Impedance [2]		695+j*135		Ω
Mode – AMPS	**min**	**typ**	**max**	**Unit**
Operating Current		11		mA
Conversion Gain		13.5		dB
Noise Figure		5.7		dB
3rd Order Input Intercept Point		2.5		dBm
RF Input return loss		10		dB
LO Input return loss		10		dB
IF Output Impedance [2]		172+j*78		Ω

1) CDMA Mixer Gain may be varied from approximately 10 to 20 dB (typical) by choice of external components. See notes.
2) IF Output externally tuned to desired impedance

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FULL CHAIN – LNA / Downconverter Characteristics

Test conditions: T_a = 25 °C, V_{DD}= 2.7 V, P_{LO} = -10 dBm, f_{IF} = 85 MHz

Mode – High Gain, High Linearity CDMA	min	typ	max	Unit
Total operating Current		20		mA
Conversion Gain [1]		25		dB
Noise Figure		1.9		dB
Input IP3		-3.5		dBm
LNA Input IP3		10.0		dBm
Mode – High Gain, Reduced Current CDMA	**min**	**typ**	**max**	**Unit**
Total operating Current		15.5		mA
Conversion Gain [1]		24.5		dB
Noise Figure		2.0		dB
Input IP3		-5		dBm
LNA Input IP3		8.0		dBm
Mode – Low Gain (LNA bypass) CDMA[2]	**min**	**typ**	**max**	**Unit**
Total operating Current		11.0		mA
Conversion Gain [1]		7.7		dB
Noise Figure		12.0		dB
Input IP3		11.5		dBm
Mode – AMPS[2]	**min**	**typ**	**max**	**Unit**
Total operating Current		15.5		mA
Conversion Gain [1]		22.8		dB
Noise Figure		2.3		dB
Input IP3		-6.5		dBm

1) Assumes 3 dB loss for image filter
2) Assumes reduced current mode

Truth Table

	Control Voltage		
Operating Mode	**Mode Ctl**	**Gain Ctl**	**Rcv Only**
High Gain & Linearity	H	H	H
High Gain, Low Current	H	H	L
Low Gain (LNA bypass)	H	L	L
AMPS	L	H	L

PIN Assignments & Functional Block Diagram
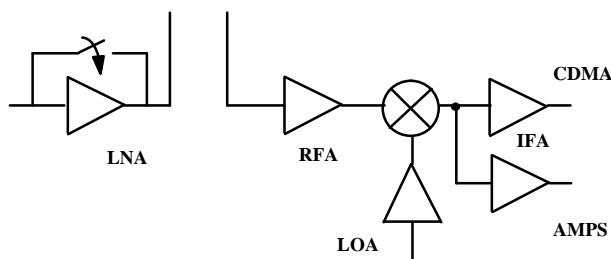
| PIN	Symbol	Description
1	LO in	Mixer LO Input
2	GND	Ground
3	LO Vdd	Supply voltage for LO Buffer Amp
4	Mix out	Mixer output to IF Amplifier
5	AMPS in	AMPS IF Amplifier input
6	CDMA in	CDMA IF Amplifier input
7	GND	Ground
8	Ifa src	IF Amplifier FET source ground
9	CDMA out	CDMA IF output
10	AMPS out	AMPS IF output
11	Mode	AMPS or CDMA IF mode control
12	RFA in	Downconverter input from image filter
13	RFA Vdd	Supply voltage for RFA
14	Vdd	Supply voltage
15	LNA Vdd	Supply voltage for LNA
16	LNA out	Output of LNA
17	GND	Ground
18	LNA in	RF Input to LNA
19	Rcv	Reduced current mode control
20	Gctl	Control voltage for LNA gain selection

Application Circuit
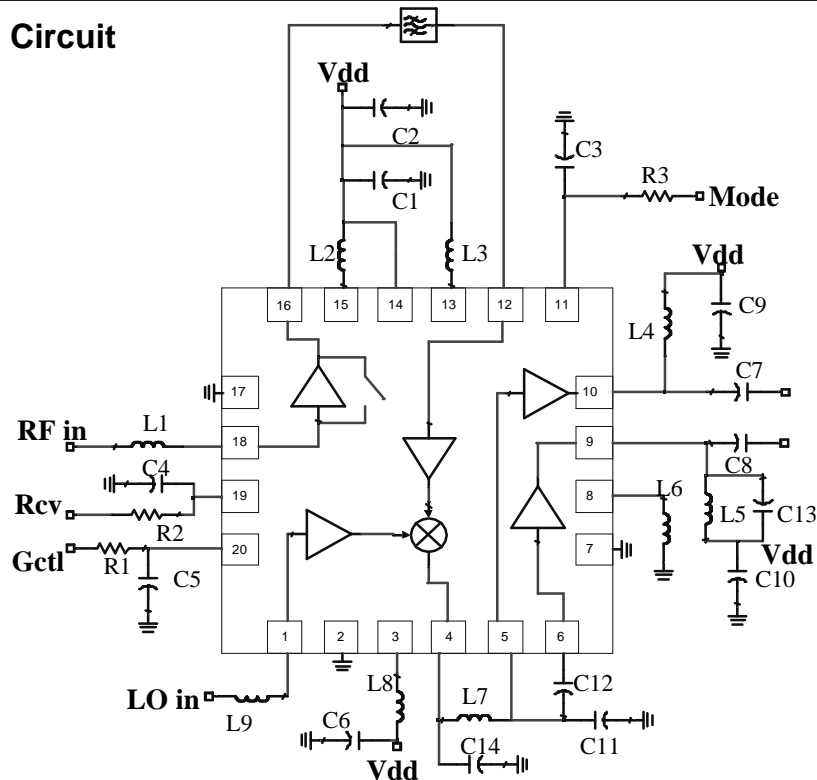
External Components

Component values for IF = 85 MHz. LO = RF +IF .

Component	Description	Package Type		Component	Description	Package Type
C1	CAP, 47 PF	0402		L1	IND, 19 NH	0402
C2	CAP, 10K PF	0402		L2	IND, 12 NH	0402
C3	CAP, 100 PF	0402		L3	IND, 12 NH	0402
C4	CAP, 47 PF	0402		L4	IND, 330 NH	0805
C5	CAP, 47 PF	0402		L5	IND, 270 NH	0603
C6	CAP, 1000 PF	0402		L6	IND, 220 NH	0603
C7	CAP, 18 PF	0402		L7	IND, 270 NH	0603
C8	CAP, 10 PF	0402		L8	IND, 18 NH	0402
C9	CAP, 10K PF	0402		L9	IND, 12 NH	0402
C10	CAP, 10K PF	0402				
C11	CAP, 12 PF	0402		R1	RES, 47 KOHM	0402
C12	CAP, 100 PF	0402		R2	RES, 47 KOHM	0402
C13	CAP, 3.3 PF	0402		R3	RES, 47 KOHM	0402
C14	CAP, 0.5 PF	0402				

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Package Outline - VQFN 20
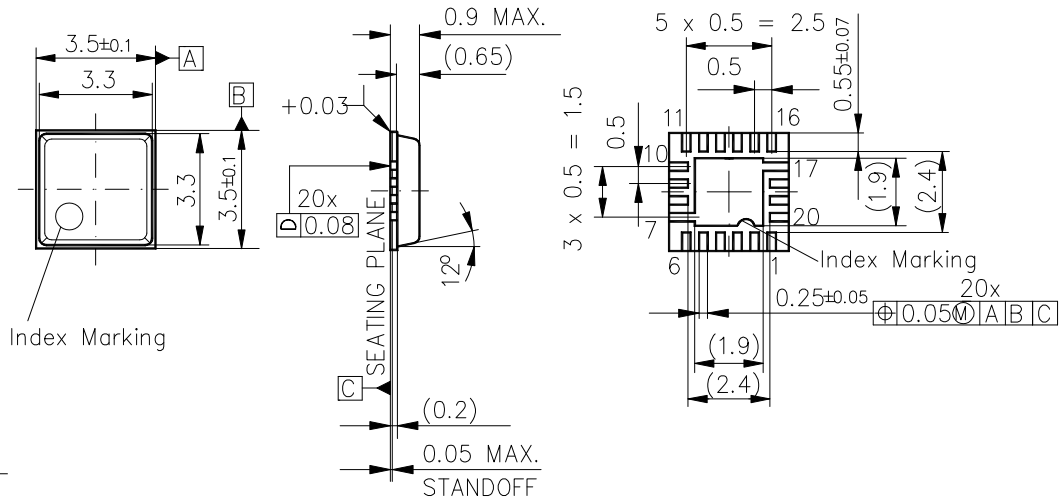
Recommended PCB Layout

CMH82

Evaluation Board

2000 (mil)

2000 (mil)
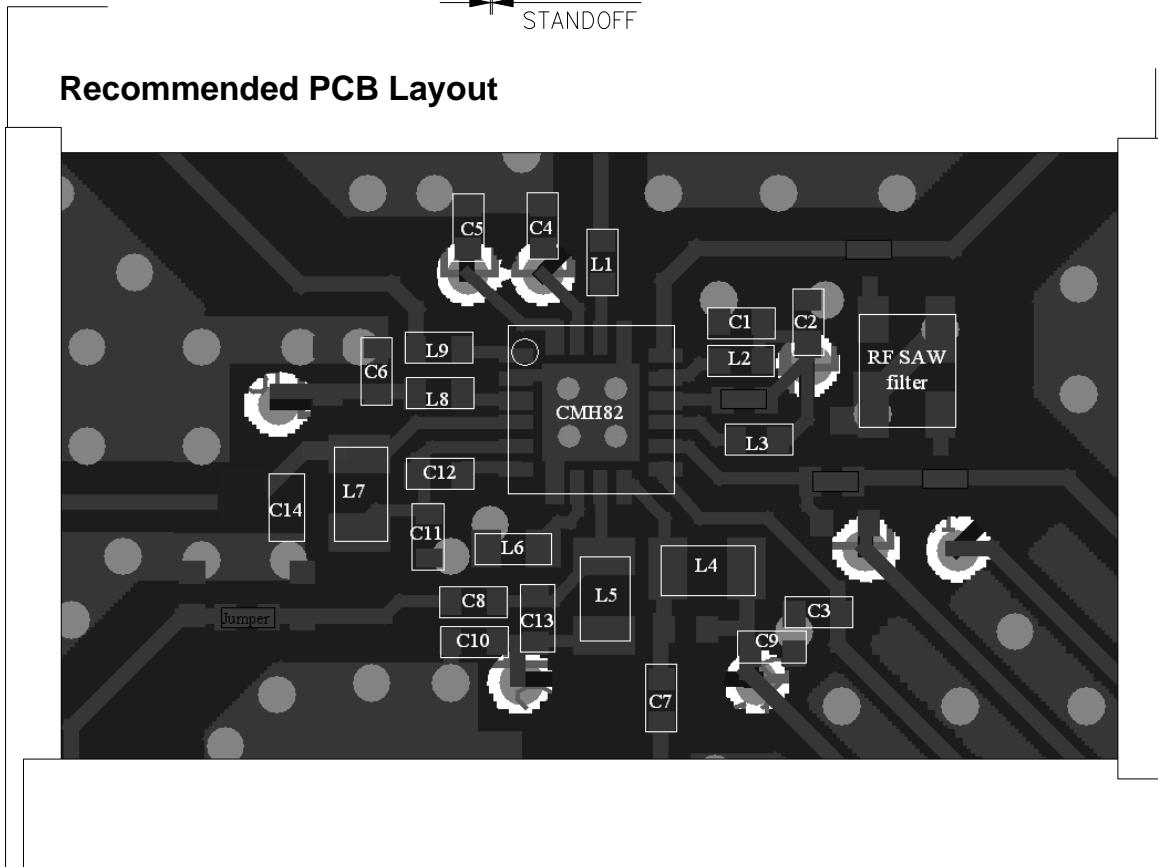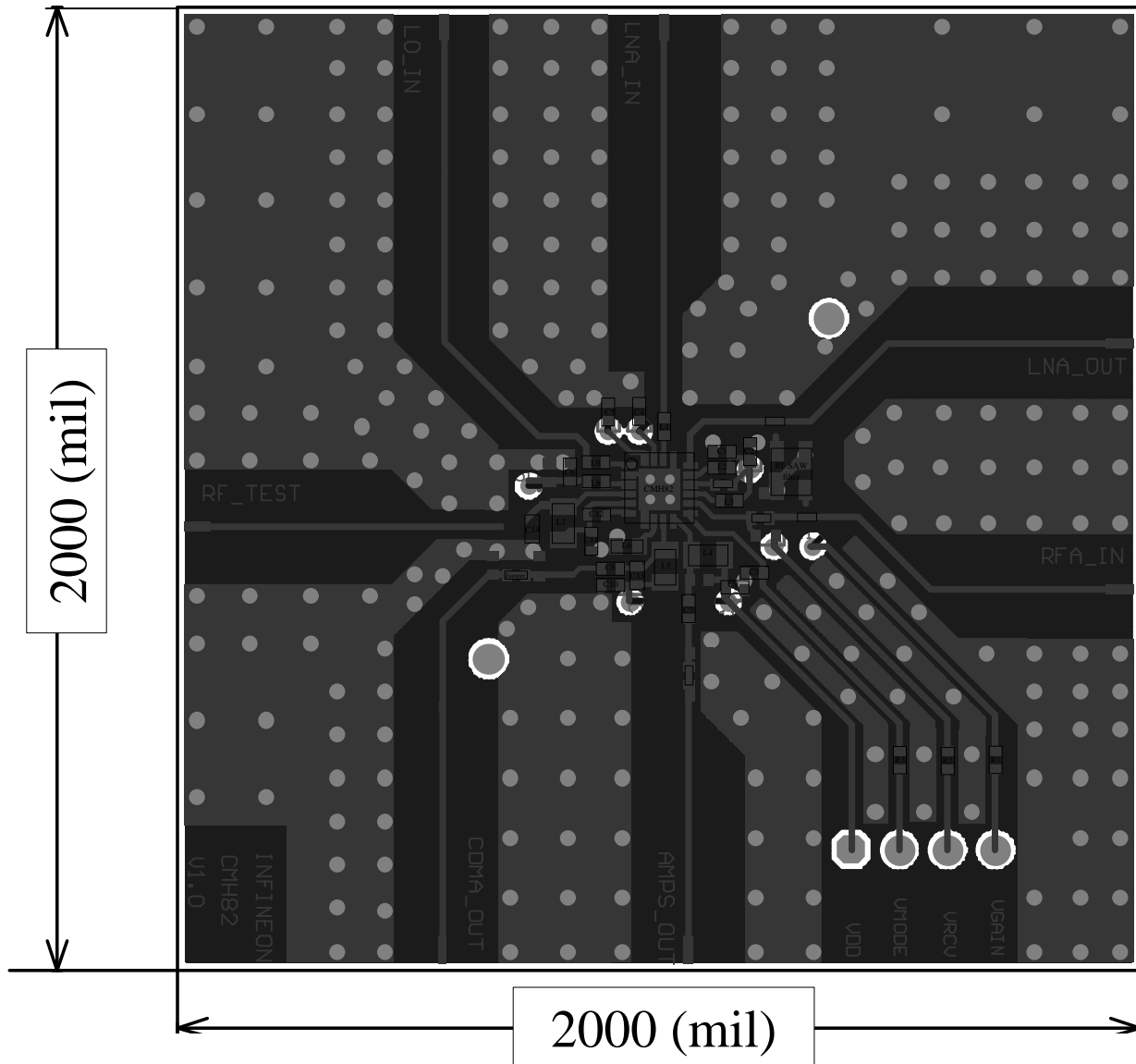
CMH82 – Application Information

DC Biasing:

Supply Voltage.
    One regulated voltage source is needed for CMH82. On the evaluation board, it is labeled VDD.

Minimum LO Power for Proper Biasing
    For proper biasing of the CMH82, a minimum LO input power is required. If the part is turned ON without any LO drive applied, all currents will be extremely high. The minimum LO required is approximately –12 dBm. Operation with LO input powers below the minimum value causes the current to increase in all amplifier stages. For higher LO input power levels the current stays relatively constant over a wide range of LO powers. Proper matching of the LO amplifier is also important to achieve the lowest current consumption and to minimize the required LO input power.

Adjustable Current Level
    The CMH82 can operate in two different current/linearity modes: High Linearity (with higher current) and Reduced Current (lower linearity). To operate with reduced current the voltage on pin 19 (RCV) should be set LOW. Some additional current reduction can be achieved by reducing the voltage at pin 14 by inserting a resistor between VDD and pin 14. The current pulled by pin 14 is approximately 1 mA. Higher currents can be realized by using a higher VDD voltage.

Tuning LO and IF Amplifiers:

    The CMH82 can be tuned to utilize either high or low side LO frequencies and allows a wide range of IF frequencies. Depending on the chosen frequency plan the off chip components for the LO and IF amplifiers will need to be optimized. An application circuit with all component values is provided for high side LO injection with IF frequency of 85 MHz (RF freq 869 – 894 MHz).

    Two external components (L9 and L8) are required for tuning the LO. L8 is critical for setting the minimum current and to achieve the constant DC current over the operating band. L9 sets the input match.

    Components L7, C11 and C12 form the input match for the IF amplifiers and will vary depending on the chosen IF frequency. The inductor on pin 8 allows adjustment to the gain of the IF amplifiers. Output matching components shown in the application circuit provide a transformation for a 50 Ohm load impedance. The output impedance for the CDMA IFA (looking into pin 9) at 85 MHz is approximately (695 + j*135) Ohms. The AMPS output impedance is approximately (172 + j*78) Ohms at 85 MHz.

Downconverter Gain Adjustment:

The **Downconverter gain can be adjusted by changing the source feedback inductor L6 for the IFA**. Higher inductance will give lower downconverter gain and typically improve the IIP3.

Gain/Current Control Pins:

LOW = 0 to 0.3 V
HIGH = Vdd to (Vdd – 0.3) V

VGAIN – select between high and low gain states in the LNA.
        VGAIN = HIGH : LNA ON (~12 dB Gain, ~ 6 mA current)
        VGAIN = LOW   : LNA bypassed (~ 4 dB Loss, no current)

VRCV - selects Current/Linearity mode (changes current in LNA/RFA/IFA)
        VRCV = LOW   selects Reduced Current Mode
        VRCV = HIGH   selects High Linearity Mode.

VMODE - selects which IF amplifier is ON
        VMODE = LOW   selects AMPS mode
        VMODE = HIGH   selects CDMA mode

Other Notes:

Inductor L1 is critical for setting the Noise Figure of the LNA. A high Q wire wound inductor (e.g. Coilcraft) is recommended to achieve minimum NF.

LNA current can be determined by subtracting the current in Low Gain mode from the current in High Gain mode (keeping VRCV and VMODE constant).

Capacitor C14 can be eliminated if a slightly higher (~0.5 dB) downconverter noise figure is tolerable.

Control lines (G_CNTL, VRCV and VMODE) have an input impedance of > 1 MΩ when Vdd is ON. When VDD is off, they have approximately 20 KΩ input impedance.