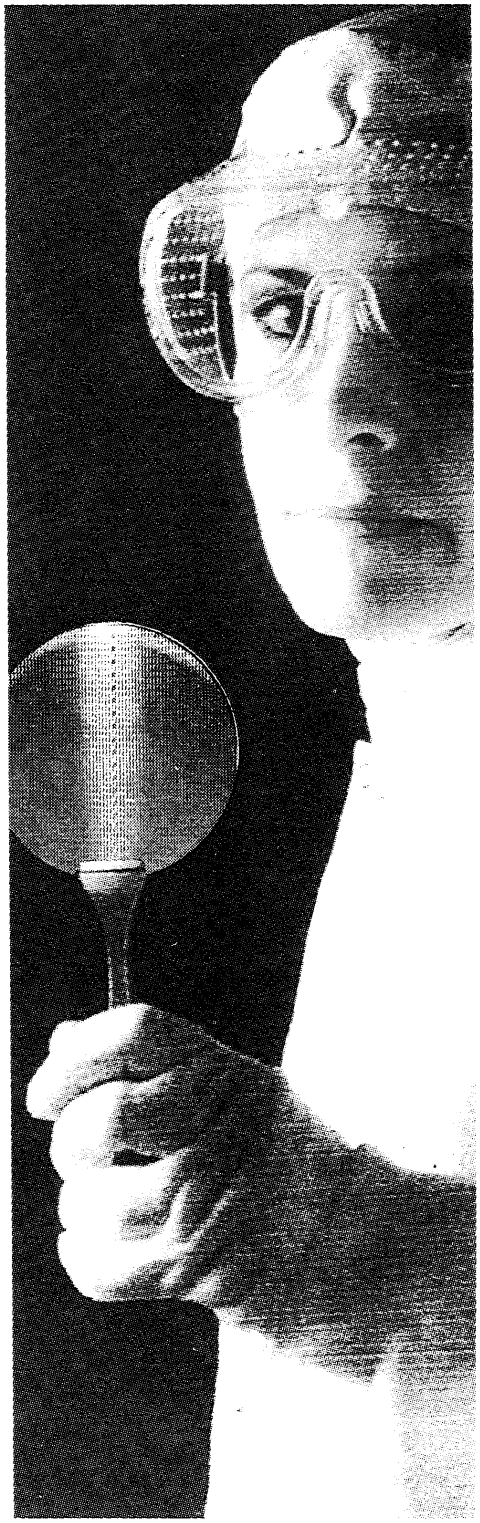
CF004 Series GaAs Pseudomorphic HEMT and MESFET Chips



- ❑ **Super Low Noise: 1.5 dB at 18 GHz**
- ❑ **High Gain: Usable to 44 GHz**
- ❑ **Flat Gain for Distributed Amplifiers**
- ❑ **Active Layers Include: Pseudomorphic HEMT, Epitaxial and Ion Implanted**
- ❑ **Wafer Qualification Procedure**
- ❑ **Customer Wafer Selection Available**

Celeritek CF004 Series Chips

Celeritek CF004 Series chips are GaAs based transistors which include the CF004-01, CF004-02 and CF004-03 models. They are 150 µm gate width, sub-half-micron gate length GaAs devices with Celeritek's proprietary Silicon Nitride passivation.

Celeritek's Wafer Qualification Procedure for CF004 Series FETs consists of DC, RF and reliability testing of both individual die and generic 6 to 18 GHz amplifier modules.

The CF004-01 provides unusually high gain in narrow- and wide-band applications up to 40 GHz. For example, 9 dB of gain is achievable in a 6 to 18 GHz balanced amplifier circuit; 5 dB of gain can be realized in an 18 to 40 GHz circuit.

The CF004-03 model is Celeritek's state-of-the-art GaAs Pseudomorphic HEMT device. It provides the lowest noise and highest gain attainable above 18 GHz. Its rugged construction allows it to withstand the same input power as conventional MESFETs.

All CF004 Series devices exhibit extraordinarily flat S_{21} vs frequency making them excellent for distributed amplifier circuits. These devices are available in chip form and are suitable for airborne, shipboard and ground-based equipment. Screening includes MIL-STD-750 Class B, Class S and commercial screening.

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CF004 Series GaAs Chips

Specifications (T_A = 25°C)				CF004-01			CF004-02			CF004-03		
Active Layer				Ion Implanted			Epitaxial			Pseudomorphic HEMT		
Symbol	**Parameters and Conditions**	**Frequency (GHz)**	**Units**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
NF_{opt}	Optimum Noise Figure V_{DS} = 3.0 V, I_{DS} = 10 mA	18.0	dB		2.2	3.0		1.8	2.4		1.5	2.0
Ga	Gain at NF_{opt} V_{DS} = 3.0 V, I_{DS} = 10 mA	18.0	dB	7.0	8.0		8.0	9.0		9.0	10.0	
$\|S_{21}\|^2$	50 Ohm Insertion Gain V_{DS} = 6.0 V, I_{DS} = 25 mA	2.0 10.0 18.0 26.0	dB dB dB dB		8.0 8.0 7.0 3.0			9.0 9.0 8.0 4.0			10.0 10.0 9.0 5.0	
P_{1dB}	Power Output @ 1 dB GC V_{DS} = 6.0 V, I_{DS} = 25 mA	12.0	dBm		15.0			13.0			13.0	
g_m	Transconductance V_{DS} = 3.0 V, V_{GS} = 0 V		mS		30			40			45	
I_{DSS}	Drain Current V_{DS} = 3.0 V, V_{GS} = 0 V		mA	20	30	60	15	30	60	15	30	60
V_P	Pinchoff Voltage V_{DS} = 3.0 V, I_{DS} = 1 mA		Volts	-0.7	-1.3	-2.5	-0.5	-1.3	-2.5	-0.5	-1.3	-2.5
BV_{GD}	Breakdown Voltage, Gate-Drain I_{GD} = 100 µA		Volts	-5.5	-8.0		-5.5	-8.0		-5.5	-8.0	
R_{th}	Thermal Resistance		°C/W		300			300			300	

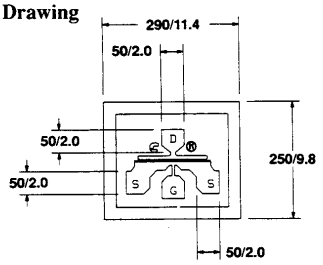
Absolute Maximum Ratings

Parameter	Symbol	Ratings
Drain-Source Voltage	V_{DS}	8V
Gate-Source Voltage	V_{GS}	-5V
Drain Current	I_{DS}	I_{DSS}
Continuous Dissipation	P_T	400 mW
Channel Temperature	T_{CH}	175°C
Storage Temperature	T_{STG}	-65°C to +175°C

Typical Noise Parameters - CF004-03 V_{DS} = 3.0 V, I_{DS} = 10 mA

Frequency (GHz)	NF opt (dB)	Ga (dB)	Gamma opt (Mag)	Gamma opt (Ang)	Rn/50
2.0	0.44	18.9	0.94	4	1.60
4.0	0.55	16.7	0.86	9	1.10
6.0	0.67	14.9	0.78	17	0.81
8.0	0.80	13.6	0.72	28	0.64
10.0	0.93	12.5	0.66	41	0.54
12.0	1.08	11.8	0.60	52	0.46
14.0	1.23	11.1	0.53	62	0.39
16.0	1.40	10.6	0.43	72	0.32
18.0	1.57	10.1	0.32	86	0.25
20.0	1.75	9.6	0.22	110	0.20
22.0	1.94	9.0	0.16	146	0.17
24.0	2.14	8.3	0.19	-171	0.17
26.0	2.35	7.4	0.26	-152	0.19

Chip Outline Drawing



CF004 CHIP (UNITS IN MICRONS/MILS)
THICKNESS: 110 MICRONS/4.3 MILS

Die Attach and Bonding Procedures

Die Attach: Conductive epoxy or eutectic die attach is recommended. For eutectic die attach: Preform: AuSn (80% Au, 20% Sn); Stage Temperature: 290°C, ±5°C; Handling Tool: Tweezers; Time: 1 min or less.

Wire Bonding: Wire Size: 0.7 to 1.0 mil in diameter (pre-stressed); Thermocompression bonding is preferred over thermosonic bonding. For thermocompression bonding: Stage Temperature: 250°C; Bond Tip Temperature: 150°C; Bonding Tip Pressure: 18 to 40 gms depending on size of wire.

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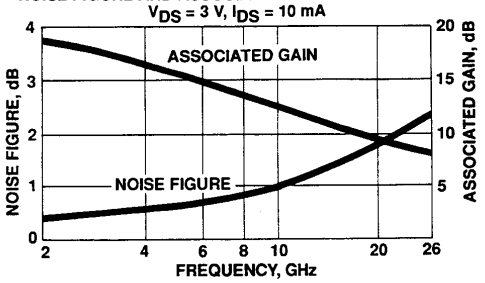
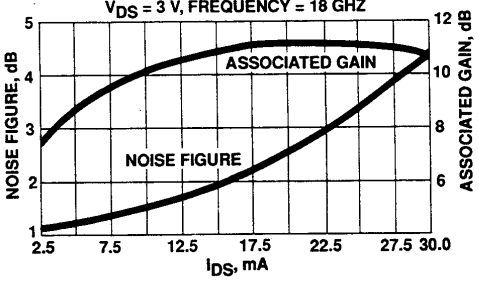
CF004 Series GaAs Chips

Typical Performance (T_A = 25°C)

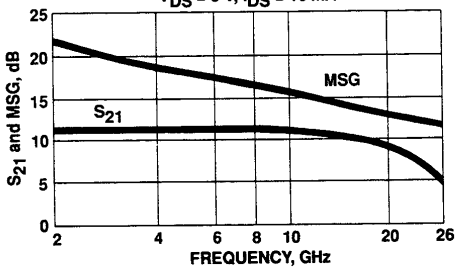
CF004-03
NOISE FIGURE AND ASSOCIATED GAIN vs FREQUENCY
V_{DS} = 3 V, I_{DS} = 10 mA



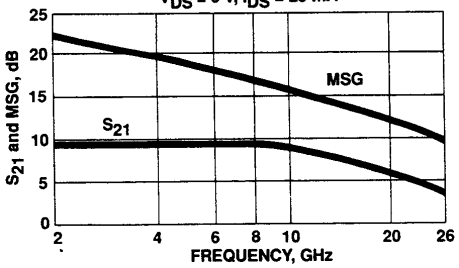
CF004-03
NOISE FIGURE AND ASSOCIATED GAIN vs I_{DS}
V_{DS} = 3 V, FREQUENCY = 18 GHZ



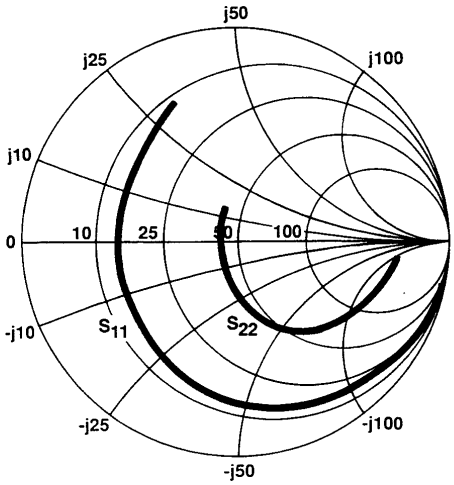
CF004-03
S_{21} AND MSG vs FREQUENCY at LOW NOISE BIAS
V_{DS} = 3 V, I_{DS} = 10 mA



CF004-01
S_{21} AND MSG vs FREQUENCY at POWER BIAS
V_{DS} = 6 V, I_{DS} = 25 mA

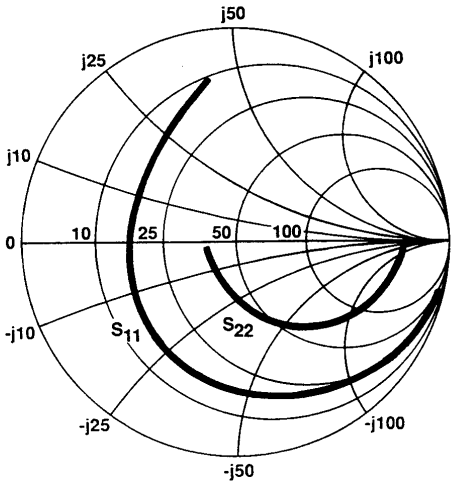


CF004-03
S_{11} AND S_{22} vs FREQUENCY at LOW NOISE BIAS
V_{DS} = 3 V, I_{DS} = 10 mA



FREQUENCY 2.0 to 26.0 GHz

CF004-01
S_{11} AND S_{22} vs FREQUENCY at POWER BIAS
V_{DS} = 6 V, I_{DS} = 25 mA



FREQUENCY 2.0 to 26.0 GHz

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CF004 Series GaAs Chips

Typical Scattering Parameters, Common Source (S-Parameters Include Bonding Wire Parasitics)

CF004-01 at Power Bias V_{DS} = 6 V, I_{DS} = 25 mA

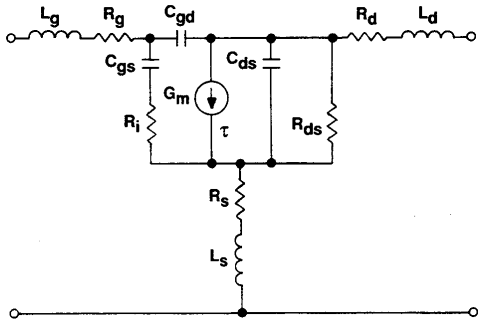
Frequency	S_{11}		S_{21}			S_{12}			S_{22}		K	MSG
(GHz)	(Mag)	(Ang)	(dB)	(Mag)	(Ang)	(dB)	(Mag)	(Ang)	(Mag)	(Ang)		(dB)
2.0	0.97	-14	9.5	2.99	156	-35.3	0.02	78	0.77	-2	0.39	22.4
4.0	0.93	-30	9.7	3.04	150	-29.4	0.03	76	0.76	-7	0.43	19.5
6.0	0.86	-49	9.5	3.00	133	-26.2	0.05	67	0.75	-13	0.57	17.9
8.0	0.77	-73	9.4	2.97	114	-24.2	0.06	58	0.70	-21	0.70	16.8
10.0	0.67	-97	8.9	2.78	95	-23.4	0.07	43	0.65	-30	0.99	16.1
12.0	0.61	-120	8.4	2.62	78	-22.1	0.08	39	0.62	-40	1.00	15.2
14.0	0.55	-142	7.9	2.48	62	-21.3	0.09	34	0.60	-48	1.07	14.6
16.0	0.49	-168	7.5	2.36	47	-20.5	0.09	27	0.57	-54	1.15	14.0
18.0	0.49	157	7.0	2.24	30	-19.3	0.11	19	0.50	-61	1.12	13.1
20.0	0.55	125	6.2	2.05	12	-18.1	0.13	8	0.42	-68	1.06	12.2
22.0	0.66	109	5.1	1.79	-4	-18.1	0.13	1	0.29	-80	1.10	11.6
24.0	0.72	101	3.9	1.56	-17	-17.3	0.14	1	0.18	-105	1.08	10.6
26.0	0.78	98	2.8	1.38	-29	-16.4	0.15	-6	0.14	-164	0.95	9.6

CF004-03 at Low Noise Bias V_{DS} = 3 V, I_{DS} = 10 mA

Frequency	S_{11}		S_{21}			S_{12}			S_{22}		K	MSG
(GHz)	(Mag)	(Ang)	(dB)	(Mag)	(Ang)	(dB)	(Mag)	(Ang)	(Mag)	(Ang)		(dB)
2.0	0.98	-13	11.2	3.62	165	-32.8	0.02	82	0.76	-5	0.23	22.0
4.0	0.94	-26	11.1	3.60	153	-27.0	0.05	74	0.74	-11	0.31	19.1
6.0	0.90	-42	11.0	3.54	138	-23.8	0.06	65	0.71	-19	0.39	17.4
8.0	0.85	-61	11.0	3.53	122	-21.6	0.08	52	0.65	-30	0.47	16.3
10.0	0.77	-80	10.5	3.36	106	-20.5	0.09	37	0.59	-42	0.63	15.5
12.0	0.72	-97	10.2	3.25	91	-19.1	0.11	29	0.56	-54	0.63	14.7
14.0	0.66	-113	10.0	3.18	77	-18.3	0.12	20	0.53	-63	0.70	14.2
16.0	0.59	-136	10.0	3.15	63	-17.4	0.14	8	0.47	-71	0.77	13.7
18.0	0.55	-171	9.8	3.10	45	-16.2	0.16	-4	0.35	-82	0.80	13.0
20.0	0.57	149	9.2	2.89	24	-15.6	0.17	-17	0.20	-89	0.85	12.4
22.0	0.65	123	7.6	2.40	7	-15.9	0.16	-29	0.04	-131	0.93	11.7
24.0	0.68	112	5.9	1.97	-5	-16.5	0.15	-32	0.09	110	1.06	11.2
26.0	0.72	111	4.9	1.76	-13	-16.4	0.15	-35	0.18	111	1.02	10.7

Device Model

Parameters	CF004-01 VDS = 6V, IDS = 25mA	CF004-03 VDS = 3V, IDS = 10mA	Units
L_g	0.41	0.36	nH
R_g	2.0	2.0	Ω
C_{gs}	0.21	0.14	pF
R_i	6.6	2.5	Ω
C_{gd}	0.013	0.019	pF
G_m	38	45	mS
τ	2.2	2.1	ps
C_{ds}	0.060	0.060	pF
R_{ds}	357	359	Ω
R_d	2.7	2.7	Ω
L_d	0.37	0.33	nH
R_s	3.0	2.7	Ω
L_s	0.08	0.08	nH



Wafer Qualification Procedure

- 100% DC Test, 100% Visual Insp.
- Sample Chip Performance Test — NF, Power, S-Parameters, IP3, Power Blast
- Sample Circuit Performance Tests 6-18 GHz Module — NF, Power, Gain, VSWR
- Reliability Assessment — Power Blast & Burn-In

80% of tested samples must meet specifications for wafer acceptance.

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Specifications subject to change.

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