C2910A
Microprogram Controller Megafunction

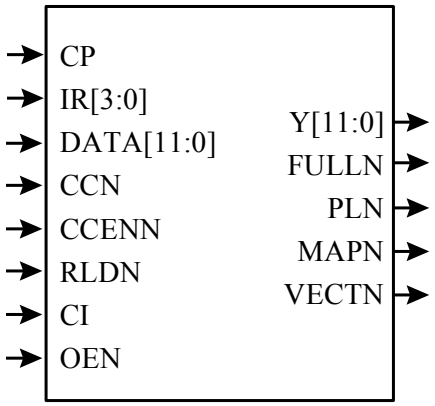
General Description

The C2910A microprogram controller megafunction is an address sequencer that controls the sequence of execution for the microinstructions stored in microprogram memory. The megafunction can sequentially access the microinstructions, and it provides conditional branching to any microinstructions within the 4,096-microword range. In addition, a nine-deep LIFO stack provides a microsubroutine return linkage and looping capability.

Features

- 12-bit data width that addresses up to 4,096 words
- Internal Loop Counter - Pre-settable 12-bit down-counter for repeating instructions and counting loop interactions
- Four Address Sources - Microprogram Address may be selected from microprogram counter, branch address bus, 9-level push/pop stack, or internal holding register
- 16 powerful microinstructions
- Output Enable Controls for Three Branch Address Sources
- Positive-edge-triggered registers
- Also available in VHDL or Verilog
- Functionality based on the Advanced Micro Devices AM2910A

Symbol



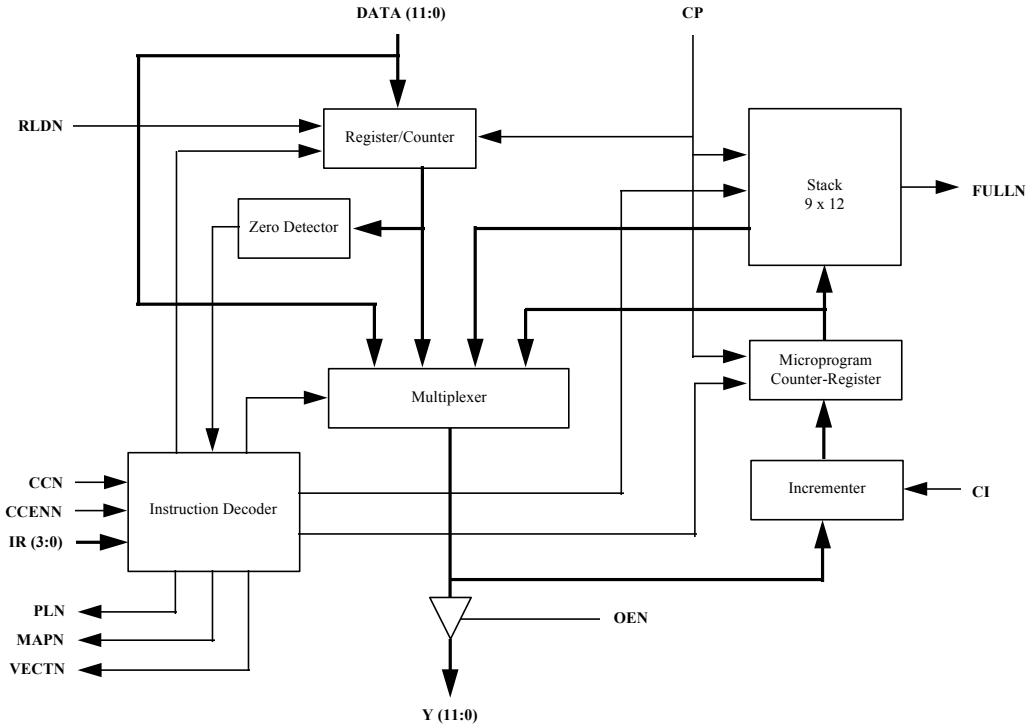
Applications

The C2910A megafunction is used in high-speed bit-slice designs.

Pin Description

Name	Type	Polarity / Bus Size	Description
CP	In	Rising	Clock
IR	In	4	Instruction
DATA	In	12	Direct Data
CCN	In	Low	Condition Code
CCENN	In	Low	Condition Code Enable
RLDN	In	Low	Register Load Enable
CI	In	-	Carry-In
OEN	In	Low	Output Enable
Y	Out	12	Microprogram Address
FULLN	Out	Low	Full Flag
PLN	Out	Low	Pipeline Address Enable
MAPN	Out	Low	Map Address Enable
VECTN	Out	Low	Vector Address Enable

Block Diagram



Functional Description

The C2910A megafunction is partitioned into modules as shown above and described below.

Multiplexer

The four-input multiplexer is used to select either the register/counter, direct input, microprogram counter, or stack as the source of the next microinstruction address.

Register Counter

This block consists of 12 D-type, edge-triggered flip-flops, with a common enable. When its load control, RLDN is low, new data is loaded on a positive clock transition. The output of the register/counter is available to the multiplexer as a source for the next microinstruction address. The direct input furnishes a source of data for loading the register/counter.

Microcontroller Counter/Register (μPC)

This block consists of a 12-bit incrementer followed by a 12-bit register. The μPC can be used in either of two ways: When the carry-in to the incrementer is high, the microprogram register is loaded on the next clock cycle with the current Y output word plus one (Y + 1 → μPC). Sequential microinstructions are thus executed. When the carry-in is low, the incrementer passes the Y output word unmodified so that μPC is reloaded with the same Y word on the next clock cycle (Y → μPC). The same microinstruction is thus executed any number of times.

Stack

This 9-word by 12-bit stack is used to provide return address linkage when executing microsubroutines or loops. The stack contains a built-in stack pointer which always points to the last word written. This allows stack reference operations (looping) to be performed without a pop.

Instruction Decoder

This block decodes the incoming instruction and generates the appropriate control signals for all the other blocks. The instruction decoder block also generates the outputs PLN, MAPN, and VECTN

Verification Methods

The C2910A megafunction's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model which contained the original AMD 2910A chip, and the results compared with the megafunction's simulation outputs.

Device Utilization & Performance

Supported Family	Device Tested	Utilization			Performance
		LEs	Memory	Memory bits	F_{max}
Cyclone	EP1C20-6	294	0	0	139 MHz
Stratix	EP1S20-5	294	0	0	138 MHz
Stratix-II	EP2S60-3	232	0	0	148 MHz

Deliverables

Encrypted Licenses

- Post-synthesis EDIF netlist
- Place & route scripts
- Assignment & Configuration
- Symbol file
- Include file
- Testbench (self-checking)
- Vectors for testing the core
- Documentation

HDL Source Licenses

- VHDL or Verilog HDL source code
- Testbench (self-checking)
- Vectors for testing the core
- Simulation script
- Synthesis script
- Documentation

Megafunction Modifications

The C2910A megafunction can be customized to include:

- Different data width
- Different stack depth

Please contact CAST for any required modifications

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