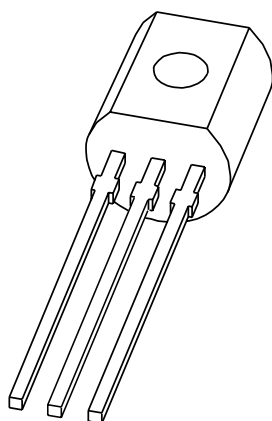# DATA SHEET

BSN254; BSN254A

N-channel enhancement mode vertical D-MOS transistor

Product specification

Supersedes data of 1997 Jun 23

2002 Feb 19

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Semiconductors

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N-channel enhancement mode vertical D-MOS transistor

BSN254; BSN254A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown
- Low R_{DSon}.

APPLICATIONS

- Line current interruptor in telephone sets
- Relay, high-speed and line transformer drivers.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT54 (TO-92) variant package.

PINNING - SOT54 variant

PIN	DESCRIPTION	
	BSN254	BSN254A
1	gate	source
2	drain	gate
3	source	drain

note: various pinnings are available on request

Fig.1 Simplified outline and symbol.
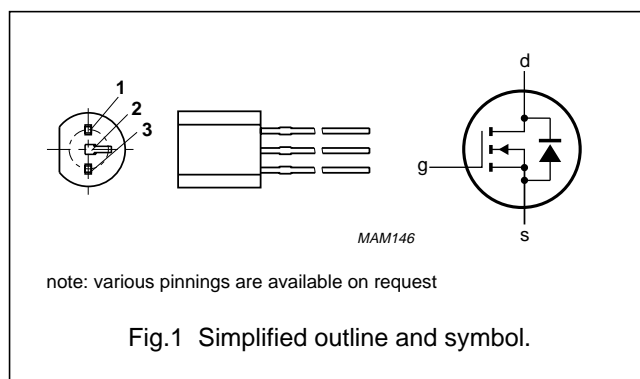
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	250	V
I_D	drain current (DC)		–	310	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\ °C$	–	1	W
R_{DSon}	drain-source on-state resistance	$I_D = 300\ mA$; $V_{GS} = 10\ V$	2.8	5	Ω
V_{GSth}	gate-source threshold voltage	$I_D = 1\ mA$; $V_{DS} = V_{GS}$	–	2	V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	250	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	310	mA
I_{DM}	peak drain current		–	1.25	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\ °C$; note 1	–	1	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on a printed-circuit board; maximum lead length 4 mm; mounting pad for drain lead minimum 10×10 mm.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient; note 1	125	K/W

Note

1. Device mounted on a printed-circuit board; maximum lead length 4 mm; mounting pad for drain lead minimum 10×10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10$ μA; $V_{GS} = 0$	250	–	–	V
I_{GSS}	gate-source leakage current	$V_{GS} = \pm20$ V; $V_{DS} = 0$	–	–	±100	nA
V_{GSth}	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$	0.8	–	2	V
R_{DSon}	drain-source on-state resistance	$I_D = 20$ mA; $V_{GS} = 2.4$ V	–	–	7.5	Ω
		$I_D = 300$ mA; $V_{GS} = 10$ V	–	2.8	5	Ω
I_{DSS}	drain-source leakage current	$V_{DS} = 200$ V; $V_{GS} = 0$	–	–	1	μA
$\mid Y_{fs} \mid$	transfer admittance	$I_D = 300$ mA; $V_{DS} = 25$ V	200	600	–	mS
C_{iss}	input capacitance	$V_{DS} = 25$ V; $V_{GS} = 0$; f = 1 MHz	–	100	120	pF
C_{oss}	output capacitance	$V_{DS} = 25$ V; $V_{GS} = 0$; f = 1 MHz	–	21	30	pF
C_{rss}	feedback capacitance	$V_{DS} = 25$ V; $V_{GS} = 0$; f = 1 MHz	–	10	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$I_D = 250$ mA; $V_{DD} = 50$ V; $V_{GS} = 0$ to 10 V	–	6	10	ns
t_{off}	turn-off time	$I_D = 250$ mA; $V_{DD} = 50$ V; $V_{GS} = 10$ to 0 V	–	47	60	ns

N-channel enhancement mode vertical D-MOS transistor
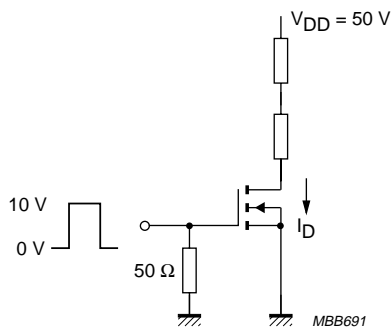
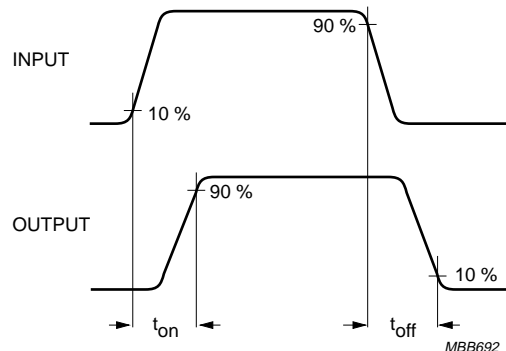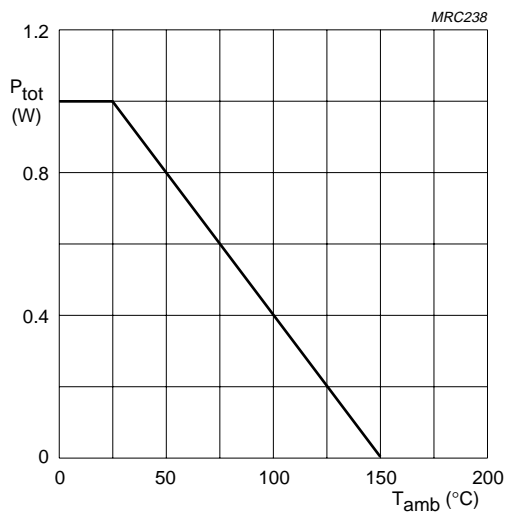BSN254; BSN254A

Fig.2 Switching times test circuit.
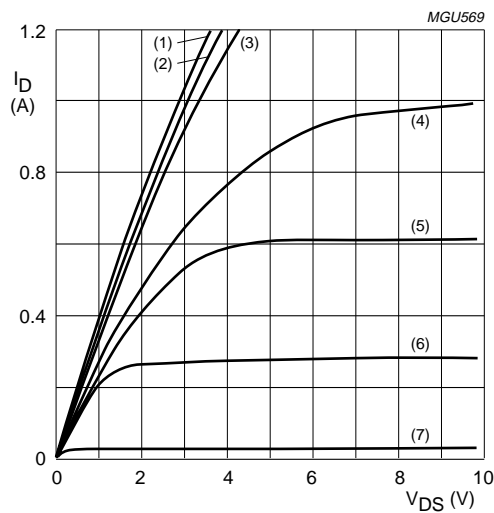

Fig.3 Input and output waveforms.
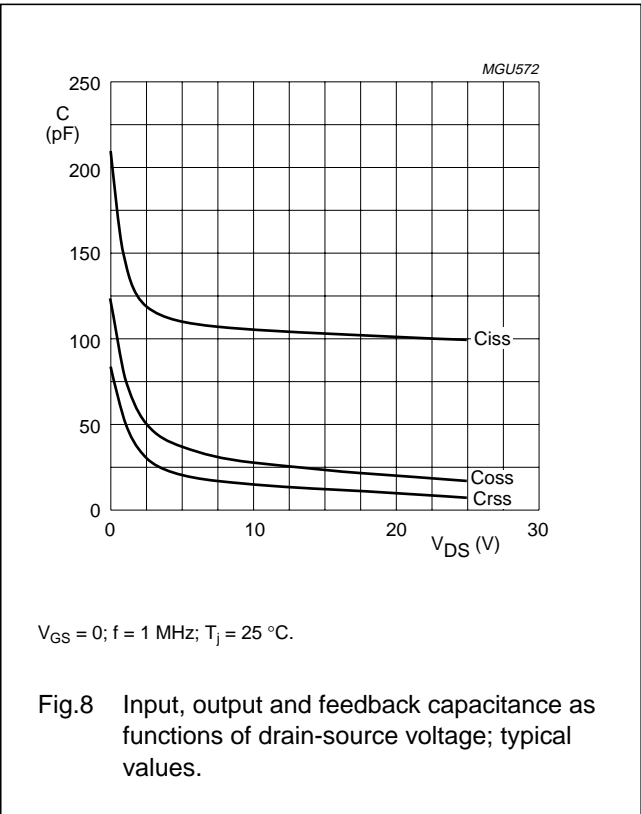

Fig.4 Power derating curve.

$T_j = 25\ °C.$
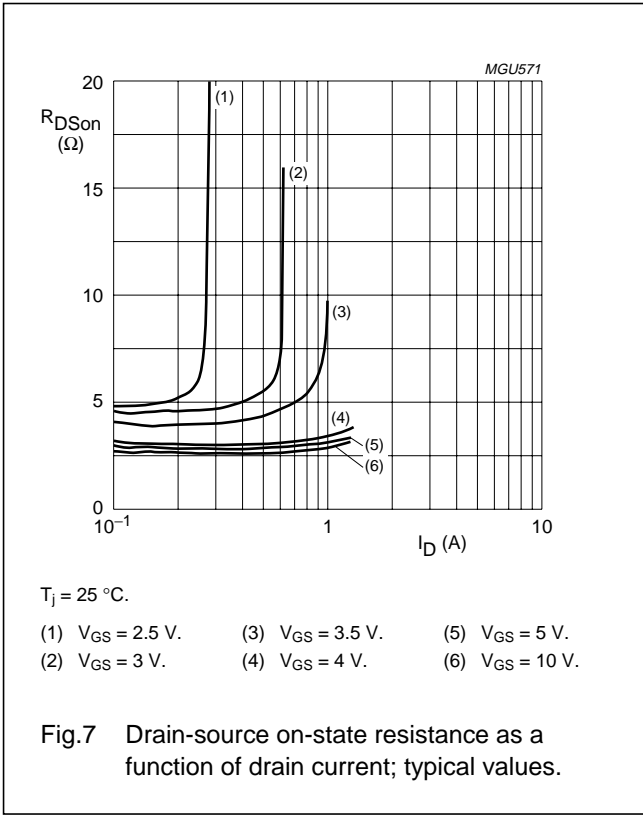
(1) $V_{GS} = 10$ V.　　(4) $V_{GS} = 3.5$ V.　　(7) $V_{GS} = 2$ V.
(2) $V_{GS} = 5$ V.　　(5) $V_{GS} = 3$ V.
(3) $V_{GS} = 4$ V.　　(6) $V_{GS} = 2.5$ V.

Fig.5 Typical output characteristics.

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$V_{DS} = 10$ V; $T_j = 25$ °C.

Fig.6 Typical transfer characteristics.

$T_j = 25$ °C.

(1) $V_{GS} = 2.5$ V.	(3) $V_{GS} = 3.5$ V.	(5) $V_{GS} = 5$ V.
(2) $V_{GS} = 3$ V.	(4) $V_{GS} = 4$ V.	(6) $V_{GS} = 10$ V.

Fig.7 Drain-source on-state resistance as a function of drain current; typical values.

$V_{GS} = 0$; f = 1 MHz; $T_j = 25$ °C.

Fig.8 Input, output and feedback capacitance as functions of drain-source voltage; typical values.
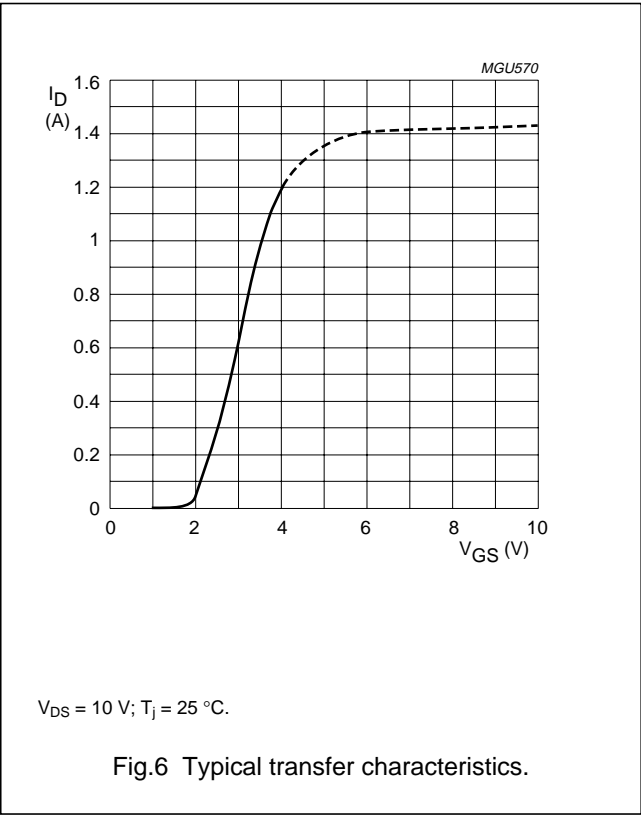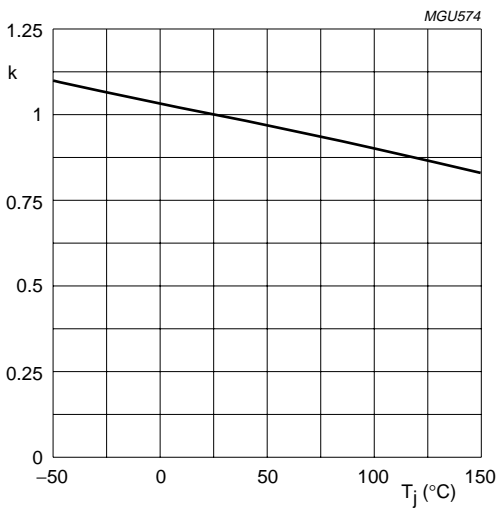
N-channel enhancement mode vertical D-MOS transistor

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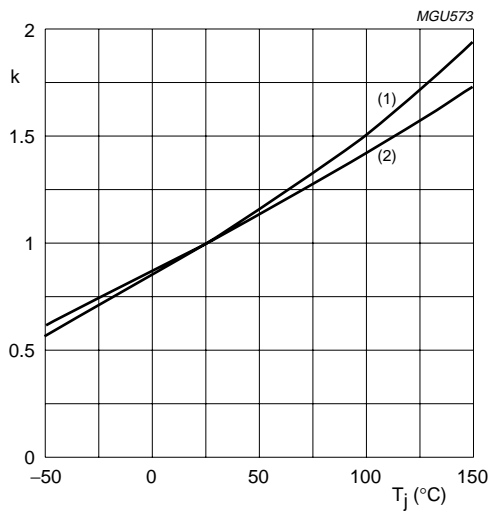
$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ ^{\circ}C}$$

Typical R_{DSon}:

(1) I_D = 250 mA; V_{GS} = 10 V.

(2) I_D = 20 mA; V_{GS} = 2.4 V.

Fig.9   Temperature coefficient of drain-source
on-state resistance; typical values.

$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25\ ^{\circ}C}$$

Typical V_{GSth} at 1 mA.

Fig.10   Temperature coefficient of gate-source
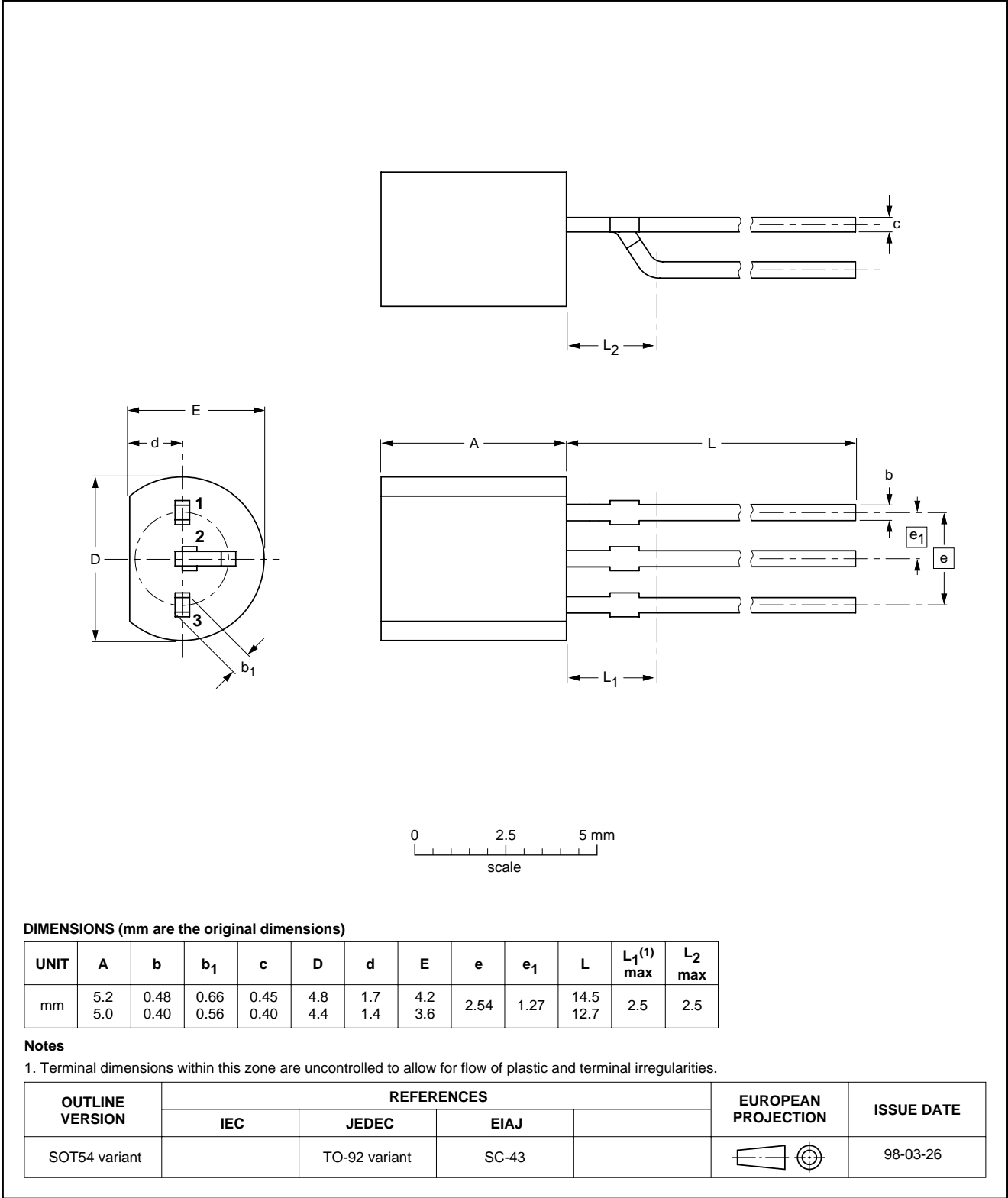threshold voltage; typical values.

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PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)   **SOT54 variant**

0   2.5   5 mm

scale

DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	$L_1^{(1)}$ max	L_2 max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	**JEDEC**	**EIAJ**			
SOT54 variant		TO-92 variant	SC-43			98-03-26

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DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
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