

# Multilayer ceramic capacitor

HighCV, X7R 0805  $1\mu F$  50 V

Series/Type: Chip

Ordering code: B37941K5105K0\*\*

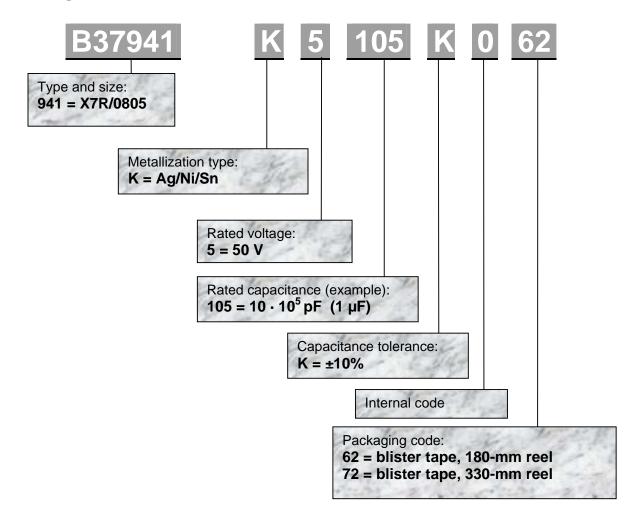
Date: 25.10.2005

Version: 2

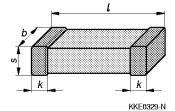
HighCV, X7R 0805 1µF 50 V

Chip

## **Ordering code**



# **Dimensional drawing**



Size	I	b	S	k
[inch / mm]	[mm]	[mm]	[mm]	[mm]
<b>0805</b> / 2012	2.0 ±0.20	1.25 ±0.15	1.35 max.	0.13 - 0.75

see also "Ordering codes and chip thickness", dimensions in accordance to CECC 32101-801

KB VS PE 25.10.2005

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#### **Electrical data**

Temperature characteristic: X7R

Climatic category (IEC 60068-1): 55/125/56

Standard: EIA
Dielectric: Class 2
Rated voltage: 50 V

Capacitance<sup>1)</sup> test conditions

Test frequency:  $(1.0 \pm 0.2) \text{ kHz}$ Test voltage:  $(1.0 \pm 0.2) \text{ V}_{\text{RMS}}$ 

Max. relative capacitance change:  $\pm 15\%$ Dissipation factor tanδ (limit value):  $< 25 \cdot 10^{-3}$ Time constant  $\tau$  at +25 °C: > 500 s

Operating temperature range: -55 °C ... +125 °C

Capacitance value: 1 µF

#### **Note**

This MLCC is designed for automotive applications.

It is specified for applications in automotive DC board nets from 12V to 24V with pulse-loaded environment up to 300V maximum pulse height acc. to IEC 7637<sup>2)</sup>.

Qualification has been performed acc. to AEC-Q200 for 50V rated voltage.

Permanent DC-loading above 25V respectively AC-loading above 40V (peak to peak) is not recommended. Please contact your local EPCOS dealer for your application.

KB VS PE 25.10.2005

Subject to aging, please see "General Technical Information" at www.epcos.com/ceramic capacitors or the databook "Multilayer Ceramic Capacitors".

<sup>&</sup>lt;sup>2)</sup> Pulses 1,2,3,4,5,6 of IEC 7637 and jump-start pulses are specified

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Chip

### Ordering codes and chip thickness

Size	$C_R$	Ordering code	Thickness	Packing quantity	
				Ø 180-mm reel	Ø 330-mm reel
[inch]	[µF]		[mm]	[pcs]	[pcs]
0805	1	B37941K5105K062*	1.25 ±0.1	3000	12000

\* Ordering code example Standard tolerance: ±10%

Standard packaging: Blister tape, 180-mm reel

### **Further information**

Please see General Technical Information at <a href="www.epcos.com/ceramic capacitors">www.epcos.com/ceramic capacitors</a> or the data book "Multilayer Ceramic Capacitors" for further information on:

- Soldering directions
- Taping and packing
- Surface mounting instructions
- Effects of mechanical stress

# **Cautions and warnings**

- Derating: A "state of the art" application design is essential to achieve failures rates at ppb level. Do not use designs based on 100% of specified rated values.
- AC applications may damage MLCC on a much lower level than DC voltage due to power dissipation losses.
- Mechanical stress Please note EPCOS "General Technical Information", "Surface mounting instructions" and information about the effect of mechanical stress.
- ESD EPCOS recommends the use of varistors.
- Further processing care must be taken using moulding processes.
- Combined stresses the total stress (e.g. DC voltage, AC ripple, pulses and temperature) has to be taken into account to estimate reliability of MLCC.

KB VS PE 25.10.2005



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