DRAM

256K x 1 DRAM

FAST PAGE MODE

AVAILABLE AS MILITARY SPECIFICATIONS

- MIL-STD-883

FEATURES

- Industry standard pinout and timing
- All inputs, outputs and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby; 150mW active, typical
- Common I/O capability using "EARLY-WRITE"
- Optional PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$- ONLY,$\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256-cycle refresh distributed across 4ms
- Specifications guaranteed over full military DRAM temperature range (-55°C to +125°C)

OPTIONS MARKING

- Timing

100ns access	-10
120ns access	-12
150ns access	-15

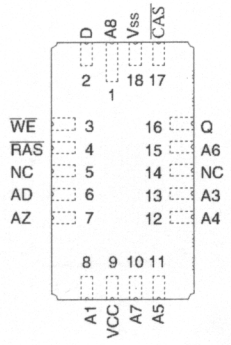
- Packages

Ceramic DIP (300 mil)	C	No. 100
Ceramic Flatpack	F	No. 300
Ceramic LCC	EC	No. 200

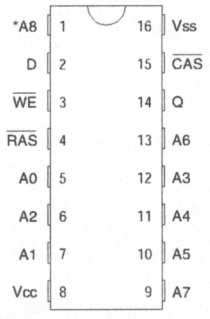
NOTE: Consult factory for other package options.

PIN ASSIGNMENT (Top View)

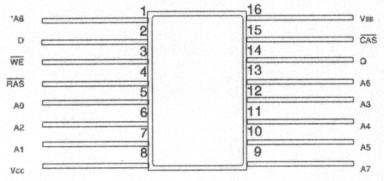
18-Pin LCC



16-Pin DIP
(D-2)



16-Pin F/P



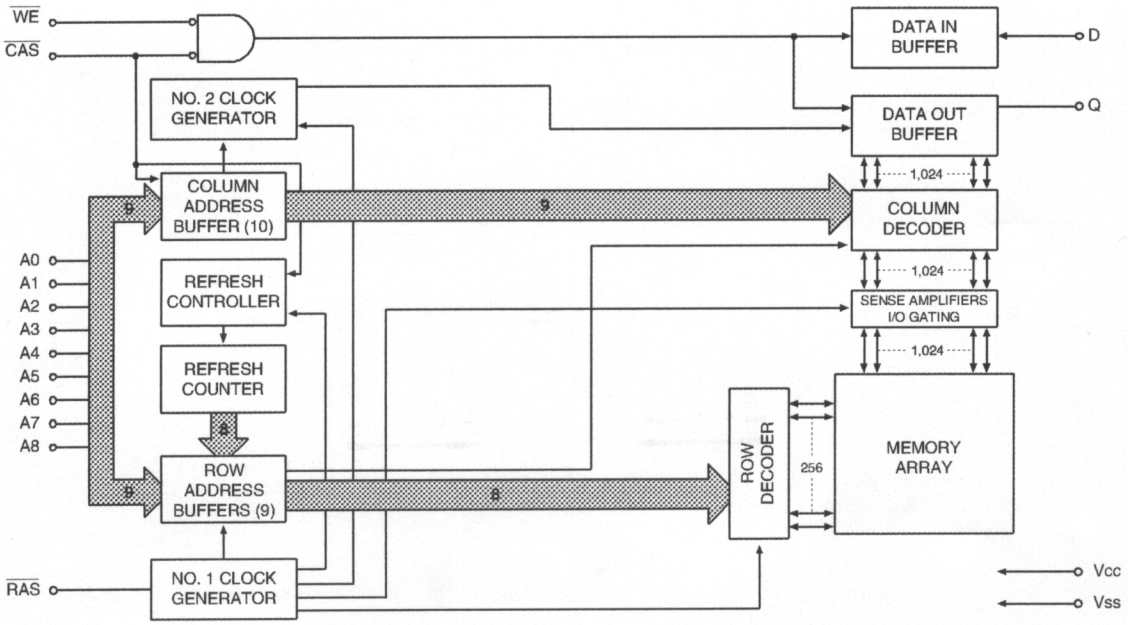
*Address not used for $\overline{RAS}$-ONLY REFRESH

GENERAL DESCRIPTION

The AS4C1259 883C is a randomly accessed solid-state memory containing 262,144 bits organized in a x1 configuration. The 18 address bits are entered 9 bits at a time using $\overline{RAS}$ to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. If the $\overline{WE}$ pin goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, the output pin is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-MODIFY- WRITEcycle. Data in is latched when $\overline{WE}$ strobes LOW.

By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled to execute several faster READ, WRITE, READ-WRITE or READ-MODIFY-WRITE cycles within the $\overline{RAS}$ address defined page boundary. Returning $\overline{RAS}$ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (READ, WRITE, $\overline{RAS}$-ONLY or HIDDEN REFRESH) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4ms (regardless of sequence).

EQUIVALENT FUNCTIONAL BLOCK DIAGRAM
PAGE MODE



TRUTH TABLE

FUNCTION	RAS	CAS	WE	ADDRESSES		DATA
				^tR	^tC	
Standby	H	H	H	X	X	High-Z
READ	L	L	H	ROW	COL	Data Out
EARLY-WRITE	L	L	L	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	ROW	COL	Data Out, Data In
PAGE-MODE READ	L	H→L→H	H	ROW	COL	Data Out, Data Out
PAGE-MODE EARLY-WRITE	L	H→L→H	L	ROW	COL	Data In, Data In
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	ROW	COL	Data Out, Data In
RAS-ONLY REFRESH	L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -1.5V to +7.0V
Storage Temperature Range ..... -65°C to +150°C
Power Dissipation ..... 1 W
Lead Temperature (soldering 5 sec.) ..... 300°C
Junction Temperature (Tj) ..... +150°C
Short Circuit Output Current 50mA
Thermal Resistance (θjc) 16-pin DIP ..... 50°C/W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL PERFORMANCE CHARACTERISTICS

(Notes: 4, 6, 7) (-55°C ≤ T_C ≤ +125°C; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Current from V_{CC} (active); $\overline{RAS}$ and $\overline{CAS}$ Cycling; $T_{RC} = T_{RC(MIN)}$	I_{CC1}		70	mA	3
Supply Current from V_{CC} (active, PAGE MODE); $\overline{RAS} = V_{IL}$, $\overline{CAS}$ Cycling; $T_{PC} = T_{PC(MIN)}$	I_{CC2}		65	mA	3
Supply Current from V_{CC} (standby); $\overline{RAS}$ and $\overline{CAS} = V_{IH}$	I_{CC3}		8	mA	
Supply Current from V_{CC} (refresh, $\overline{RAS}$ ONLY); $\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$	I_{CC4}		70	mA	3
Supply Current from V_{CC} (refresh, $\overline{CAS}$-BEFORE-$\overline{RAS}$); $\overline{RAS}$ and $\overline{CAS}$ Cycling	I_{CC5}		70	mA	3
Output High Voltage (I_{OH} = -5mA)	V_{OH}	2.4		V	1
Output Low Voltage (I_{OL} = 5mA)	V_{OL}		0.4	V	1
Input Leakage	I_{IH}	-5	5	µA	
Any input (0V ≤ V_{IN} ≤ V_{CC}); all other pins = 0V	I_{IL}	-5	5	µA	
Output Leakage (0 ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-5	5	µA	

DC OPERATING CONDITIONS

(Notes: 4, 6, 7) (-55°C ≤ T_C ≤ +125°C; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc Supply Voltage	V_{CC}	4.5	5.5	V	
Vss Power Supply and Signal Reference	Vss	0.0	0.0	V	1
High Level Input Voltage (all inputs)	V_{IH}	2.4	V_{CC}+.5	V	1
Low Level Input Voltage (all inputs)	V_{IL}	-.5	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: (A_0-A_8), D	C_{I1}		7	pF	3
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	3
Output Capacitance: Q	C_O		8	pF	3

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

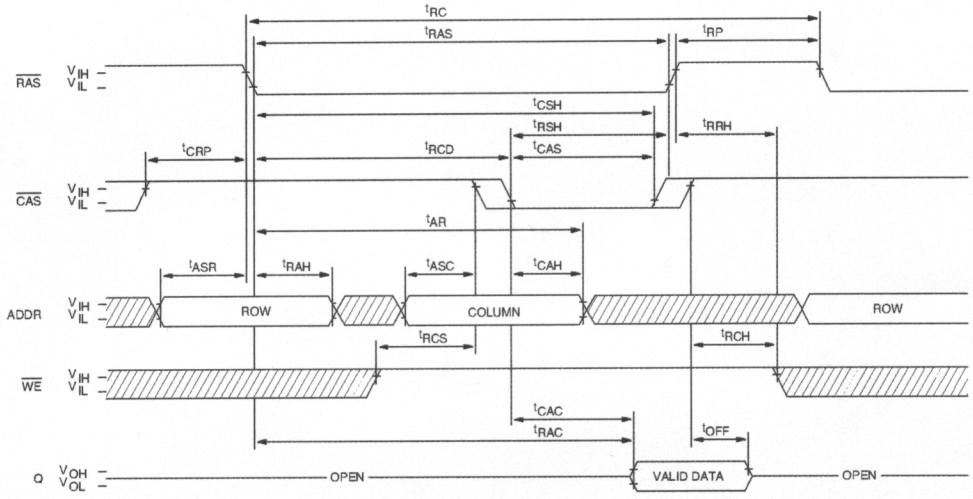
(Notes: 4, 5, 6, 7, 8) (-55°C ≤ T C ≤ 125°C, VCC = 5.0V ±10%)

AC CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^{t}RC	180		210		250		ns	
READ-MODIFY-WRITE cycle time	^{t}RWC	210		245		275		ns	18
PAGE-MODE cycle time	^{t}PC	75		90		110		ns	18
Access time from RAS\	^{t}RAC		100		120		150	ns	9
Access time from CAS\	^{t}CAC		50		60		75	ns	10
RAS\ pulse width	^{t}RAS	100	10,000	120	10,000	150	10,000	ns	
CAS\ pulse width	^{t}CAS	50	10,000	60	10,000	75	10,000	ns	
RAS precharge time	^{t}RP	70		80		90		ns	
RAS hold time	^{t}RSH	50		60		75		ns	
RAS\ to CAS\ delay time	^{t}RCD	25	50	30	60	35	75	ns	20
CAS\ precharge time	^{t}CPN	15		20		25		ns	18
CAS\ precharge time (PAGE-MODE)	^{t}CP	15		20		25		ns	11
CAS to RAS\ set-up time	^{t}CRP	5		5		5		ns	
CAS\ hold time	^{t}CSH	110		120		150		ns	
Row address set-up time	^{t}ASR	0		0		0		ns	18
Row address hold time	^{t}RAH	15		15		20		ns	
Column address set-up time	^{t}ASC	0		0		0		ns	18
Column address hold time	^{t}CAH	20		25		25		ns	
Column address hold time referenced to RAS\	^{t}AR	70		80		100		ns	
READ command set-up time	^{t}RCS	0		0		0		ns	18
READ command hold time referenced to CAS\	^{t}RCH	0		0		0		ns	18
READ command hold time referenced to RAS\	^{t}RRH	10		10		10		ns	
Output disable delay	^{t}OFF	0	20	0	20	0	25	ns	12
WRITE command set-up time	^{t}WCS	0		0		0		ns	13
WRITE command hold time	^{t}WCH	35		40		45		ns	
WRITE command hold time referenced to RAS\	^{t}WCR	85		100		120		ns	
WRITE command pulse width	^{t}WP	35		40		45		ns	
WRITE command to RAS\ lead time	^{t}RWL	35		40		45		ns	
WRITE command to CAS\ lead time	^{t}CWL	35		40		45		ns	
Data-in set-up time	^{t}DS	0		0		0		ns	14,18
Data-in hold time	^{t}DH	35		40		45		ns	14
Data-in hold time referenced to RAS\	^{t}DHR	85		100		120		ns	
CAS\ to WRITE delay	^{t}CWD	40		50		60		ns	13,18
RAS\ to WRITE delay	^{t}RWD	90		110		135		ns	13,18
Transition time (rise or fall)	^{t}T	3	100	3	100	3	100	ns	18
CAS\ set-up time (CAS-BEFORE-RAS REFRESH)	^{t}CSR	10		10		10		ns	15
CAS\ hold time (CAS-BEFORE-RAS REFRESH)	^{t}CHR	20		25		30		ns	15
Refresh period (256 cycles distributed)	^{t}REFD		4		4		4	ms	16
Refresh period (256 cycles burst)	^{t}REFB		4		4		4	ms	17
RAS\ to CAS\ precharge time	^{t}RPC		0		0		0	ns	18
WE\ set-up time before RAS\ low	^{t}WRP	10		10		10		ns	9,10,11
WE\ hold time after RAS\ low CAS\ before RAS\ refresh	^{t}WRH	10		10		10		ns	9,10,11

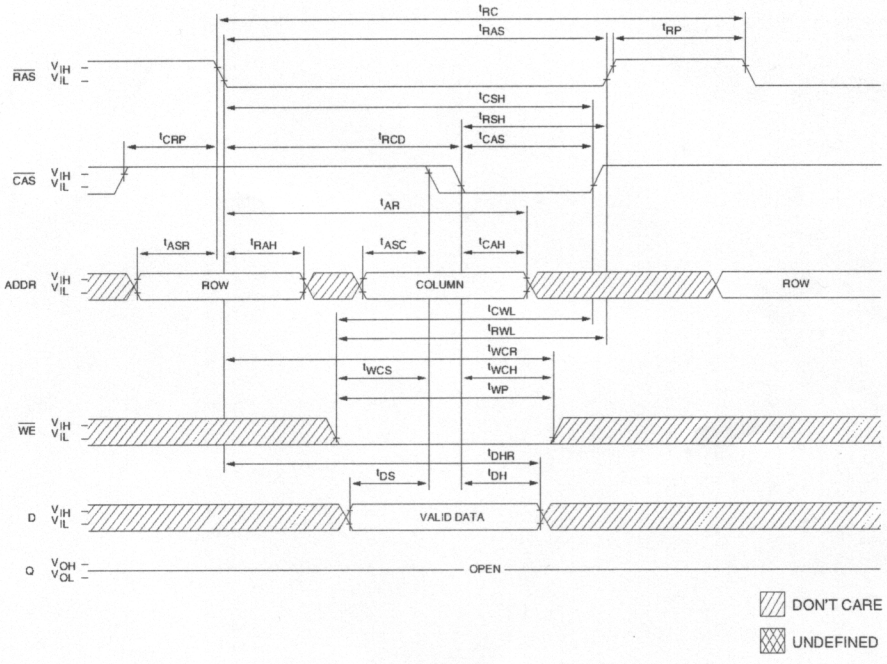
NOTES

1. All voltages referenced to V_{SS}.
2. Specified values are obtained with the output load equal to 2TTL loads and 100pF to V_{SS}.
3. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
4. An initial pause of 100µ sec is required after powerup followed by 8 dummy RAS cycles of which the first 4 cycles must be $\overline{RAS}$-only Refresh or CBR refresh cycles ($\overline{WE}$ held high) before proper device operation is assured.
5. AC characteristics assume transition time (^tT)=5ns. This parameter is not measured.
6. V_{IL} (MAX) and V_{IH} (MIN) are reference levels for measuring timing of input signals. Transition times are measured between V_{IL} and V_{IH}.
7. In addition to meeting the transition rate specification, all input signals must transit between V_{IL} and V_{IH} (or between V_{IH} and V_{IL}) in a monotonic manner.
8. If $\overline{CAS}$ = V_{IH}, data output is high impedance. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
9. Assumes that $^tRCD < {}^tRCD$ (MAX).
10. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
11. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP. Note 8 applies to determine valid data out.
12. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition. ^tOFF (MAX) is not referenced to V_{OH} or V_{OL}.
13. ^tWCS, ^tCWD and ^tRWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (MIN) the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tCWD \geq {}^tCWD$ (MIN) and $^tRWD \geq {}^tRWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to the $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
15. Enable on-chip refresh and address counters.
16. A 256-cycle distributed refresh consists of an address location refresh cycle being performed within 15.625µS so that all 256 $\overline{RAS}$ address combinations are executed within 4ms (regardless of sequence). Micron recommends distributed refresh.
17. A 256-cycle burst refresh consists of refreshing, as rapidly as minimum cycle time allows, all 256 combinations of $\overline{RAS}$ addresses (regardless of sequence). The refresh mode must be executed within 4ms.
18. This parameter is a "conditionally" guaranteed parameter that is specified to aid with device application. It is not directly verified by a specific test but is used, with several other parameters, in the performance verification of other attributes.
19. A HIDDEN Refresh may also be performed after a Write cycle. In this case $\overline{WE}$ = LOW.
20. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.

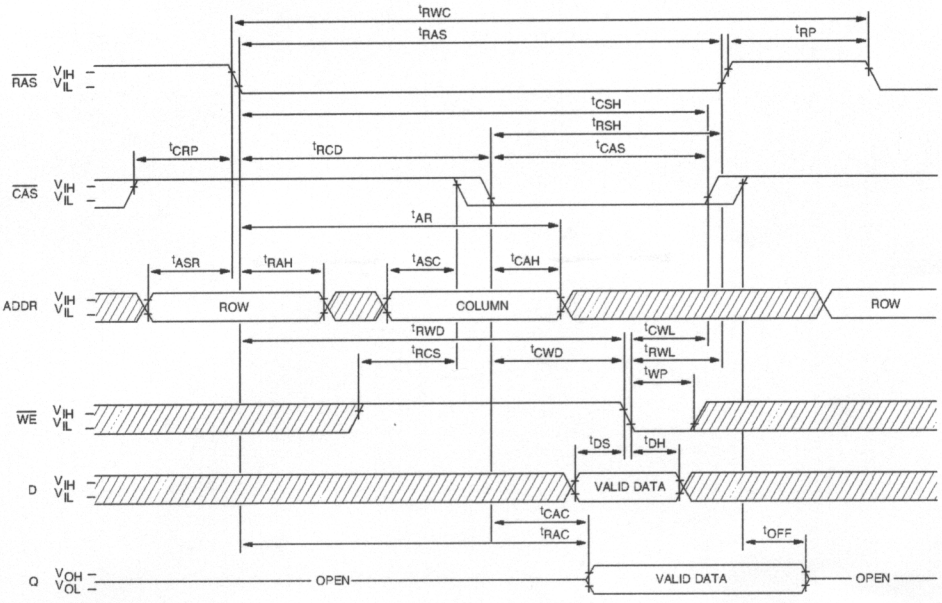
READ CYCLE



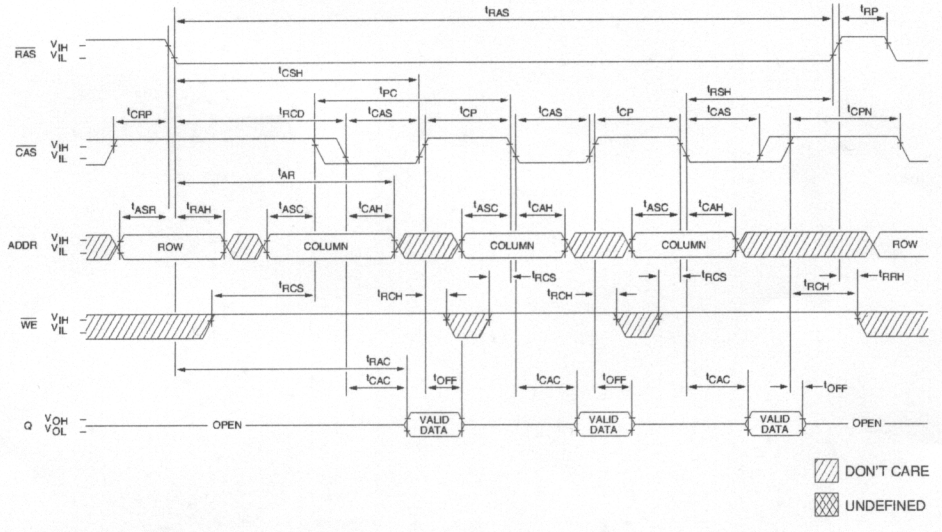
EARLY-WRITE CYCLE



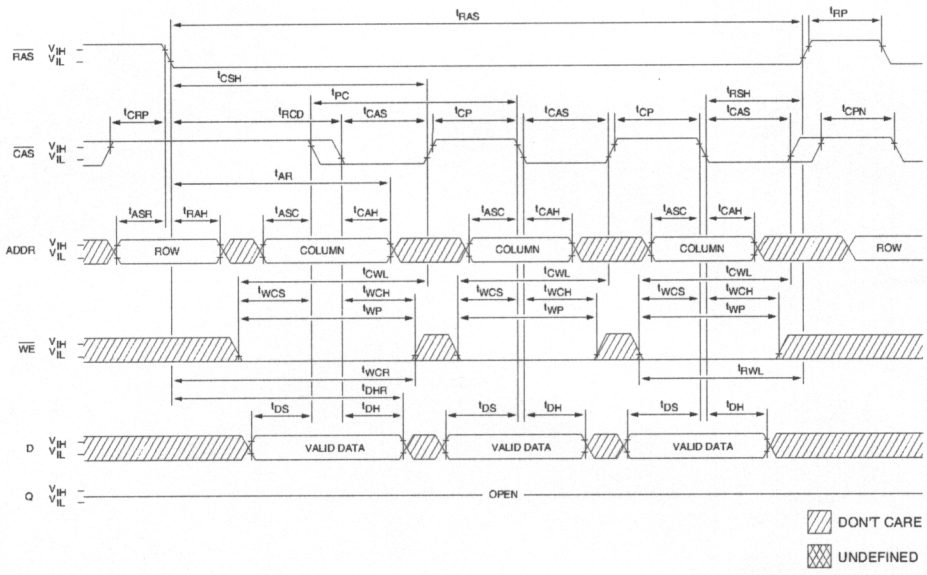
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



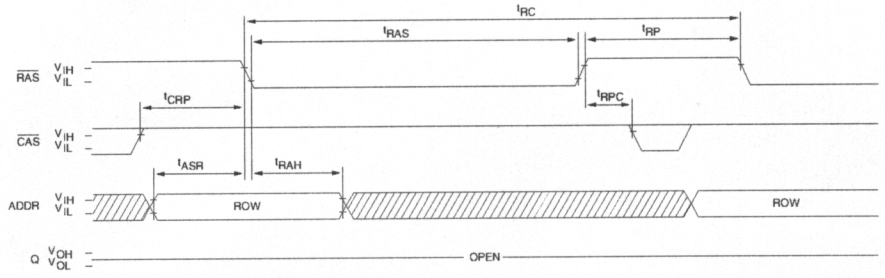
PAGE-MODE READ CYCLE



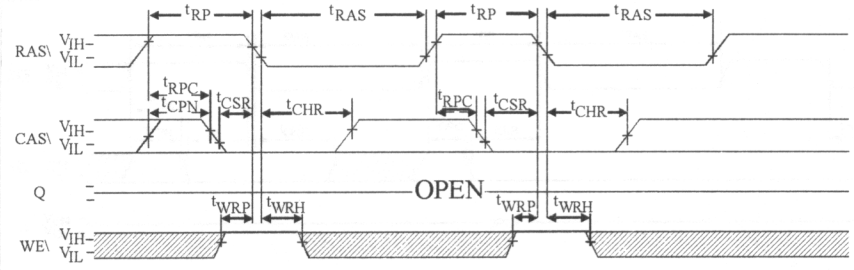
PAGE-MODE EARLY-WRITE CYCLE



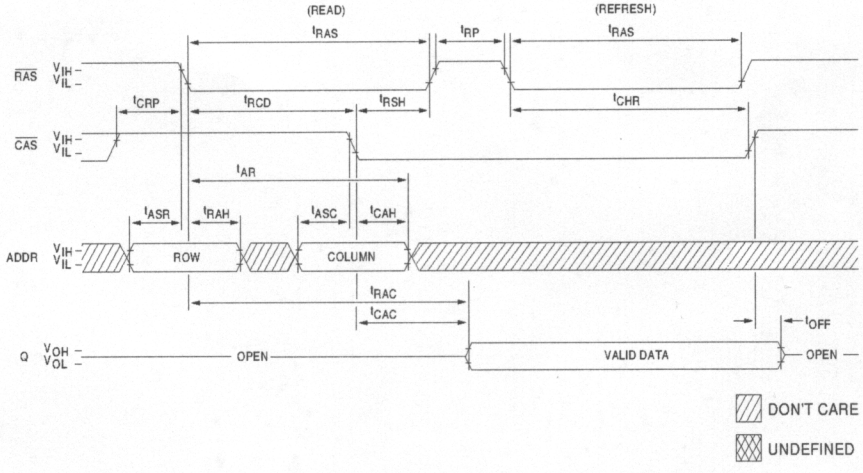
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE
(ADDR = A0-A7; A8 and $\overline{\text{WE}}$ = DON'T CARE)



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE
(A0 – A8 = DON'T CARE)



HIDDEN REFRESH CYCLE [19]
($\overline{\text{WE}}$ = HIGH)



ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per Method 5005, Table I)
INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004)	2, 8A, 10
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroups 1 and 7.

** Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.