AP602

High Dynamic Range 4W 28V HBT Amplifier

Product Features

- 800 – 2400 MHz
- +35.7 dBm P1dB
- -52 dBc ACLR @ ½W P_{AVG}
- -47 dBc IMD3 @ ½W PEP
- 16% Efficiency @ ½W P_{AVG}
- Internal Active Bias
- Internal Temp Compensation
- Capable of handling 7:1 VSWR @ 28 Vcc, 2.14 GHz, 3W CW Pout
- Lead-free/RoHS-compliant 5x6 mm power DFN package

Applications

- Mobile Infrastructure HPA
- WiBro HPA

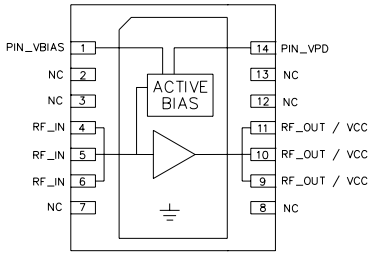
Product Description

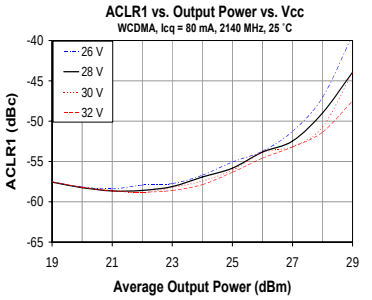
The AP602 is a high dynamic range power amplifier in a lead-free/RoHS-compliant 5x6mm power DFN SMT package. The single stage amplifier has excellent backoff linearity, while being able to achieve high performance for 800-2400 MHz applications with up to +35.7 dBm of compressed 1dB power.

The AP602 uses a high reliability, high voltage InGaP/GaAs HBT process technology. The device incorporates proprietary bias circuitry to compensate for variations in linearity and current draw over temperature. The module does not require any negative bias voltage; an internal active bias allows the AP602 to operate directly off a commonly used high voltage supply (typically +24 to +32V). An added feature allows the quiescent bias to be adjusted externally to meet specific system requirements.

The AP602 is targeted for use as a pre-driver and driver stage amplifier in wireless infrastructure where high linearity and high efficiency is required. This combination makes the device an excellent candidate for next generation multi-carrier 3G mobile infrastructure.

Functional Diagram





Specifications

W-CDMA 3GPP Test Model 1+64 DPCH, 60% clipping, PAR = 8.6 dB @ 0.01% Probability, 3.84 MHz BW, Vcc = +28V, Icq = 80 mA

Parameter	Units	Min	Typ	Max
Operational Bandwidth	MHz	800		2200
Test Frequency	MHz		2140	
Output Channel Power	dBm		+27	
Power Gain	dB		13	
Input Return Loss	dB		9	
Output Return Loss	dB		9	
ACLR	dBc		-52	
IMD3 @ +27 dBm PEP	dBc		-47	
PIN_VPD Current, Ipd	mA		2	
Operating Current, Icc	mA		112	
Collector Efficiency	%		15.7	
Output P1dB	dBm		+35.7	
Quiescent Current, Icq	mA		80	
Vpd, Vbias	V		+5	
Vcc	V		+28	

Typical Performance

W-CDMA 3GPP Test Model 1+64 DPCH, 60% clipping, PAR = 8.6 dB @ 0.01% Probability, 3.84 MHz BW, Vcc = +28V, Icq = 80 mA

Parameter	Units	Typical		
Test Frequency	MHz	940	1960	2140
Channel Power	dBm	+27	+27	+27
Power Gain	dB	15.5	14.2	13
Input Return Loss	dB	11	12	9
Output Return Loss	dB	6.4	9	9
ACLR	dBc	-50	-50	-52
IMD3 @ +27 dBm PEP	dBc	-62	-51	-47
Operating Current, Icc	mA	103	103	112
Collector Efficiency	%	17	17	15.7
Output P1dB	dBm	+35.7	+35.5	+35.7
Quiescent Current, Icq	mA		80	
Vpd, Vbias	V		+5	
Vcc	V		+28	

Notes:
1. The reference designs shown in this datasheet have the device optimized for WCDMA ACLR performance at +25° C. Biasing for the amplifier is suggested at Vcc = +28V and Icq = 80 mA to achieve the best tradeoff in terms of efficiency and linearity. Increasing Icq will improve upon the device linearity (IMD3 and ACLR), but will decrease the efficiency performance slightly. More information is given in the other parts of this datasheet.
2. The AP602 evaluation board has been tested for ruggedness to be capable of handling:
   7:1 VSWR @ +28 Vcc, 2140 MHz, 3W CW Pout,
   5:1 VSWR @ +30 Vcc, 2140 MHz, 3W CW Pout,
   3:1 VSWR @ +32 Vcc, 2140 MHz, 3W CW Pout.

Absolute Maximum Rating

Parameter	Rating
Storage Temperature, T_{stg}	-55 to +125 ºC
Junction Temperature, T_J For 10^6 hours MTTF	192 ºC
RF Input Power (CW tone), P_{in}	Input P6dB
Breakdown Voltage C-B, BV_{CBO}	80 V @ 0.1 mA
Breakdown Voltage C-E, BV_{CEO}	51 V @ 0.1 mA
Quiescent Bias Current, I_{CQ}	160 mA
Power Dissipation, P_{DISS}	4.7 W

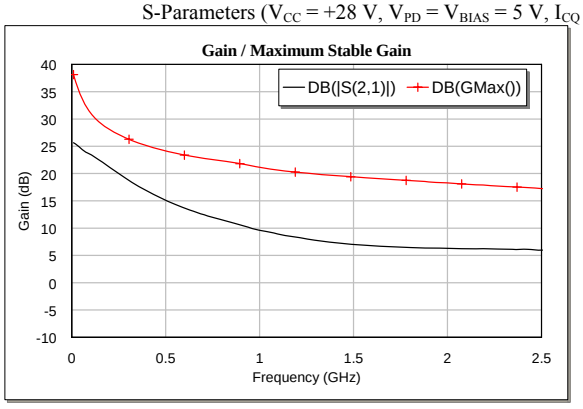
Operation of this device above any of these parameters may cause permanent damage.

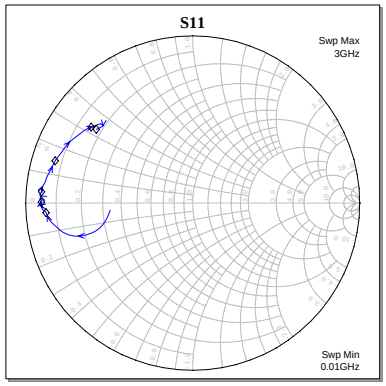
Ordering Information

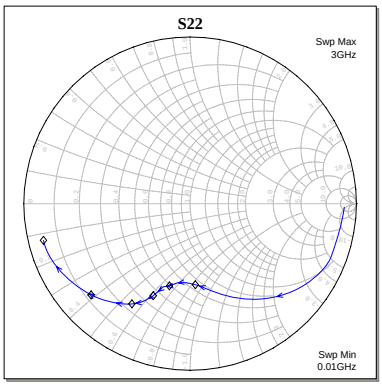
Part No.	Description
AP602-F	High Dynamic Range 28V 4W HBT Amplifier
AP602-PCB900	869-960 MHz Evaluation board
AP602-PCB1960	1930-1990 MHz Evaluation board
AP602-PCB2140	2110-2170 MHz Evaluation board

Typical Device Data

S-Parameters (V_{CC} = +28 V, V_{PD} = V_{BIAS} = 5 V, I_{CQ} = 80 mA, T = 25 °C, unmatched 50 ohm system, calibrated to device leads)





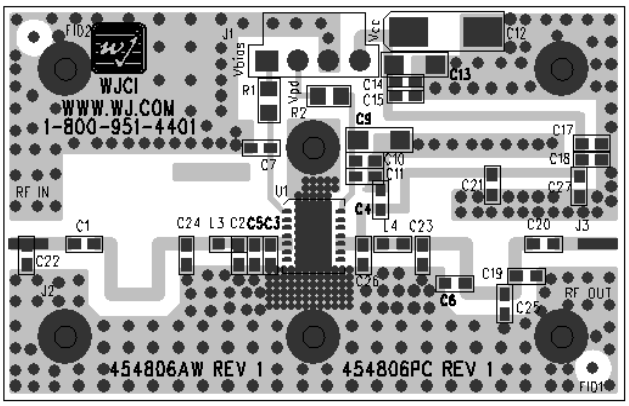


The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the marked red line. The impedance plots are shown from 50 – 3000 MHz, with markers placed at 0.5 – 3.0 GHz in 0.5 GHz increments.

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-5.48	-168.66	24.61	162.66	-43.82	67.14	-0.84	-15.48
100	-4.19	-163.72	23.51	148.99	-38.73	56.38	-1.30	-32.29
200	-2.36	-165.46	21.20	127.42	-35.02	38.63	-3.13	-55.32
400	-1.26	-173.46	16.82	105.39	-33.36	20.55	-5.71	-79.41
600	-0.93	-177.48	13.69	94.60	-33.10	12.05	-6.44	-91.66
800	-0.75	-179.37	11.52	87.62	-33.19	7.47	-6.28	-99.86
1000	-0.85	179.64	9.60	80.64	-32.66	16.69	-5.87	-104.18
1200	-0.77	178.55	8.33	75.01	-32.18	8.35	-5.44	-108.62
1400	-0.76	177.13	7.34	69.98	-31.99	4.86	-4.84	-110.75
1600	-0.85	174.34	6.75	64.38	-31.49	1.88	-4.22	-113.24
1800	-1.05	169.72	6.43	57.00	-30.96	-2.23	-3.65	-116.25
2000	-1.30	162.94	6.31	47.79	-30.28	-8.68	-3.15	-120.21
2200	-1.64	154.66	6.25	36.49	-29.50	-16.71	-2.64	-125.79
2400	-2.14	146.42	6.13	23.29	-28.80	-28.08	-2.11	-133.06
2600	-2.67	140.28	5.83	6.95	-28.30	-42.09	-1.57	-142.48
2800	-2.98	139.19	5.31	-11.57	-28.16	-59.43	-1.07	-154.01
3000	-2.77	142.63	4.53	-33.00	-28.51	-80.88	-0.83	-165.99

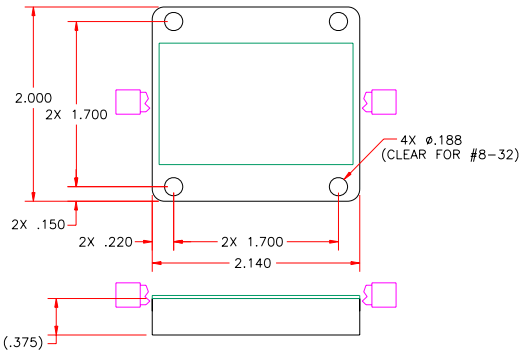
Device S-parameters are available for download off of the website at: http://www.wj.com

Application Circuit PC Board Layout



PCB Material: 0.0147" Rogers Ultralam 2000, single layer, 1 oz Cu, ε_r = 2.45, Microstrip line details: width = .042", spacing = .050"

Baseplate Configuration



Notes:
1. Please note that for reliable operation, the evaluation board will have to be mounted to a much larger heat sink during operation and in laboratory environments to dissipate the power consumed by the device. The use of a convection fan is also recommended in laboratory environments.
2. The area around the module underneath the PCB should not contain any soldermask in order to maintain good RF grounding.
3. For proper and safe operation in the laboratory, the power-on sequencing is recommended.

Evaluation Board Bias Procedure

Following bias procedure is recommended to ensure proper functionality of AP602 in a laboratory environment. The sequencing is not required in the final system application.

Bias.	Voltage (V)
Vcc	+28
Vbias	+5
Vpd	+5

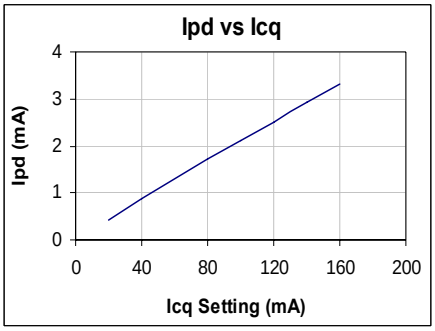
Turn-on Sequence:

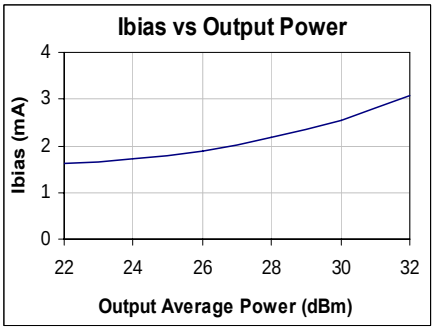
1. Attach input and output loads onto the evaluation board.
2. Turn on power supply Vcc = +28V.
3. Turn on power supply Vbias = +5V. At this point, the only current drawn by the device is leakage current (< 25µA).
4. Turn on power supply Vpd = +5V. Power supply Vcc should now be drawing typical Icq = 80 mA.
5. Turn on RF power.

Turn-off Sequence:

1. Turn off RF power.
2. Turn off power supply Vpd = +5V.
3. Turn off power supply Vbias = +5V.
4. Turn off power supply Vcc = +28V.

Notes:
1. Icq can be adjusted with the resistor R2 from the Vpd (+5V) supply and the PIN_VPD (pin14) of the amplifier. Increasing R2 results in a lower Icq. Icq should not be increased above 160mA.
2. Vpd is used as a reference for the internal active bias circuitry. It can be used to turn on/off the amplifier. Ipd depends on the Icq quiescent current setting. Ipd can be up to 4mA at a quiescent current setting of 160mA.
3. Vbias should be maintained fixed at +5V. Ibias will change based on RF input power level. It can be up to 4mA on the AP602.

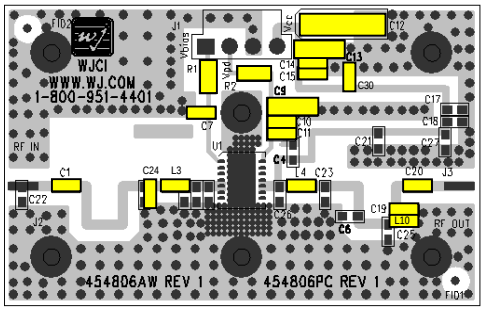


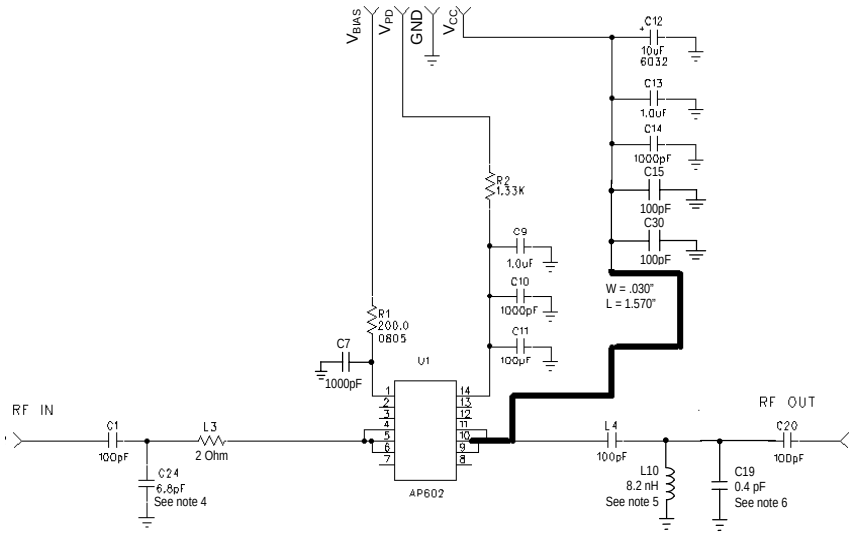


869-960 Application Circuit (AP602-PCB900)

Typical WCDMA Performance at 25 °C at a channel power of +27 dBm

Frequency	940 MHz
W-CDMA Channel Power	+27 dBm
Power Gain	15.5 dB
Input Return Loss	11 dB
Output Return Loss	6.4 dB
ACLR	-50 dBc
IMD3 @ +27 dBm PEP	-50 dBc
Operating Current, Icc	103 mA
Collector Efficiency	17 %
Output P1dB	+35.7 dBm
Quiescent Current, Icq	80 mA
Vpd, Vbias	+5 V
Vcc	+28 V

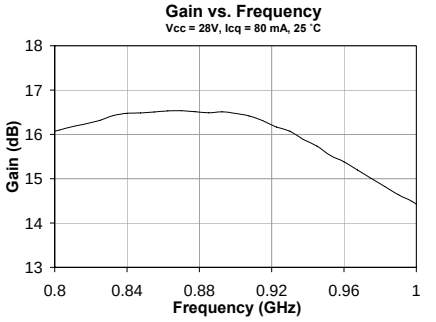


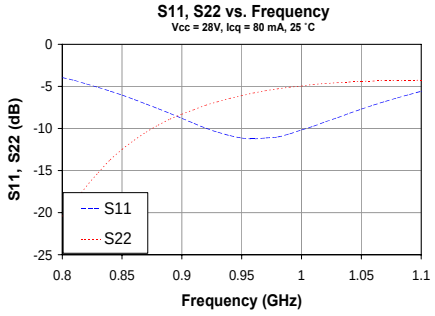


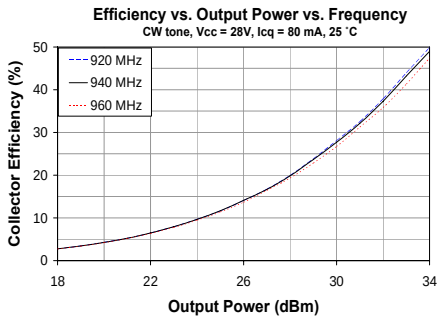
Notes:

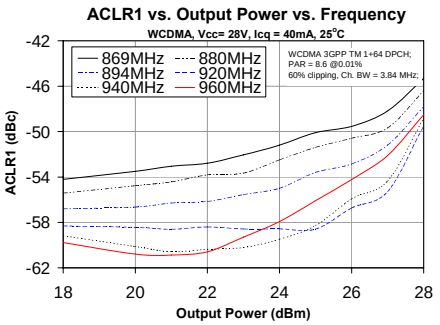
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. C20 is not required in the final design if there is no DC signal present at the output of the amplifier circuit.
4. The center of C24 is placed at 0.280" (11.5° @ 940 MHz) from the edge of the AP602 (U1).
5. The center of L10 is placed at 0.570" (23.4° @ 940 MHz) from the edge of the AP602 (U1).
6. The center of C19 is placed at 0.050" (2.1° @ 940 MHz) the center of L10.
7. The bold-faced RF trace is for the DC bias feed. The stub's length is approximately a ¼ λ.
8. The main RF trace is cut at component L3 and L4 for this particular reference design.

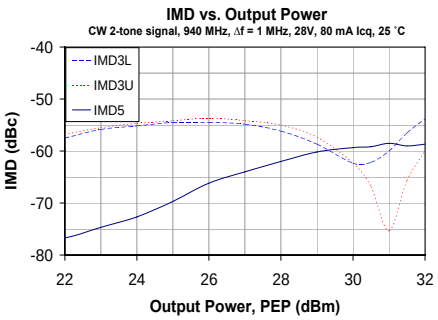
869-960 MHz Application Circuit Performance Plots

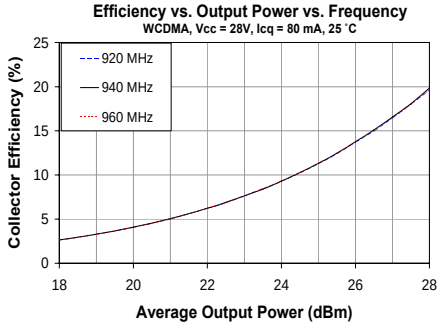










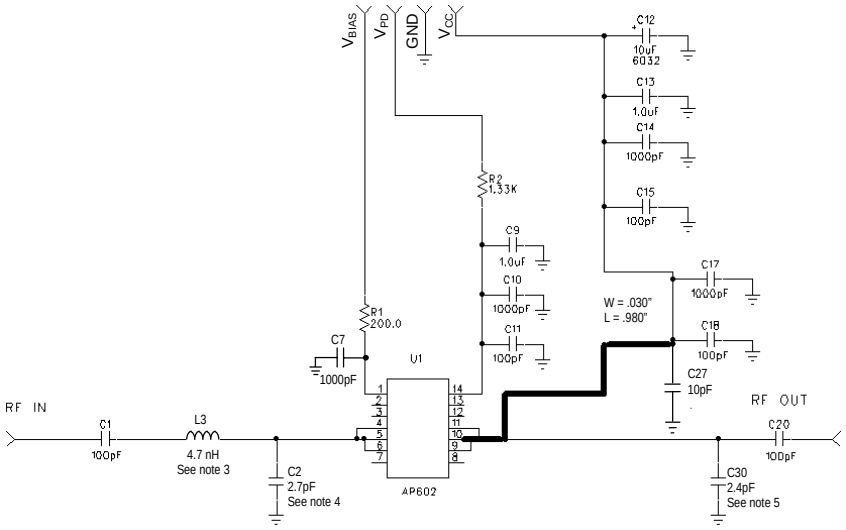


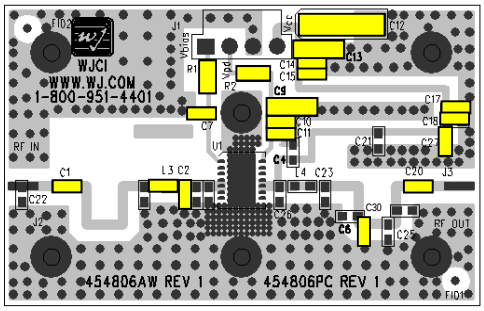
Unconditionally stable version of this application circuit is available for download off of the website at: http://www.wj.com

1930-1990 MHz Application Circuit (AP602-PCB1960)

Typical WCDMA Performance at 25 °C at a channel power of +27 dBm

Frequency	1960 MHz
W-CDMA Channel Power	+27 dBm
Power Gain	14.2 dB
Input Return Loss	12 dB
Output Return Loss	9 dB
ACLR	-50 dBc
IMD3 @ +27 dBm PEP	-51 dBc
Operating Current, Icc	103 mA
Collector Efficiency	17 %
Output P1dB	+35.5 dBm
Quiescent Current, Icq	80 mA
Vpd, Vbias	+5 V
Vcc	+28 V

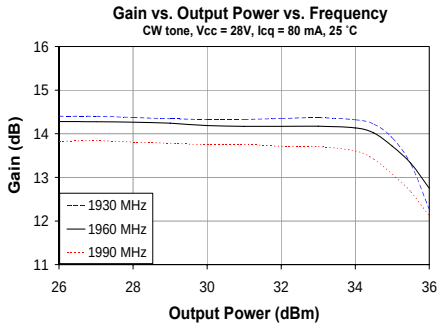


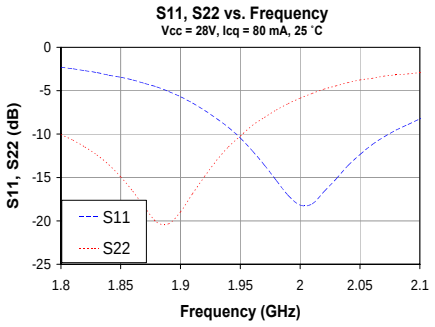


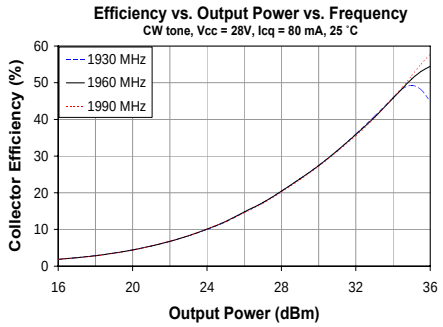
Notes:
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. The center of L3 is placed at 0.095" (8.1° @ 1960 MHz) from the center C2.
4. The center of C2 is placed at 0.135" (11.5° @ 1960 MHz) from the edge of the AP602 (U1).
5. The center of C30 is placed at 0.580" (49.6° @ 1960 MHz) from the edge of the AP602 (U1).
6. The bold-faced RF trace is for the DC bias feed. The stub's length is approximately a ¼ λ.
7. The main RF trace is cut at component location L3 for this particular reference design.

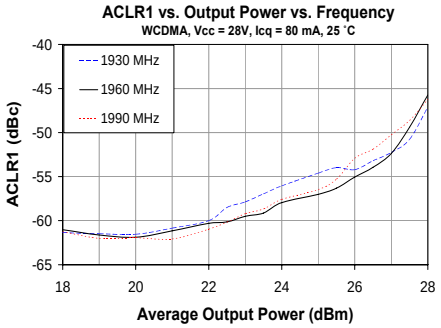
1930-1990 MHz Application Circuit Performance Plots

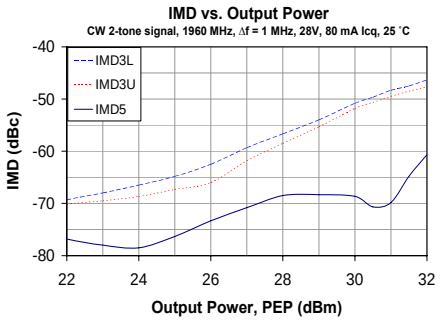
W-CDMA 3GPP Test Model 1+64 DPCH, 60% clipping, PAR = 8.6 dB @ 0.01% Probability, 3.84 MHz BW

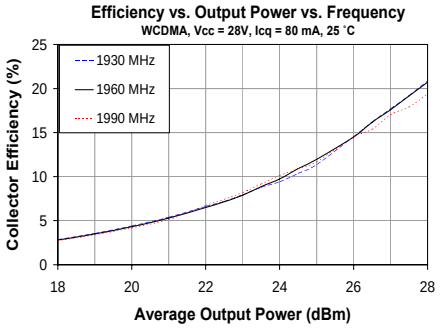








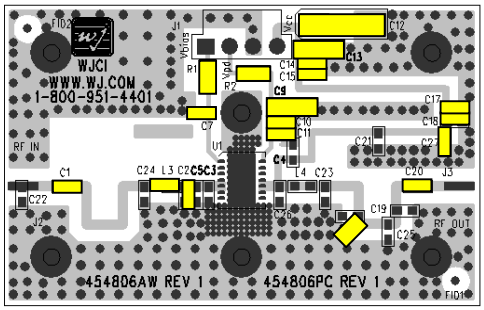


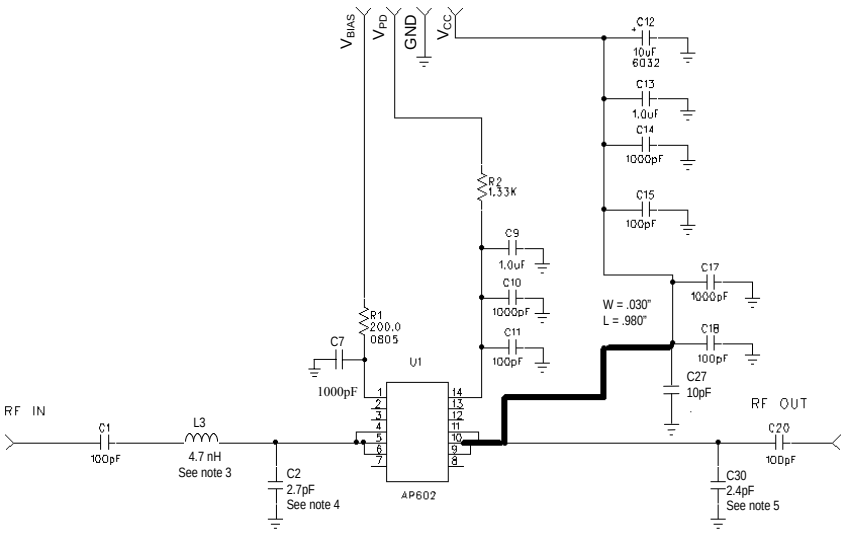


2010-2025 MHz Application Circuit

Typical Performance at 25 °C at an output power of +27 dBm

Frequency	2015 MHz
Total Output Power	+27 dBm
Power Gain	13.7 dB
Input Return Loss	12 dB
Output Return Loss	8.5 dB
IMD3 @ +27 dBm PEP	-44 dBc
Operating Current, Icc	110 mA
Collector Efficiency	16.5 %
Output P1dB	+36 dBm
Quiescent Current, Icq	80 mA
Vpd, Vbias	+5 V
Vcc	+28 V

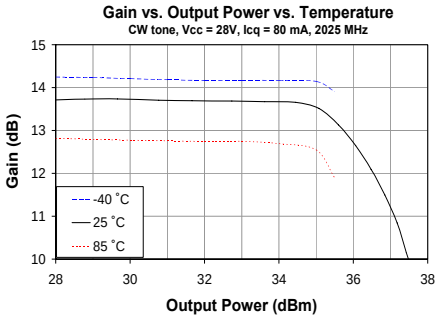


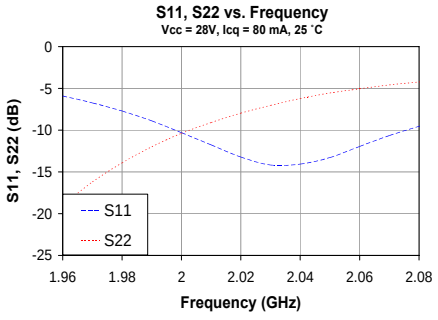


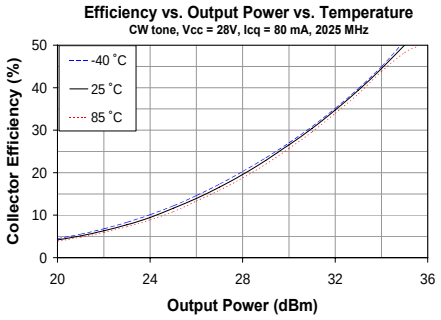
Notes:

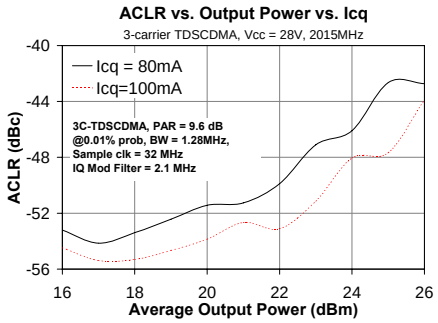
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. The center of L3 is placed at 0.095" (8.3° @ 2015 MHz) from the center of C2.
4. The center of C2 is placed at 0.135" (11.8° @ 2015 MHz) from the edge of the AP602 (U1).
5. The center of C30 is placed at 0.530" (50.9° @ 2015 MHz) from the edge of the AP602 (U1).
6. The bold-faced RF trace is for the DC bias feed. The stub's length is approximately a ¼ λ.
7. The main RF trace is cut at component location L3 for this particular reference design.

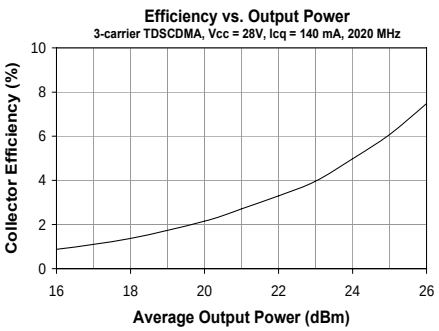
2010-2025 MHz Application Circuit Performance Plots

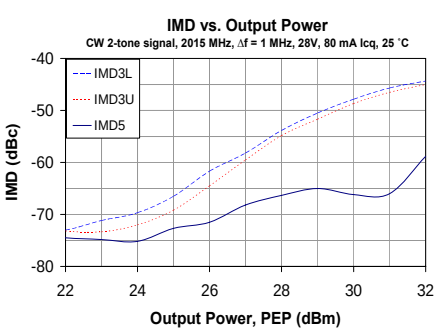










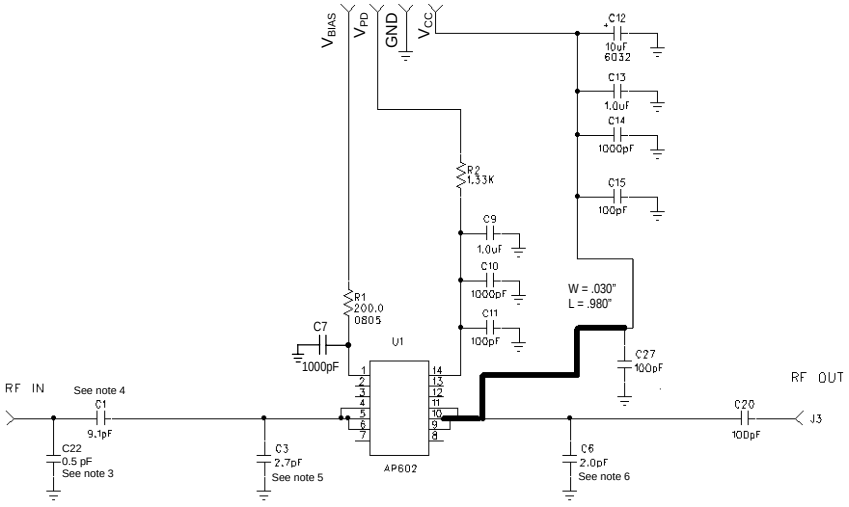


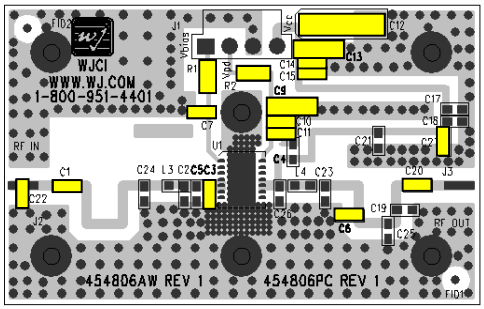
Unconditionally stable version of this application circuit is available for download off of the website at: http://www.wj.com

2110-2170 MHz Application Circuit (AP602-PCB2140)

Typical WCDMA Performance at 25 °C at a channel power of +27 dBm

Frequency	2140 MHz
W-CDMA Channel Power	+27 dBm
Power Gain	13 dB
Input Return Loss	9 dB
Output Return Loss	9 dB
ACLR	-52 dBc
IMD3 @ +27 dBm PEP	-47 dBc
Operating Current, Icc	112 mA
Collector Efficiency	15.7 %
Output P1dB	+35.7 dBm
Quiescent Current, Icq	80 mA
Vpd, Vbias	+5 V
Vcc	+28 V



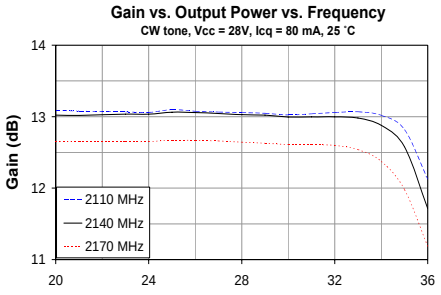


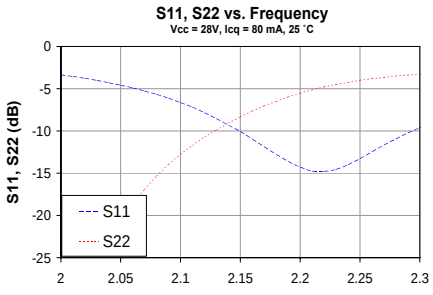
Notes:

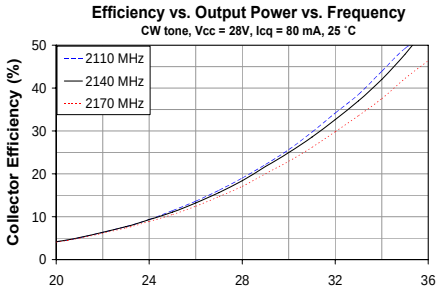
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. The center of C22 is placed at 0.185" (17.3° @ 2140 MHz) from the center of C1.
4. The center of C1 is placed at 0.910" (84.9° @ 2140 MHz) from the center of C3.
5. The center of C3 is placed at 0.035" (3.26° @ 2140 MHz) from the edge of the AP602 (U1).
6. The center of C6 is placed at 0.510" (47.6° @ 2140 MHz) from the edge of the AP602 (U1).
7. The bold-faced RF trace is for the DC bias feed. The stub's length is approximately a ¼ λ.

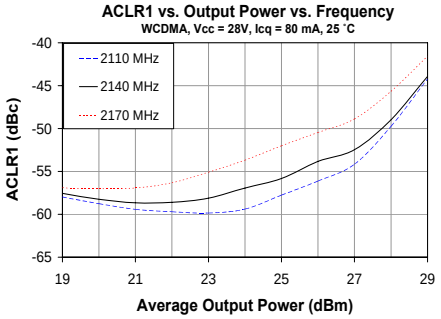
2110-2170 MHz Application Circuit Performance Plots

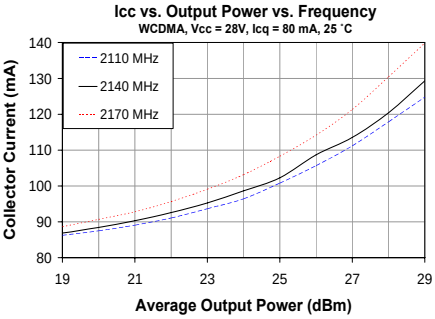
W-CDMA 3GPP Test Model 1+64 DPCH, 60% clipping, PAR = 8.6 dB @ 0.01% Probability, 3.84 MHz BW

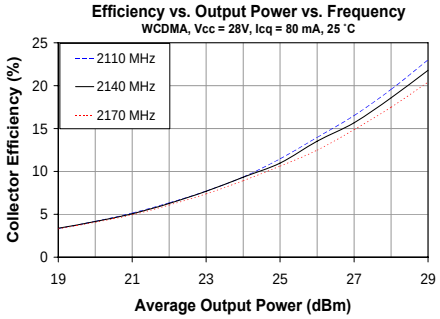








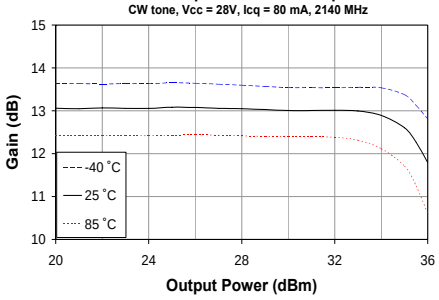




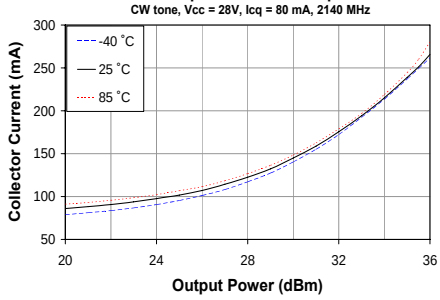
2110-2170 MHz Application Circuit Performance Plots

W-CDMA 3GPP Test Model 1+64 DPCH, 60% clipping, PAR = 8.6 dB @ 0.01% Probability, 3.84 MHz BW

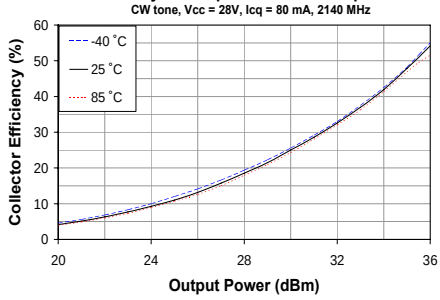
Gain vs. Output Power vs. Temperature
CW tone, Vcc = 28V, Icq = 80 mA, 2140 MHz



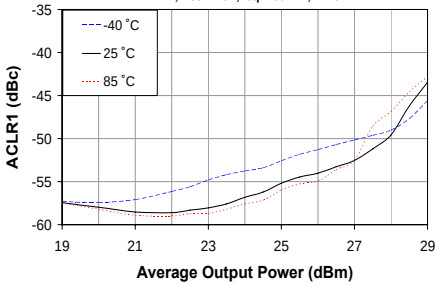
Icc vs. Output Power vs. Temperature
CW tone, Vcc = 28V, Icq = 80 mA, 2140 MHz



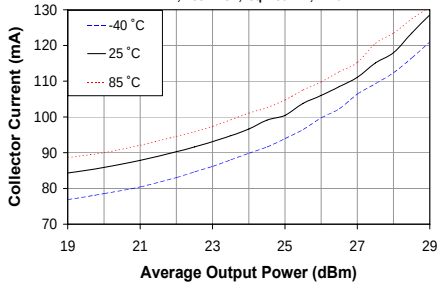
Efficiency vs. Output Power vs. Temperature
CW tone, Vcc = 28V, Icq = 80 mA, 2140 MHz



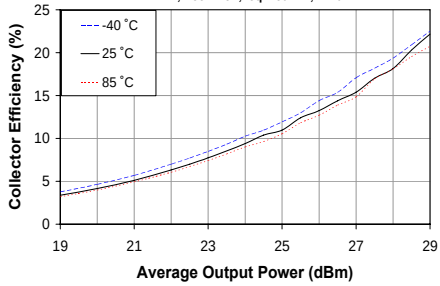
ACLR1 vs. Output Power vs. Temperature
WCDMA, Vcc = 28V, Icq = 80 mA, 2140 MHz



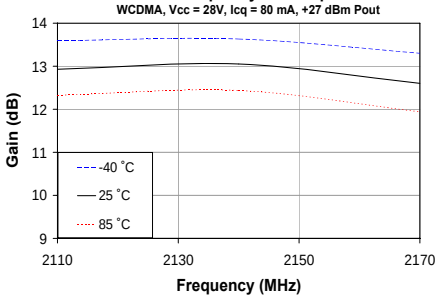
Icc vs. Output Power vs. Temperature
WCDMA, Vcc = 28V, Icq = 80 mA, 2140 MHz



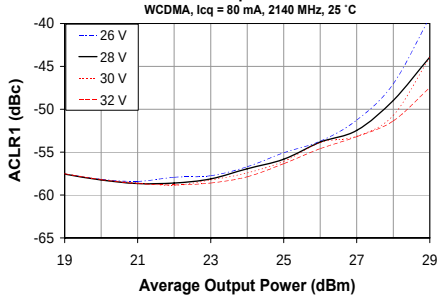
Efficiency vs. Output Power vs. Temperature
WCDMA, Vcc = 28V, Icq = 80 mA, 2140 MHz



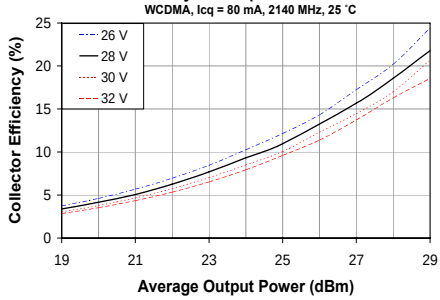
Gain vs. Frequency vs. Temperature
WCDMA, Vcc = 28V, Icq = 80 mA, +27 dBm Pout



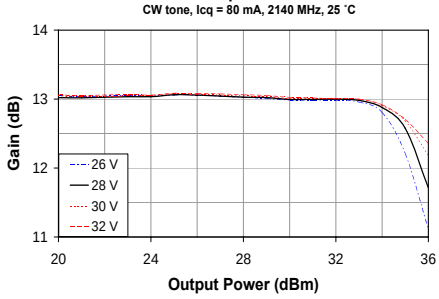
ACLR1 vs. Output Power vs. Vcc
WCDMA, Icq = 80 mA, 2140 MHz, 25 °C



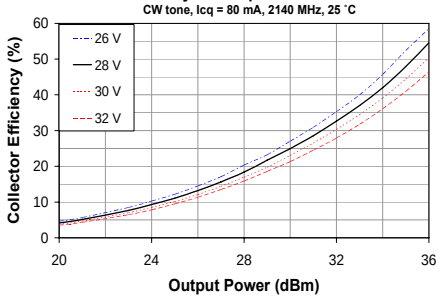
Efficiency vs. Output Power vs. Vcc
WCDMA, Icq = 80 mA, 2140 MHz, 25 °C



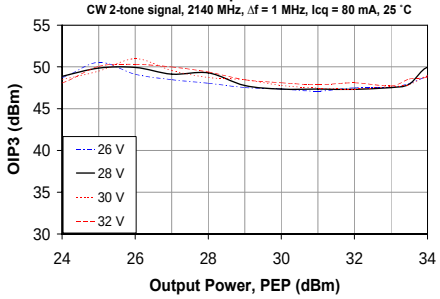
Gain vs. Output Power vs. Vcc
CW tone, Icq = 80 mA, 2140 MHz, 25 °C



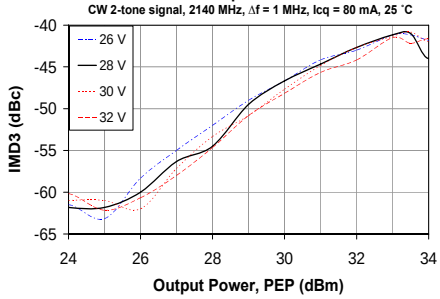
Efficiency vs. Output Power vs. Vcc
CW tone, Icq = 80 mA, 2140 MHz, 25 °C



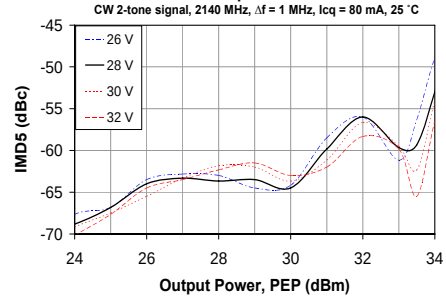
OIP3 vs. Output Power vs. Vcc
CW 2-tone signal, 2140 MHz, Δf = 1 MHz, Icq = 80 mA, 25 °C



IMD3 vs. Output Power vs. Vcc
CW 2-tone signal, 2140 MHz, Δf = 1 MHz, Icq = 80 mA, 25 °C



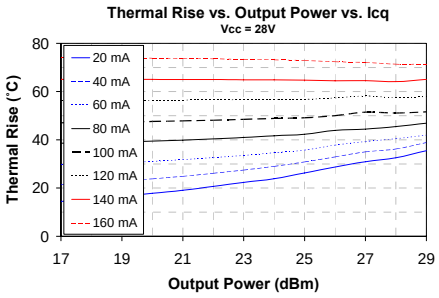
IMD5 vs. Output Power vs. Vcc
CW 2-tone signal, 2140 MHz, Δf = 1 MHz, Icq = 80 mA, 25 °C

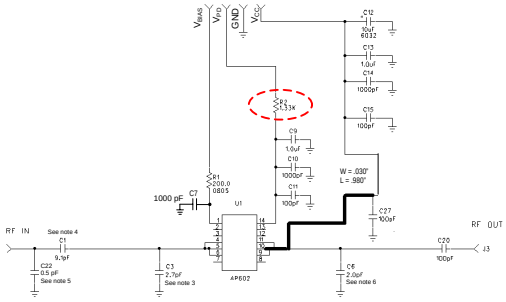


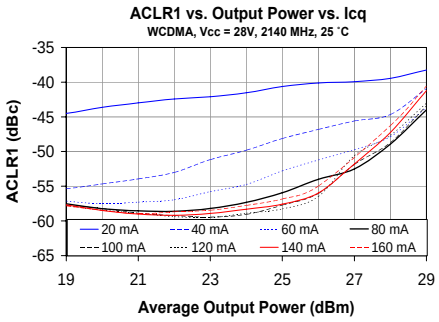
2110-2170 MHz Application Note: Changing Icq Biasing Configurations

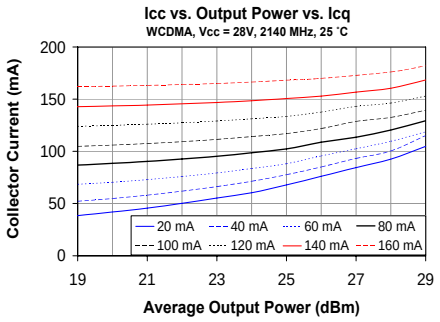
The AP602 can be configured to operate with lower bias current by varying the bias-adjust resistor – R2. The recommended circuit configurations shown previously in this datasheet have the device operating with a 80 mA as the quiescent current (I_{CQ}). This biasing level represents the best tradeoff in terms of linearity and efficiency. Lowering I_{CQ} will improve upon the efficiency of the device, but degraded linearity. Increasing I_{CQ} has nominal improvement upon the linearity, but will degrade the device's efficiency. Measured data shown in the plots below represents the AP602 measured and configured for 2.14 GHz applications. It is expected that variation of the bias current for other frequency applications will produce similar performance results.

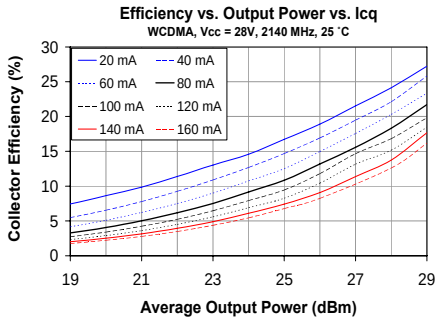
Icq (mA)	R2 (ohms)	V_{PD} (V)	PIN_V_{PD} (V)
20	6.00k	5	2.53
40	2.76k	5	2.61
60	1.80k	5	2.67
80	**1.33k**	**5**	**2.73**
100	1.05k	5	2.79
120	859	5	2.84
140	723	5	2.89
160	621	5	2.94

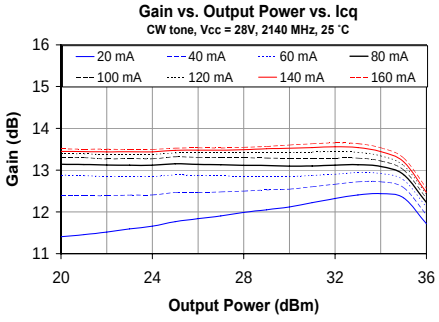


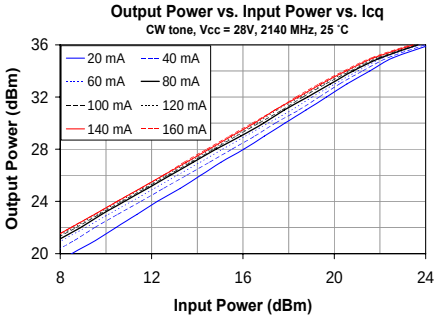


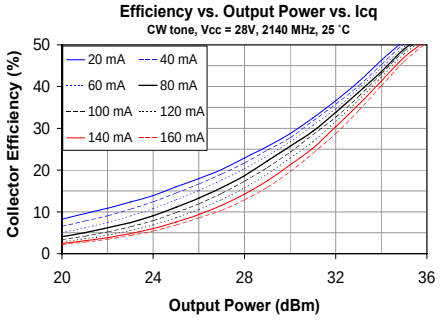


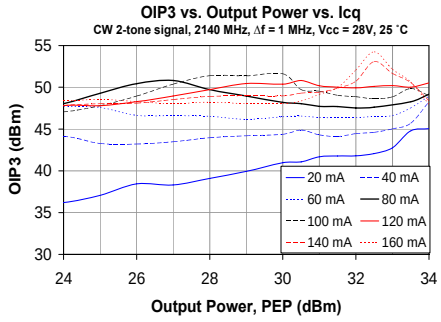


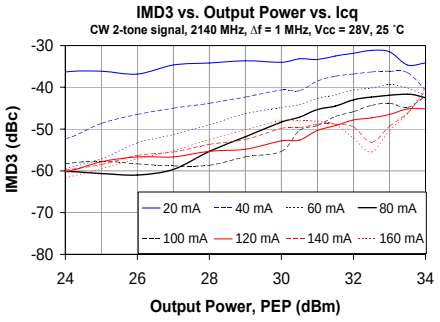


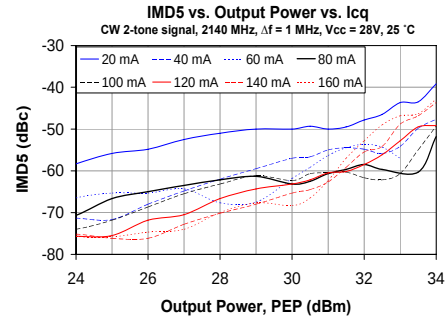








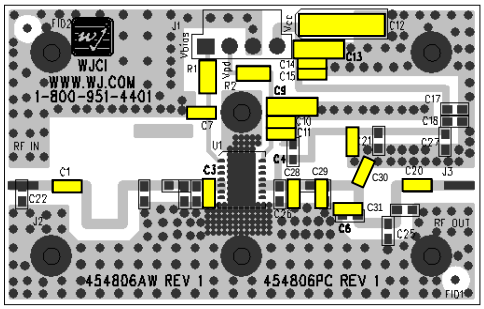


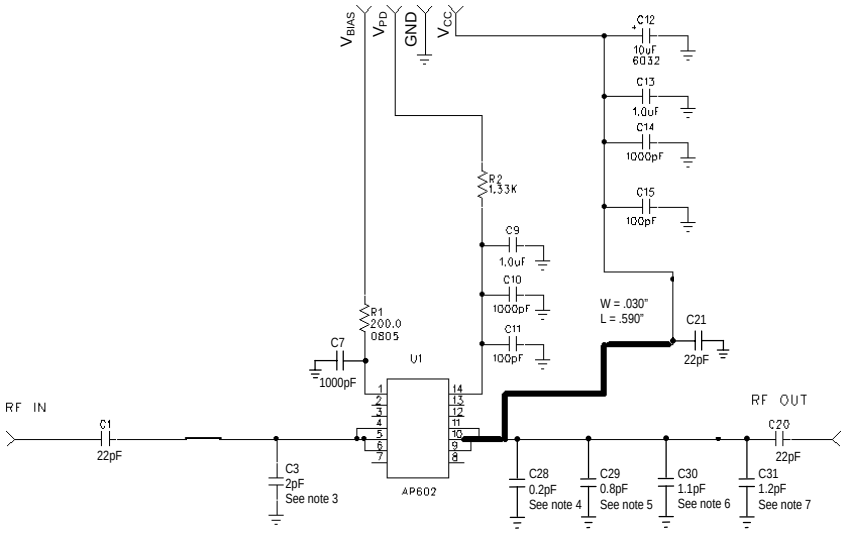


2320-2380 MHz WiBro Application Circuit

Typical WCDMA Performance at 25 °C at an output power of +27 dBm

Frequency	2350 MHz
Total Output Power	+27 dBm
Power Gain	13 dB
ACLR	-49 dBc
Operating Current, Icc	110 mA
Collector Efficiency	15.8 %
Output P1dB	+36 dBm
Quiescent Current, Icq	80 mA
Vpd, Vbias	+5 V
Vcc	+28 V

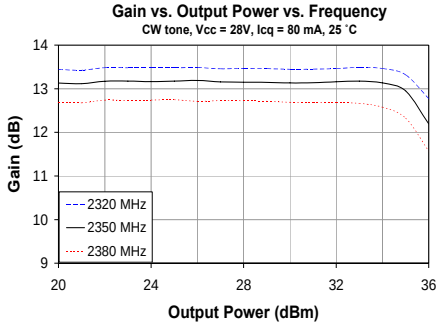


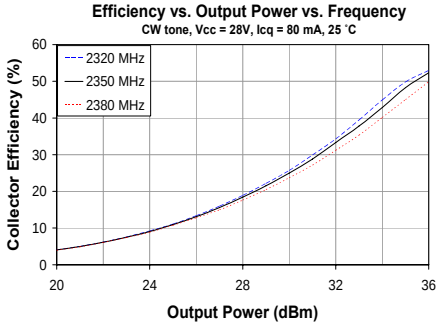


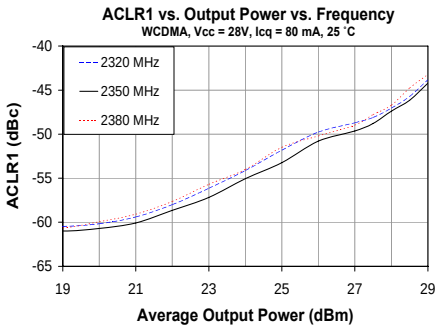
Notes:
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. The center of C3 is placed at 0.050" (5.1° @ 2.35 GHz) from the edge of the AP602 (U1).
4. The center of C28 is placed at 0.130" (13.3° @ 2.35 GHz) from the edge of the AP602 (U1).
5. The center of C29 is placed at 0.110" (11.3° @ 2.35 GHz) from the center of C28.
6. The center of C30 is placed at 0.165" (16.9° @ 2.35 GHz) from the center of C29.
7. The center of C31 is placed at 0.110" (11.3° @ 2.35 GHz) from the center of C30.
8. The bold-faced RF trace is for the DC bias feed. The stub's length is approximately a ¼ λ.

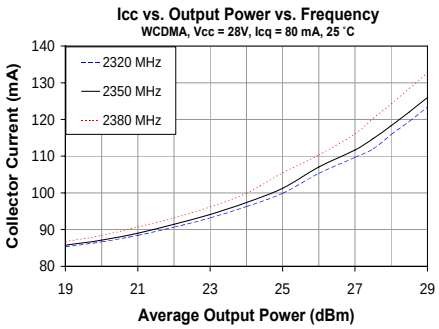
2320-2380 MHz Application Circuit Performance Plots

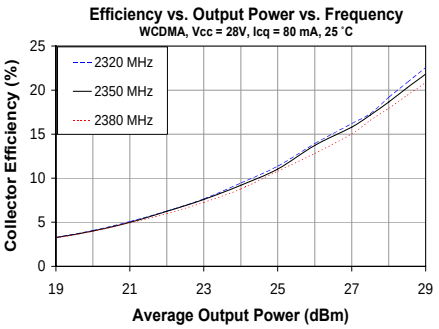
W-CDMA 3GPP Test Model 1+64 DPCH, 60% clipping, PAR = 8.6 dB @ 0.01% Probability, 3.84 MHz BW







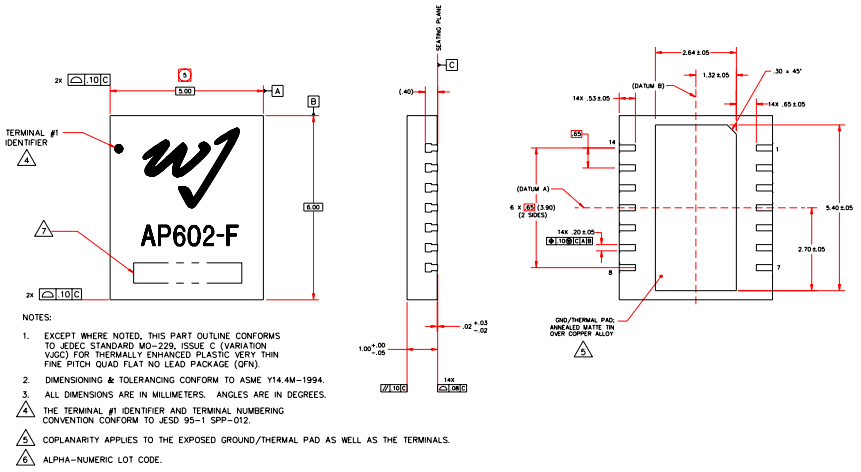




AP602-F Mechanical Information

This package is lead-free and RoHS-compliant. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes. The plating material on the pins is annealed matte tin over copper.

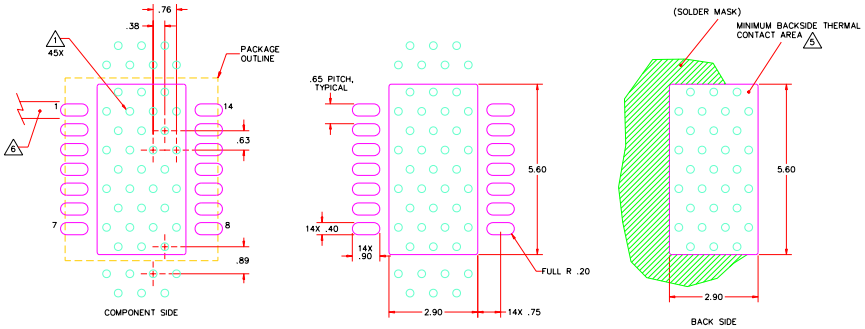
Outline Drawing



NOTES:

1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO-229, ISSUE C (VARIATION VJCC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE (QFN).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION CONFORM TO JESD 95-1 SPP-012.
5. COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS.
6. ALPHA-NUMERIC LOT CODE.

Mounting Configuration / Land Pattern

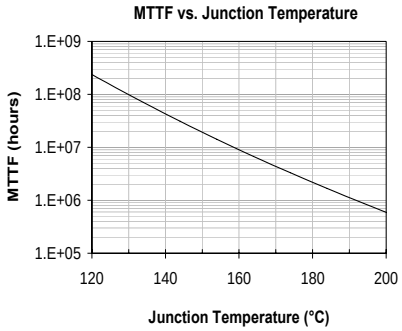


NOTES:

1. GROUND/THERMAL VIAS ARE CRITICAL FOR THE PROPER PERFORMANCEOF THIS DEVICE. VIAS SHOULD USE A .35mm (#80/.0135") DIAMETER DRILL AND HAVE A FINAL PLATED THRU DIAMETER OF .25mm (.010").
2. ADD AS MUCH COPPER AS POSSIBLE TO INNER AND OUTER LAYERS NEAR THE PART TO ENSURE OPTIMAL THERMAL PERFORMANCE.
3. TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE-TO-GROUND PAD SOLDER JOINT IS CRITICAL.
4. ADD MOUNTING SCREWS NEAR THE PART TO FASTEN THE BOARD TO A HEATSINK. ENSURE THAT THE GROUND/THERMAL VIA REGION CONTACTS THE HEATSINK.
5. DO NOT PUT SOLDER MASK ON THE BACK SIDE OF THE PC BOARD IN THE REGION WHERE THE BOARD CONTACTS THE HEATSINK.
6. RF TRACE WIDTH DEPENDS UPON THE PC BOARD MATERIAL AND CONSTRUCTION.
7. USE 1 OZ. COPPER MINIMUM.
8. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
9. A HEATSINK UNDERNEATH THE AREA OF THE PCB FOR THE MOUNTED DEVICE IS STRICTLY REQUIRED FOR PROPER THERMAL OPERATION. DAMAGE TO THE DEVICE CAN OCCUR WITHOUT THE USE OF ONE.

Thermal Specifications

Parameter	Rating
Thermal Resistance, Θ_{JC} Referenced from peak junction to the center of the bottomside ground paddle	16.6 °C / W
Junction Temperature, T_J For 10^6 hours MTTF	192 °C
Max Junction Temperature, $T_{J,max}$ For catastrophic failure	250 °C

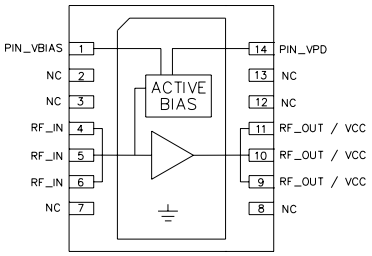


Product Marking

The component will be laser marked with an "AP602-F" product label with an alphanumeric lot code on the top surface of the package.

Tape and reel specifications for this part will be located on the website in the "Application Notes" section.

Functional Pin Layout



Pin	Function
1	PIN_VBIAS
2, 3, 7, 8, 12, 13	N/C
4, 5, 6	RF IN
9, 10, 11	RF Output / Vcc
14	PIN_VPD
Backside paddle	GND

MSL / ESD Rating

Caution! ESD sensitive device.

ESD Rating: Class 1B
Value: Passes ≥ 500V to <1000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ≥ 1000V to <2000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating: Level 3 at +260 °C convection reflow
Standard: JEDEC Standard J-STD-020