ALPHA & OMEGA
SEMICONDUCTOR

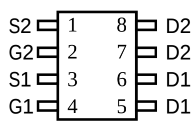
AOP800
Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

The AOP800 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications. *Standard Product AOP800 is Pb-free (meets ROHS & Sony 259 specifications). AOP800L is a Green Product ordering option. AOP800 and AOP800L are electrically identical.*

Features

V_{DS} (V) = 30V
I_D = 9.3A (V_{GS} = 10V)
$R_{DS(ON)}$ < 18mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 28mΩ (V_{GS} = 4.5V)



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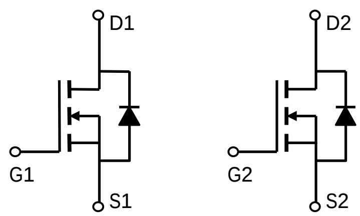

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [A]	T_A=25°C	I_D	9.3	A
	T_A=70°C		7.5	
Pulsed Drain Current [B]		I_{DM}	40	
Power Dissipation	T_A=25°C	P_D	2.5	W
	T_A=70°C		1.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	40	50	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		67	80	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	33	40	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V		30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=24V, V_{GS}=0V				1	µA
			T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V				100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA		1	1.8	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V		40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=9.3A			15.5	18	mΩ
			T_J=125°C		22.3	27	
		V_{GS}=4.5V, I_D=7.4A			23	28	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=9.3A			23		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V			0.75	1	V
I_S	Maximum Body-Diode Continuous Current					3	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz			1040	1250	pF
C_{oss}	Output Capacitance				180		pF
C_{rss}	Reverse Transfer Capacitance				110		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz			0.7	0.85	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=9.3A			19.2	24	nC
Q_g(4.5V)	Total Gate Charge				9.36		nC
Q_{gs}	Gate Source Charge				2.6		nC
Q_{gd}	Gate Drain Charge				4.2		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.6Ω, R_{GEN}=3Ω			5.2		ns
t_r	Turn-On Rise Time				4.4		ns
$t_{D(off)}$	Turn-Off DelayTime				17.3		ns
t_f	Turn-Off Fall Time				3.3		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=9.3A, dI/dt=100A/µs			16.7	22	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=9.3A, dI/dt=100A/µs			6.7		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t≤ 10s thermal resistance rating.
B: Repetitive rating, pulse width limited by junction temperature.
C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
D. The static characteristics in Figures 1 to 6 are obtained using 80µs pulses, duty cycle 0.5% max.
E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

Rev3: August 2005

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

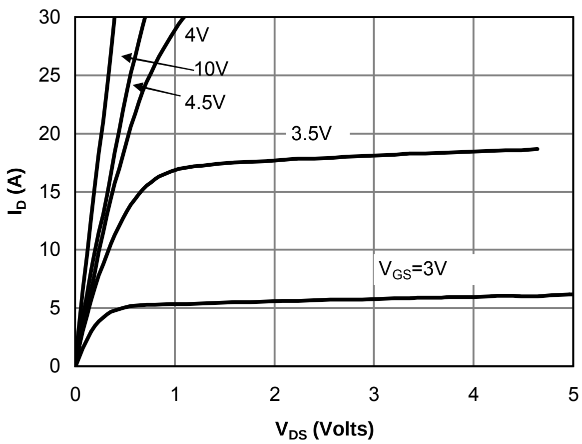

Fig 1: On-Region Characteristics

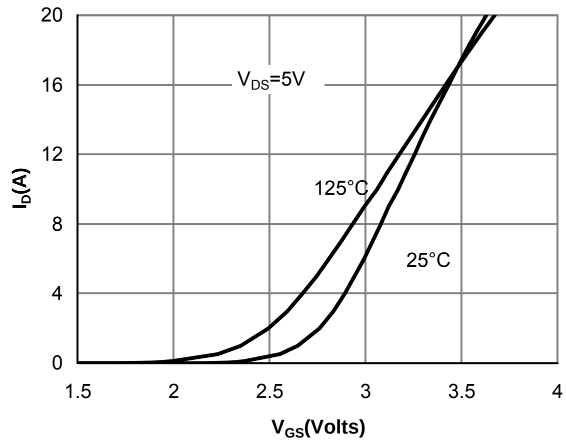

Figure 2: Transfer Characteristics

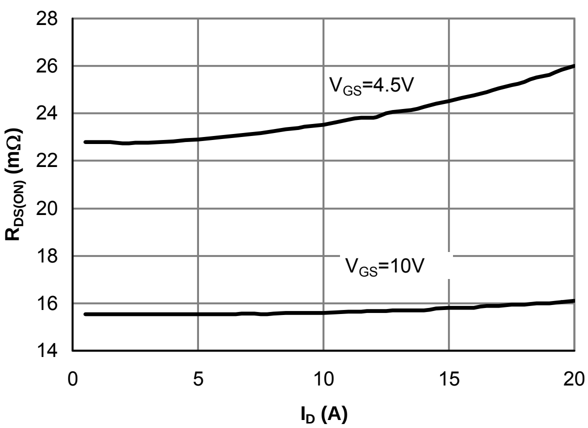

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

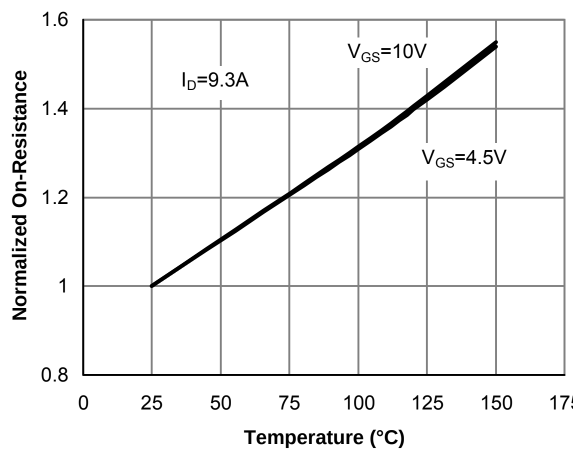

Figure 4: On-Resistance vs. Junction Temperature

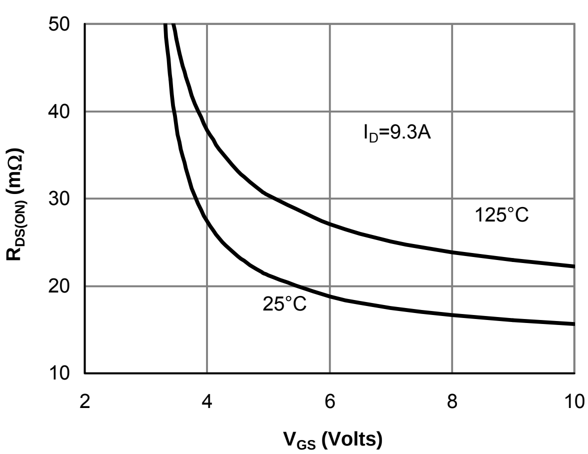

Figure 5: On-Resistance vs. Gate-Source Voltage

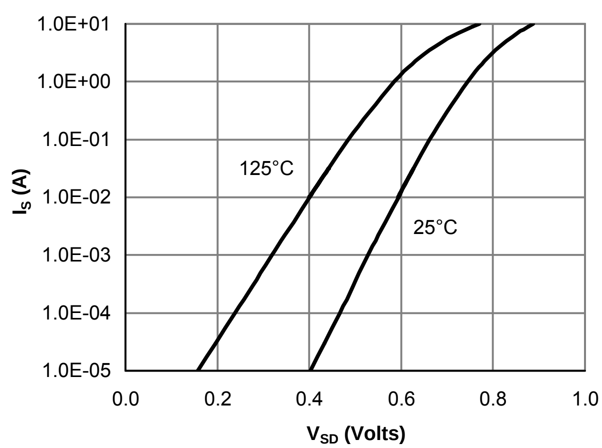

Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

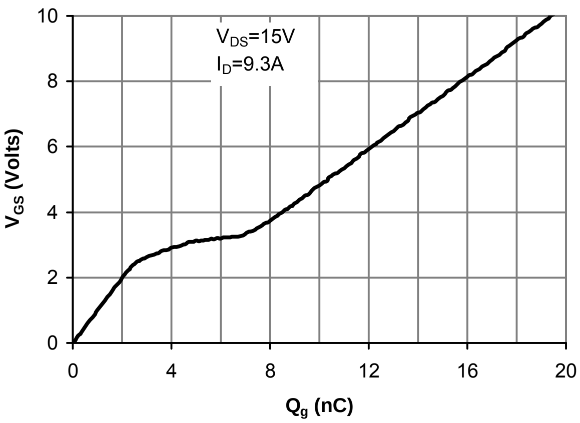

Figure 7: Gate-Charge Characteristics

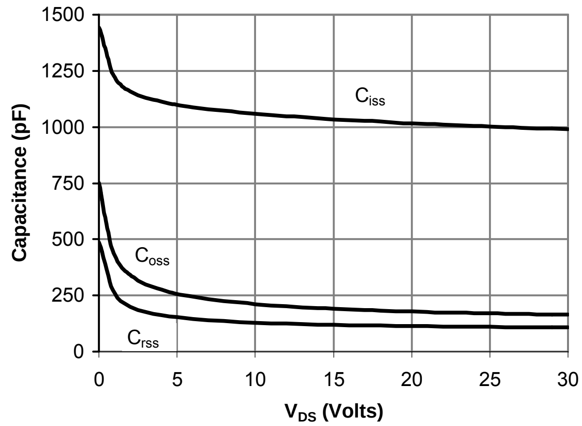

Figure 8: Capacitance Characteristics

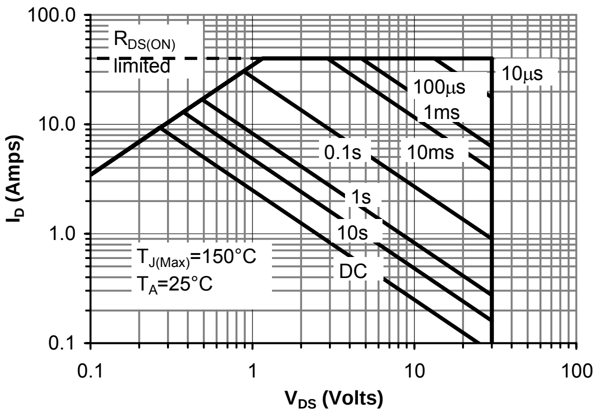

Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

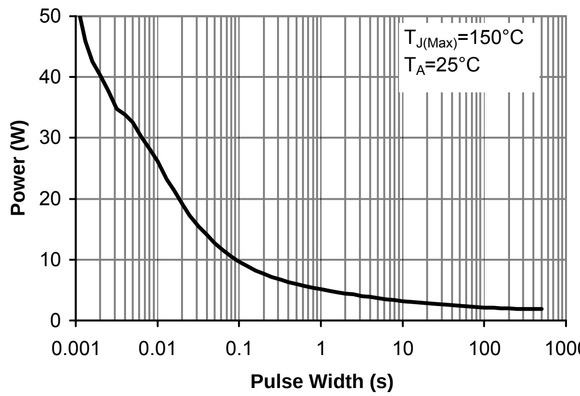

Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

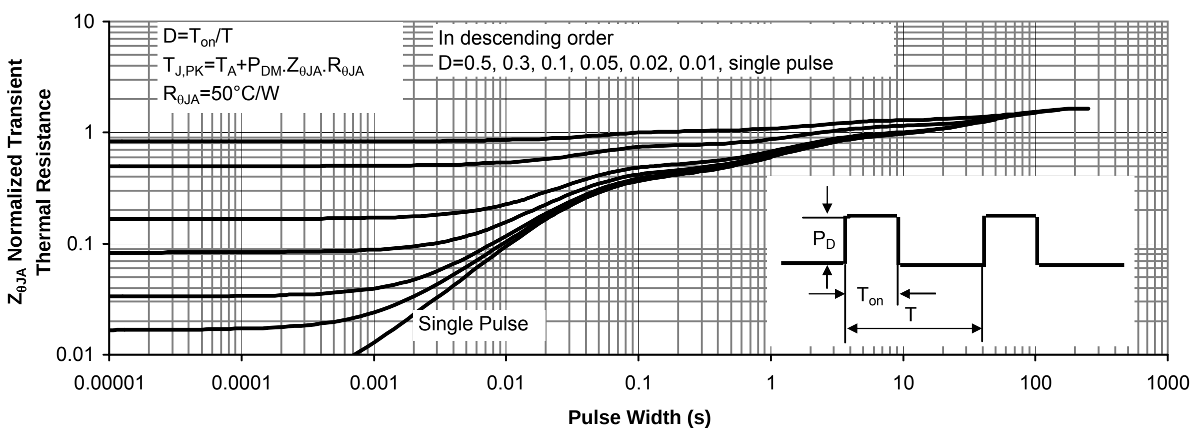

Figure 11: Normalized Maximum Transient Thermal Impedance