AMIS710401-A4: 400dpi CIS Module

Red 600nm LED Light Source

Data Sheet

1.0 General Description

The AMIS-710401-A4 (PI401MC-A4) is a contact image sensor (CIS) module using MOS image sensor technology for high-speed performance and high sensitivity. These CIS modules contain a complete optical imaging system that includes the light source and focusing elements.

The MOS image sensors are mounted on a printed circuit board (PCB) and housed in an A4 size module. They contain video processing circuits, allowing for high scanning speeds. The module comes with its LED light source, which provides the light power. Since the light power limits the exposure, which is proportional to the product of scanning speed and light power, the module's maximum scanning speed and signal output voltage are limited, in this case with the Red light source, to a 5.5MHz clock rate.

The module is designed for scanning A4 size (216mm) documents with 16 dots per millimeter (dpm) resolution. Applications include document scanning, mark readers, gaming and office automation equipment.

2.0 Key Features

- LED light source, lens and sensor are integrated into a single module
- 660nm LED light source
- Analog video, pixel rate as high as 5.5MHz
- 630μsec/line minimum scanning speed @ maximum of 5.5MHz clock rate
- 16 dots/mm resolution, 216mm scanning length
- Wide dynamic range
- Standard A4 size ≅ 14.5mm x 19.5mm x 232mm
- Low power
- Light weight

3.0 Functional Description

Each of the modules consists of 27 AMIS-720442 (PI3042) image sensors, serially cascaded together. Each sensor consists of 128 photo-sensing elements (pixels), resulting in a module with a length of 3456 pixels.

These image sensors, which are cascaded in a sequence to form a single line array, contain associated multiplex switches, which are sequentially accessed with its digital shift register. Each register has a chip-select switch, which activates its shift register upon the completion of its preceding sensor's scan. In turn, after completing its own scan the register activates its successor's register. The start pulse initiates the shift register of the first chip in the line array. The first chip then sequentially clocks out the integrated charges proportional to the image on the selected pixel site. These charges are passed through the sensors' multiplexing switch and then out onto the video line, where these charges are converted to a proportional voltage signal pulse. When the first sensor completes its scan, the chip-select switch on the following chip is switched on to continue its line scan. This process continues until the module completes its scan. A new scan is initiated when a start pulse is again entered into the first chip of each section.

The 27 sensors are cascaded together and bonded onto a PCB. They share a common clock line. Their shift registers have end-of-line pulses that are connected to the following sensor's register start input. Their video output shares a common video line. This video line forms a storage capacitance, which is buffered by a video amplifier that functions as an output video driver. The charge from each output is integrated onto the video line capacitance and readout. Then, each pixel is reset and ready to integrate the following pixel charge.

Mounted in the module is a one-to-one graded indexed micro lens array, which focuses the images on scanned documents onto the sensors' sensing plane, where it the images are converted to proportional electrical charges.

Illumination is accomplished by means of single line array of Red 660nm LED light sources. The LED chips are mounted on a PCB then bonded in appropriate combinations to provide a 5.0V input light source.

All components are housed in a small plastic housing, which has a glass cover that acts as the focal point for the object being scanned, protecting the imaging array, micro lens assembly, and LED light source from dust.

Figure 1 and Figure 2 show a block diagram and a cross section of a module.

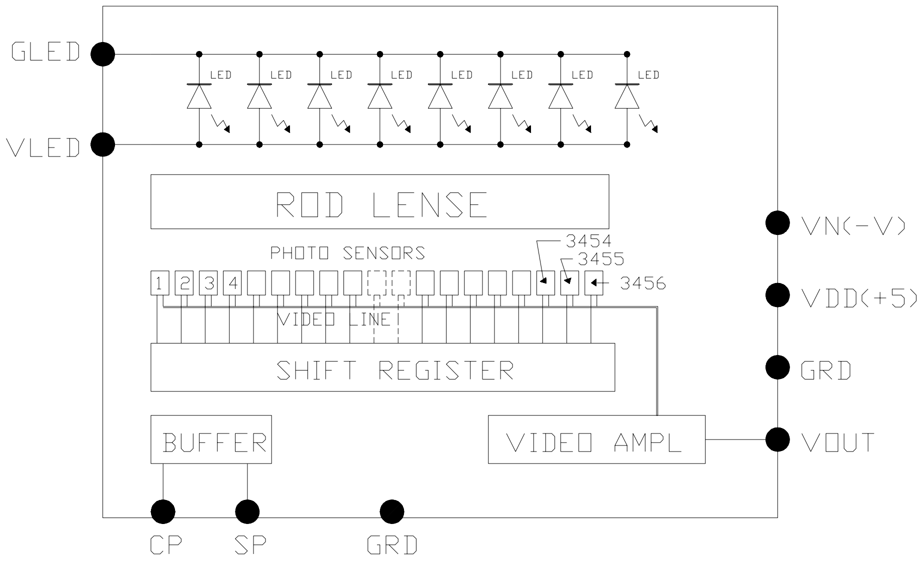

Figure 1: Module Block Diagram

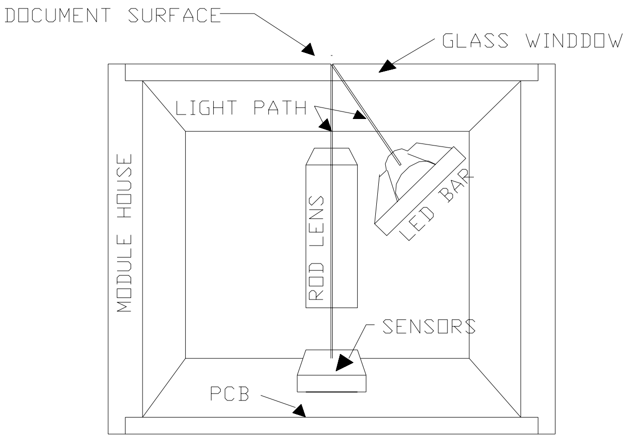

Figure 2: Module Cross Section

4.0 Connector Pin Out

Inputs and outputs to the module are accomplished via a 10-pin connector, part number JAE IL-Z-10P-S125L3-E, located on one end of the module.

Table 1 lists the connector pin out with its symbols and descriptions.

Table 1: Pin Out Configuration

Connector Pin Number	Symbol	Description
1	VOUT	Analog video output
2	GND	Ground, 0V
3	VDD (+5V)	Power supply
4	VN (-5V to -12V)	Negative power supply
5	GND	Ground, 0V
6	SP (START)	Shift register start pulse
7	GND	Ground
8	CP (CLOCK)	Clock pulse
9	GLED	Ground for the light source, 0V
10	VLED	Power supply for the light source

Table 2 shows the absolute maximum ratings for the parameters. Table 3 shows the absolute maximum for the LED light source. These are the absolute maximum ratings and continuous operation is not recommended.

5.0 Absolute Maximum Rating

Table 2: Absolute Maximum Ratings

Parameter	Symbol	Max. Rating	Units
Power supply	Vdd	7	V
	Idd	100	mA
	Vn	|-15|	V
	In	10	mA
Input clock pulse (high level)	Vih	Vdd - 0.5V	V
Input clock pulse (low level)	Vil	|-0.5|	V

Table 3: LED Absolute Maximum Ratings

Parameter	Max. Rating	Units
AMIS-710401-A4 660nm Red LED		
VLED	5.5	V
ILED	0.7	A

6.0 Environmental Specifications

Table 4 lists the environmental conditions for the modules.

Table 4: Operating and Storage Environment

Parameter	Max. Rating	Units
Operating temperature	0 to +50	°C
Operating humidity	10 to 90	%
Storage temperature	-20 to +75	°C
Storage humidity	10 to 90	%

7.0 Electro-Optical Characteristics at 25°C

Table 5 lists the fixed geometrical electro-optical characteristics. Table 6 shows the factory adjustable specification characteristics constrained to the limits of the test target and the LED light source.

Table 5: Fixed Geometrical Electro-Optical Characteristics

Parameter	Value	Units
Total number of pixels in each module	3456	Elements
Pixel-to-pixel spacing	62.5	μm

7.1 Module: AMIS-710401-A4; Light Source: 660nm Red LED

Table 6: AMIS-710401-A4 / 660nm Red LED Electro-Optical Characteristics

Parameter	Symbol	Value	Units	Note
Line scanning rate (1)	Tint	692	μsec	@ 5.0MHz clock frequency
Clock frequency(2)	Fclk	5.0	MHz	
Bright output voltage(3)(7)	Video output	1.25±0.25	V	
Bright output non-uniformity(4)	Up	< ±30	%	
Adjacent photo-response non-uniformity(5)	Upn	<25	%	
Dark non-uniformity(6)	Ud	< 150	mV	
Dark output voltage(7)	Dark level (DL)	< 100	mV	
Modulation transfer function(8)	MTF	> 40	%	

Notes:

(1) Tint is the line-scanning rate or integration time and is determined by the interval between two start pulses (SP). The integration time is factory adjusted to give 1.25V output with the maximum clock frequency of 5MHz. However, a minimum integration of 630μs is with a maximum 5.5MHz clock frequency.
(2) Fclk is the main clock frequency and also equals the pixel rate.
(3) Video output level is dependent on the Integration time and the LED light power.
(4) Up = [Vp(max) - Vpavg] / Vpavg x 100% or [Vpavg - Vp(min)] / Vpavg} x 100%, whichever is greater.
Where Vp(max) = maximum pixel level, Vp(min) = minimum pixel level, and Vpavg = average of all pixels.
(5) Adjacent photo-response non-uniformity (Upn)
(6) Upn = Max ((Vpn – Vpn+1) / Min (Vpn, Vpn+1)) x 100%, where Vpn is the pixel output voltage of Pixel n in the light.
(7) Ud = Vdmax - Vdmin, where Vdmin is the minimum output voltage with the LED off and Vdmax is maximum output voltage with the LED on.
(8) See the paragraph in Section 9.0 for explanation.
(9) See the paragraph in Section 10.0. A graph of the typical MTF vs Depth of Focus is shown.

8.0 Recommended Operating Conditions at 25°C

Table 7 lists the recommended operating conditions. Table 8 lists the recommended operating conditions for t he LED light source.

Table 7: Recommended Operating Conditions at 25°C

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply	Vdd (positive)	4.5	5.0	5.5	V
	Vn (negative)	-12	-5	-4.5	V
	Idd (positive)	14	17	20	mA
	In (negative)	8	9	10	mA
Input voltage (high level)	Vih	Vdd - 1.0	Vdd - 0.5	Vdd	V
Input voltage (low level)	Vil	0		0.6	V
Clock frequency (1)	Fclk	0.346		5.5	MHz
Clock pulse high duty cycle	Duty	25			%
Clock pulse high duration	Pwck	46			ns
Integration time(1)	Tint	630		10000	μs
Operating temperature	Top	0	25	50	°C

Table 8: Recommended Operating Conditions at 25°C

LED Light Source	Parameter	Min.	Typ.	Max.	Units
660nm Red LED	VLED		5.0	5.5	V

Note:

(1) The maximum clock speed is limited by the LED power of the modules' light source.
The minimum clock speed is determined by the longest tolerable integration time. Because of the leakage current build up, the integration time is recommended to be no greater than 10ms.

9.0 Reset Level and Video Sampling Time

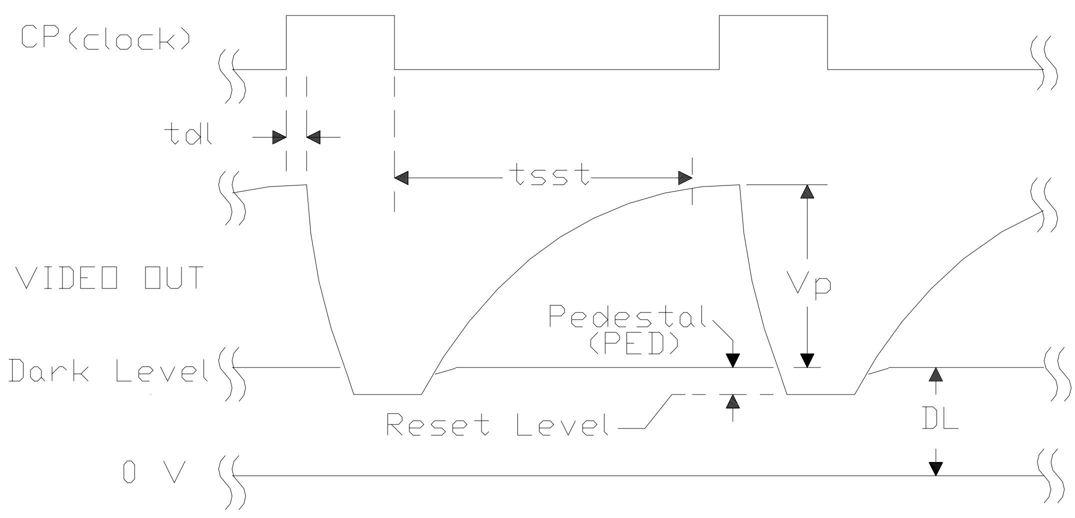

Figure 3: Reset Level and Sample Time

Figure 3 shows the video signal waveform and details a single pixel. The signal output waveform is shown referenced to the input clock waveform. Also shown is the terminology used to define the dark and bright output levels, Vp, and the recommended pixel sampling times, tsst. Also shown is the clock to video reset time delay, tdl.

The dark level is defined by using the module imaging on a black target or with the light source turned off. The dark level is then measured from ground or 0V. The reset level is a reference level of the reset switch, which is not necessarily at ground. The reason for this is that after the reset operation, the video signal is passed through an amplifier, which may have some offsets. The difference between the dark level and reset level is called the pedestal, PED. Hence, the reset level will sit below the dark level.

The video pixels demonstrated in this graph are ideal waveforms from a CIS module, using a phototransistor imaging structure. The video output at high speeds, such as 5.0MHz, does not instantly rise to its final value, although if it is given enough time it would eventually approach its steady state value (in order of milliseconds). However, at high speeds it is impractical to wait until a final stable value is reached. The suggested sampling point, tsst, is therefore a few nanoseconds prior to the signal falling edge of Vp.

10.0 Depth of Focus

Figure 4 shows two graphs of typical MTF versus Distance, which can be used to define the working depth-of-focus (DOF). The two curves indicate the spread among the production modules. Note that the MTF is greater than 50 percent between the 0.0mm and 0.1mm depth. Distances greater than 0.1mm from the glass surface are still usable, but discretion must be used in its application. Since this module is a 400dpi module, the MTF was measured with a 400dpi or a 200 line-pair per inch optical bar pattern. The test was conducted with the pixel rate set to 5.0MHz.

The effective algorithm used in the measurements is as described by the following equation:

$$MTF=\{[Vp(n)+Vp(n+1)]/2-[Vp(n+2)+Vp(n+3)]/2\}/\{[Vp(n)+Vp(n+1)]/2+[Vp(n+2)+Vp(n+3)]/2\}$$

Where n is 1, 2, ...3456th, Vp(n) is the signal amplitude of the nth pixel.

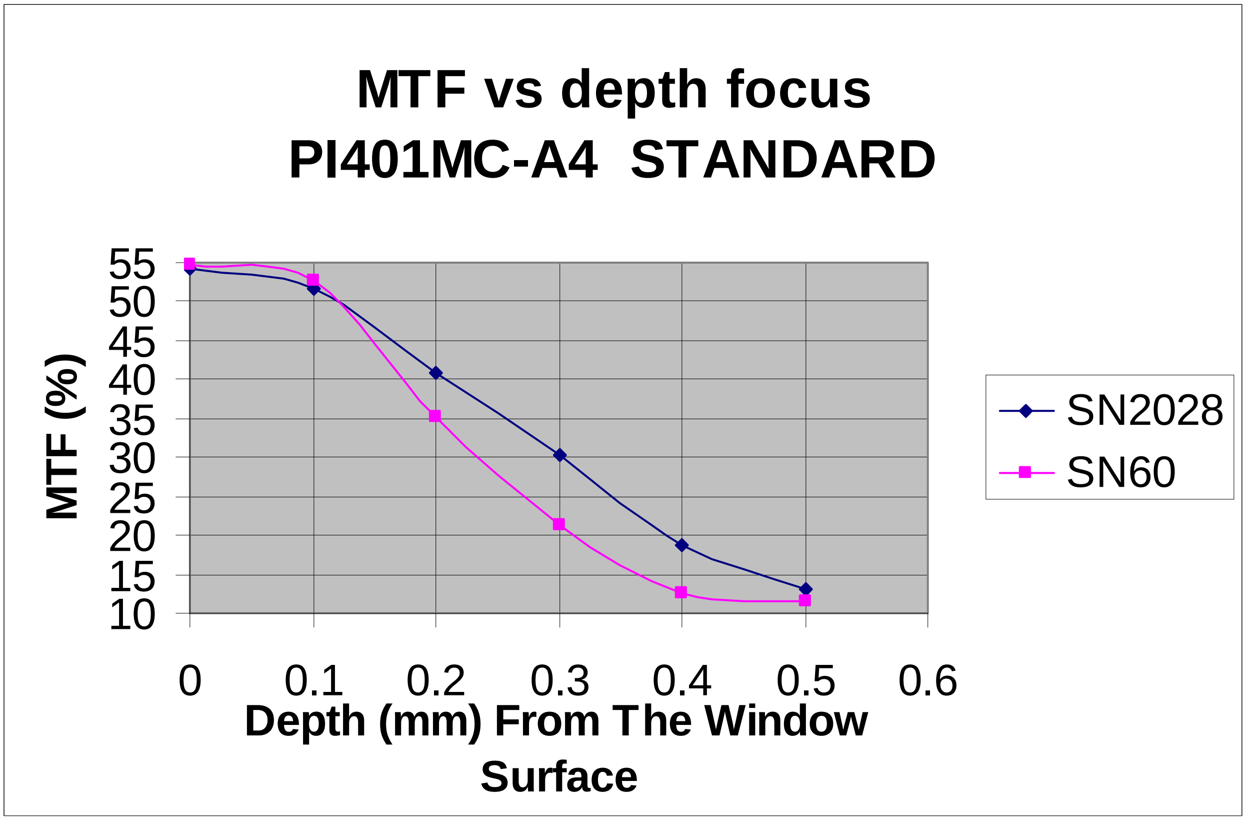

Figure 4: Typical MTF versus Distance

11.0 Timing Characteristics at 25°C

The timing characteristics at 25°C for the I/O clocks are shown in Figure 5 and their definitions are detailed in Table 9.

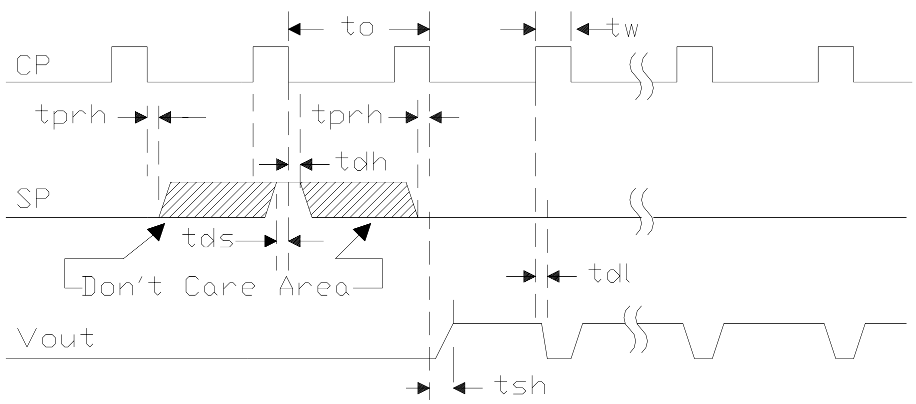

Figure 5: Module Timing Diagram

Table 9: Timing Definitions

Item	Symbol	Min.	Typ.	Max.	Units
Clock cycle time	to	0.182		2.9	µs
Clock pulse width	tw	46		730	ns
Clock duty cycle		25		75	%
Prohibit crossing time of the SP(1)	tprh	84			ns
Data setup time	tds	86			ns
Data hold time	tdh	94			ns
Signal delay time	tdl	50			ns
Signal settling time	tsh	100			ns

Note:

(1) "Prohibit crossing of the SP", tprh, is to indicate that the start pulse should not be active high between two consecutive low going clock pulses. All falling clock edges under an active high start pulse loads the internal shift register, therefore the start pulse must be active over only one falling clock edge. A high start pulse crossing over any rising clock edges are ignored by the shift register. One simple way to ensure that the start pulse will not be actively high for any two consecutive falling clock edges is to generate the start pulse on a rising clock edge and terminate it on the following rising clock edge.

12.0 Mechanical Structure of the Module

Figure 6 is an overview of the module housing, showing its connector location, its approximate overall dimensions and its general layout. It is not intended for use as a design reference. A detailed drawing for AMIS-710401-A4 module housing is available upon request.

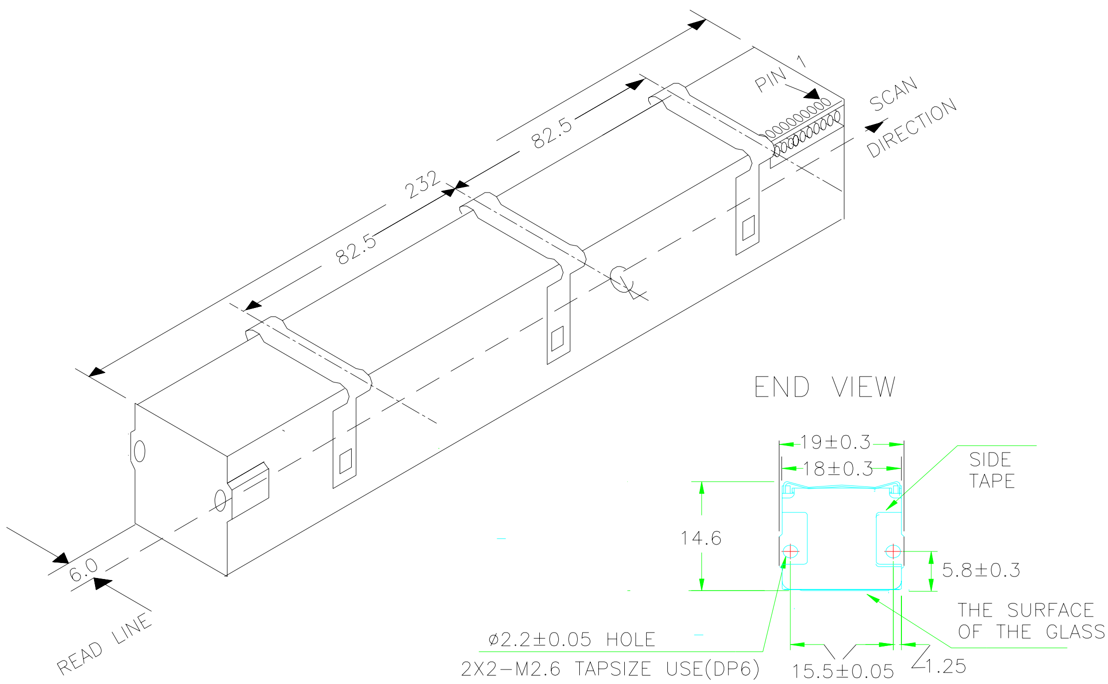

Figure 6: Module Mechanical Overview

13.0 Company or Product Inquiries

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