QUAD/DUAL N-CHANNEL ENHANCEMENT MODE EPAD® MATCHED PAIR MOSFET ARRAY

$V_{GS(th)}$= +1.4V

GENERAL DESCRIPTION

ALD110814/ALD110914 are monolithic quad/dual N-Channel MOSFETs matched at the factory using ALD's proven EPAD® CMOS technology. These devices are intended for low voltage, small signal applications.

The ALD110814/ALD110914 MOSFETs are designed and built with exceptional device electrical characteristics matching. Since these devices are on the same monolithic chip, they also exhibit excellent tempco tracking characteristics. Each device is versatile as a circuit element and is a useful design component for a broad range of analog applications. They are basic building blocks for current sources, differential amplifier input stages, transmission gates, and multiplexer applications. For most applications, connect V- and N/C pins to the most negative voltage potential in the system and V+ pin to the most positive voltage potential (or left open unused). All other pins must have voltages within these voltage limits.

The ALD110814/ALD110914 devices are built for minimum offset voltage and differential thermal response, and they are designed for switching and amplifying applications in +1.5V to +10V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment.

The ALD110814/ALD110914 are suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the Field Effect Transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 30pA at room temperature. For example, DC beta of the device at a drain current of 3mA and input leakage current of 30pA at 25°C is = 3mA/30pA = 100,000,000.

FEATURES

- Enhancement-mode (normally off)
- Standard Gate Threshold Voltages: +1.4V
- Matched MOSFET to MOSFET characteristics
- Tight lot to lot parametric control
- Parallel connection of MOSFETs to increase drain currents
- Low input capacitance
- $V_{GS(th)}$ match to 10mV
- High input impedance — $10^{12}\Omega$ typical
- Positive, zero, and negative $V_{GS(th)}$ temperature coefficient
- DC current gain $>10^8$
- Low input and output leakage currents

ORDERING INFORMATION

Operating Temperature Range* 0°C to +70°C		0°C to +70°C	
16-Pin Plastic Dip Package	16-Pin SOIC Package	8-Pin Plastic Dip Package	8Pin SOIC Package
ALD110814PC	ALD110814SC	ALD110914PA	ALD110914SA

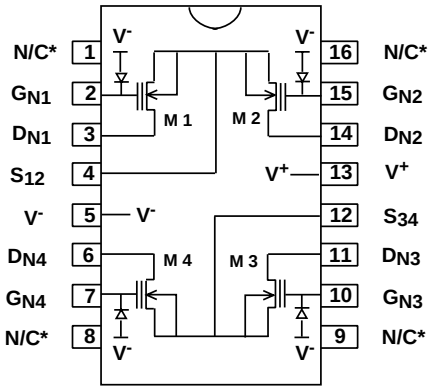
* Contact factory for industrial or military temp. ranges or user-specified threshold voltage values.

APPLICATIONS

- Precision current mirrors
- Precision current sources
- Voltage choppers
- Differential amplifier input stages
- Discrete voltage comparators
- Voltage bias circuits
- Sample and Hold circuits
- Analog inverters
- Level shifters
- Source followers and buffers
- Current multipliers
- Discrete analog multiplexers/matrices
- Discrete analog switches

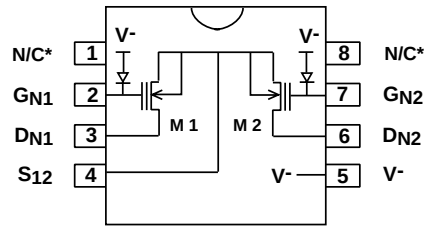
PIN CONFIGURATION

ALD110814



PC, SC PACKAGES

ALD110914



PA, SA PACKAGES

*N/C pins are internally connected.
Connect to V- to reduce noise

ABSOLUTE MAXIMUM RATINGS

Drain-Source voltage, V_{DS} ____ 10.6V
Gate-Source voltage, V_{GS} ____ 10.6V
Power dissipation ____ 500 mW
Operating temperature range PA, SA, PC, SC package ____ 0°C to +70°C
Storage temperature range ____ -65°C to +150°C
Lead temperature, 10 seconds ____ +260°C

OPERATING ELECTRICAL CHARACTERISTICS

V+ = +5V (or open) V- = GND T_A = 25°C unless otherwise specified

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

		ALD110814 / ALD110914				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Gate Threshold Voltage	$V_{GS(th)}$	1.38	1.40	1.42	V	I_{DS} =1μA V_{DS} = 0.1V
Offset Voltage $V_{GS(th)1}$-$V_{GS(th)2}$	V_{OS}		3	10	mV	I_{DS} =1μA
Offset VoltageTempco	TC ΔV_{OS}		5		μV/ °C	V_{DS1} = V_{DS2}
GateThreshold Voltage Tempco	TC$\Delta V_{GS(th)}$		-1.7 0.0 +1.6		mV °C	I_D = 1μA I_D = 20μA, V_{DS} = 0.1V I_D = 40μA
On Drain Current	$I_{DS\ (ON)}$		12.0 3.0		mA	V_{GS} = +10.6V V_{GS} = + 5.4V V_{DS} = + 5V
Forward Transconductance	G_{FS}		1.4		mmho	V_{GS} = +5.4V V_{DS} = +10.4V
Transconductance Mismatch	ΔG_{FS}		1.8		%	
Output Conductance	G_{OS}		68		μmho	V_{GS} = + 5.4V V_{DS} = +10.4V
Drain Source On Resistance	$R_{DS\ (ON)}$		500		Ω	V_{DS} = 0.1V V_{GS} = +4.0V
Drain Source On Resistance Mismatch	$\Delta R_{DS\ (ON)}$		0.5		%	V_{DS} = 0.1V V_{GS} = +5.4V
Drain Source Breakdown Voltage	BV_{DSX}	10			V	I_{DS} = 1.0μA V_{GS} = -0.4V
Drain Source Leakage Current[1]	$I_{DS\ (OFF)}$		10	100 4	pA nA	V_{GS} = +0.4V V_{DS} =10V, T_A = 125°C
Gate Leakage Current[1]	I_{GSS}		3	30 1	pA nA	V_{DS} = 0V V_{GS} = 10V T_A =125°C
Input Capacitance	C_{ISS}		2.5		pF	
Transfer Reverse Capacitance	C_{RSS}		0.1		pF	
Turn-on Delay Time	t_{on}		10		ns	V^+ = 5V R_L= 5KΩ
Turn-off Delay Time	t_{off}		10		ns	V^+ = 5V R_L= 5KΩ
Crosstalk			60		dB	f = 100KHz

Notes: [1] Consists of junction leakage currents