PRODUCT BRIEF

AHA G709D-40 FEC Core

40 GB/S ITU G.709 REED-SOLOMON DECODER

The G709D-40 core implements the 16 block interleaved RS(255,239) code specified by in Annex A of the ITU G.709 standard.

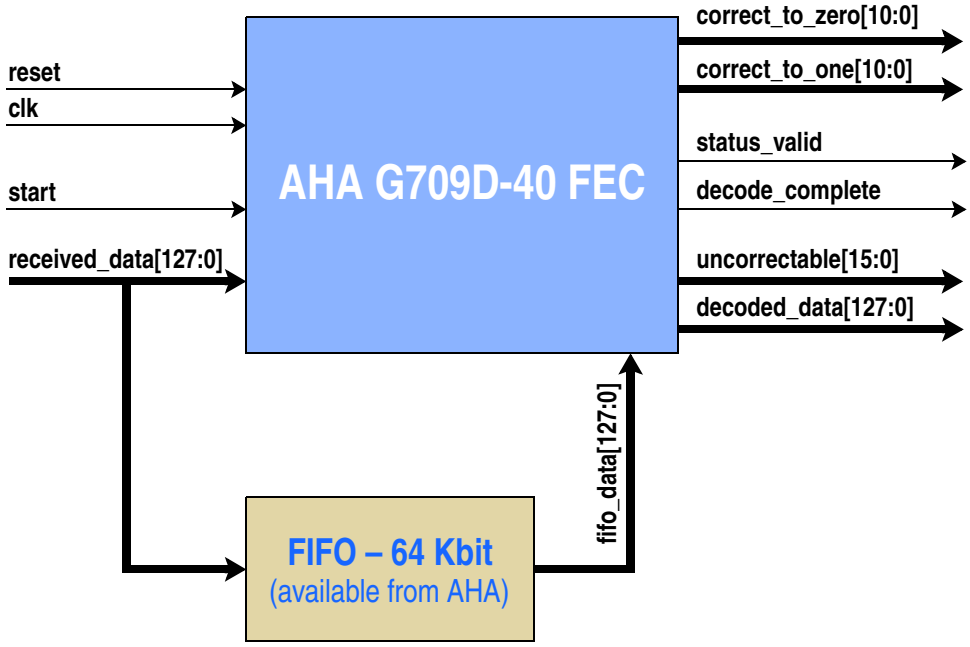
The G709D-40 core is specifically designed to efficiently perform the Reed-Solomon decoding function specified by the standard. The core requires no configuration, no initialization, and no re-synchronization procedure or includes any unnecessary features that would add area, power or complexity to your design.

A G709E Reed-Solomon encoder core is also available from AHA.

FEATURES

- ITU G.709 compatible Reed-Solomon core
- Input and output data streams are block-interleaved for seamless connection in G.709 system
- 40 Gbits/sec operation in 0.13µ CMOS process
- 220 Kgates in 0.13µ using a typical standard cell library
- One-edge, one-clock fully synchronous design without multi-cycle paths
- Separate FIFO for increased flexibility and simplified IC floor planning
- Complete error reporting for Bit Error Rate calculation and feedback into threshold detection circuits

Figure 1: AHA G709D-40 FEC



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INPUT SIGNALS

clk - 332 MHz core clock. All inputs are registered on the rising edge.

reset - Synchronous reset.

received_data[127:0] - Received data bus. Data bus is valid every clock and is registered on the rising edge of **clk**. The data frame is restarted whenever **start** is active. The core accepts 8-bytes per transfers

start - Signal is active to when the first 8 bytes of the G.709 frame in on the **received_data** bus. Must be inactive on all other data transfers in the frame. Maybe asserted at anytime of the data frame needs to be reset to the first transfer.

fifo_data[127:0] - FIFO data. Delay version of the **received_data** data stream. The bus is registered on the rising edge of **clk**.

OUTPUT SIGNALS

decode_complete - Decoding complete. Active when the first 8-byte transfer of the G.709 frame is on the **decode_data** data bus and inactive on all subsequent transfers.

decoded_data[127:0] - Decoded data. The first 8-bytes of the corrected G.709 frame are valid when **decode_complete** is active and the remainder of the frame is available over the subsequent 509 clocks. The data is driven from the rising edge of **clk**.

status_valid - Status valid signal. Active for a single **clk** following the completion of the frame to indicate when the **uncorrectable**, **correct-to-zero**, and **correct_to_one** signals are valid.

uncorrectable[15:0] - Uncorrectable block flags. Each bit of the signal corresponds to one of the 16 Reed-Solomon blocks in the G.709 frame. Valid when **status_valid** is active.

correct_to_zero[10:0] - Number of bits corrected from '1' to '0' in the just completed G.709 frame. Signal is valid when **status_valid** is active.

correct_to_one[10:0] - Number of bits corrected from '0' to '1' in the just completed G.709 frame. Signal is valid when **status_valid** is active.

DELIVERABLES

- G.709D-40 FEC core (VHDL)
- Timing constraints (DesignCompiler and Ambit format)
- Test bench and verification vectors (VHDL)
- Single use license to AHA's Reed-Solomon patents

PATENTS

Design uses one or more of the following US Patents: 5,170,399; 5,099,482; 4,873,688; 5,396,502

ABOUT AHA

Comtech AHA Corporation (AHA) develops and markets superior integrated circuits, boards, and intellectual property core technology for communications systems architects worldwide. AHA has been setting the standard in Forward Error Correction and Lossless Data Compression technology for many years and provides flexible, cost-effective solutions for today's growing bandwidth and reliability challenges. Comtech AHA Corporation is a wholly owned subsidiary of Comtech Telecommuncations Corp. (NASDAQ: CMTL). For more information, visit www.aha.com.

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