

AZ DISPLAYS, INC.

SPECIFICATIONS FOR LIQUID CRYSTAL DISPLAY

PART NUMBER:

AGM2416B

DATE:

September 13, 2005

1 General Specifications

Item	Standard Value	Unit
Display Pattern	<input checked="" type="checkbox"/> Dot-Graphic <input type="checkbox"/> Character <input type="checkbox"/> Digits <input type="checkbox"/> _____ <input type="checkbox"/> with ICON	Dots
Color	<input type="checkbox"/> Mono. <input type="checkbox"/> Grayscale <input checked="" type="checkbox"/> _FSTN_	
Module Dimension	92.0 X 71.8 X 2.0	mm
Viewing Area	67.0 X 46.8	mm
Active Area	62.38 X 42.38	mm
Character Size	/	mm
Character Pitch	/	mm
DOT Size	0.245 X 0.24	mm
DOT Pitch	0.265 X 0.26	mm
LCD Type	<input type="checkbox"/> TN, Positive <input type="checkbox"/> TN, Negative <input type="checkbox"/> HTN, Positive <input type="checkbox"/> HTN, Negative <input type="checkbox"/> STN, Yellow-Green <input type="checkbox"/> STN, Gray <input type="checkbox"/> STN, Blue <input checked="" type="checkbox"/> FSTN, Positive <input type="checkbox"/> FSTN, Negative <input type="checkbox"/> Color STN <input type="checkbox"/> FM LCD	
Polarizer Type	<input checked="" type="checkbox"/> Transflective <input type="checkbox"/> Transmissive <input type="checkbox"/> Reflective <input type="checkbox"/> Anti-Glare	
View Direction	<input checked="" type="checkbox"/> 6H <input type="checkbox"/> 12H <input type="checkbox"/> _____	
LCD Controller & Driver	ST8016 & ST8024	
LCD Driving Method	1/160duty, 1/14bias	
Interface Type	<input type="checkbox"/> I ² C <input type="checkbox"/> 4-wire Serial <input type="checkbox"/> 3-wire Serial <input type="checkbox"/> 6800 <input type="checkbox"/> 8080 <input checked="" type="checkbox"/> 4-bit <input type="checkbox"/> _____	
Backlight Type	/	
Backlight Color	/	
EL/CCFL Driver type	/	
DC-DC Converter	<input type="checkbox"/> Build-in <input checked="" type="checkbox"/> External	
Operation Temperature (°C)	-10 ~ 60 (T _{OPL} – T _{OPH})	°C
Storage Temperature (°C)	-20 ~ 70 (T _{STL} -- T _{STH})	° C

3.1 Pin Description

Segment Pin

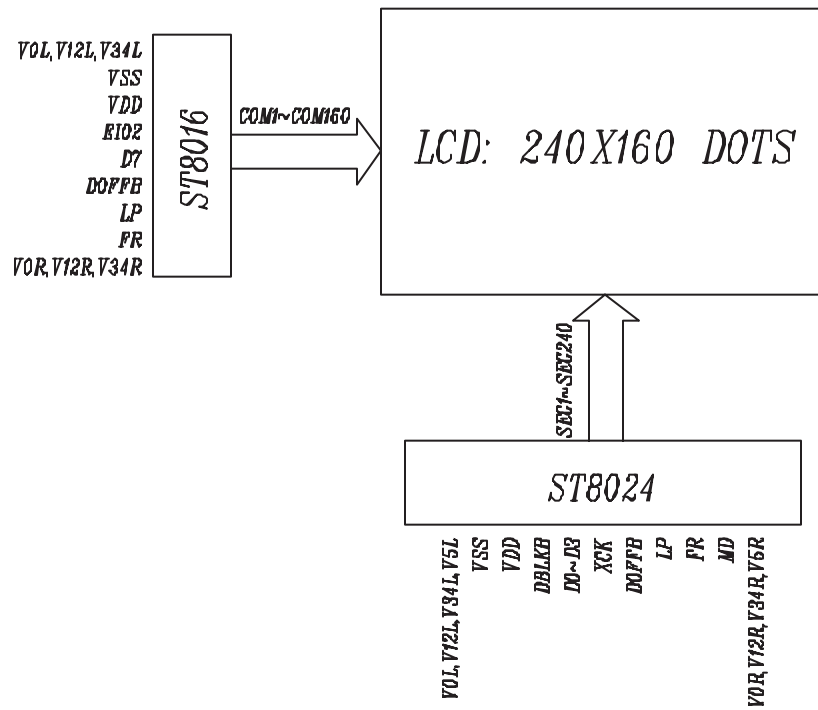
Pin No.	Symbol	Function Description
1	V0L	Bias power supply pins for LCD drive voltage Normally use the bias voltages set by a resistor divider Ensure that voltages are set such that $V_{SS} \cdot V_5 < V_{43} < V_{12} < V_0$. V_{iL} and V_{iR} ($i = 0, 12, 43, 5$) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin
2	V12L	
3	V34L	
4	V5L	
5	VSS	Ground
6	VSS	
7	VDD	Logic power supply
8	VDD	
9	DBLKB	Use as contrast control, use PWM signal as input. Connect to V_{DD} for no contrast control.
10	D0	Data bus
11	D1	
12	D2	
13	D3	
14	XCK	Clock input pin for taking display data * Data is read at the falling edge of the clock pulse.
15	DOFFB	Control input pin for output of non-select level The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. When set to V_{SS} level "L", the LCD drive output pins (Y_1 - Y_{240}) are set to level V_{SS} . When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of DISPOFF. When the DISPOFF function is canceled, the driver outputs non-select level (V_{12} or V_{43}), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if DISPOFF removal time does not correspond to what is shown in AC characteristics, it can not output the reading data correctly. Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
16	LP	Latch pulse input pin for display data Data is latched at the falling edge of the clock pulse.
17	FR	AC signal input pin for LCD drive waveform The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. Normally it inputs a frame inversion signal. The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
18	MD	Mode selection pin When set to V_{SS} level "L", 8-bit parallel input mode is set. When set to V_{DD} level "H", 4-bit parallel input mode is set. Refer to "RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS" in Functional Operations.
19	V5R	Bias power supply pins for LCD drive voltage

20	V34R	Normally use the bias voltages set by a resistor divider Ensure that voltages are set such that $V_{SS} < V_5 < V_{43} < V_{12} < V_0$. V_{iL} and V_{iR} ($i = 0, 12, 43, 5$) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin
21	V12R	
22	V0R	

Common Pin

Pin No.	Symbol	Function Description
23	V0L	Bias power supply pins for LCD drive voltage Normally use the bias voltages set by a resistor divider. Ensure that voltages are set such that $V_{SS} < V_{43} < V_{12} < V_0$. V_{iL} and V_{iR} ($i = 0, 12, 43$) must connect to an external power supply, and supply regular voltage that is assigned by specification for each power pin.
24	V12L	
25	V34L	
26	VSS	Ground
27	VSS	
28	VSS	
29	VDD	Logic power supply
30	VDD	
31	VDD	
32	EIO2	Shift data input for shift register at common mode
33	D7	Dual mode data input at common mode
34	DOFFB	Control input pin for output of non-select level The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. When set to V_{SS} level "L", the LCD drive output pins (Y_1 - Y_{160}) are set to level V_{SS} . When set to "L _i ±", the contents of the shift register are reset to not reading data. When the /DISPOFF function is canceled, the driver outputs non-select level (V_{12} or V_{43}), and the shift data is read at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly. Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
35	LP	Shift clock pulse input pin for bi-directional shift register * Data is shifted at the falling edge of the clock pulse.
36	FR	AC signal input pin for LCD drive waveform The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. Normally it inputs a frame inversion signal. The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal. Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
37	V34R	Bias power supply pins for LCD drive voltage Normally use the bias voltages set by a resistor divider. Ensure that voltages are set such that $V_{SS} < V_{43} < V_{12} < V_0$. V_{iL} and V_{iR} ($i = 0, 12, 43$) must connect to an external power supply, and supply regular voltage that is assigned by specification for each power pin.
38	V12R	
39	V0R	

3.2 Block Diagram



4. Electrical-optical Specifications

4.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	-0.3 to +7.0	V	1,2
Supply voltage (2)	V_o	V_{OL}, V_{OR}	-0.3 to +45.0	V	
	V_{12}	V_{12L}, V_{12R}	-0.3 to $V_o + 0.3$	V	
	V_{43}	V_{43L}, V_{43R}	-0.3 to $V_o + 0.3$	V	
	V_5	V_{SL}, V_{SR}	-0.3 to $V_o + 0.3$	V	
Input voltage	V_i	D17-DI0, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, DISPOFF, TEST1	-0.3 to $V_{DD} + 0.3$	V	
Storage temperature	T_{STG}		-45 to +125	°C	

NOTES:

1. TA = +25 °C
2. The maximum applicable voltage on any pin with respect to Vss (0 V).

4.2 Electrical-Optical Characteristics

No	Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
1	Current (all SEG on)	I	Ta=25°C	-	15.0	30.0	• A	
2	Contrast Ratio	Cr	Ta=25°C $V_{LCD} = 19.5V$	4.5	5.0	-	-	
3	Threshold voltage	Vth	Ta=25°C	1.85	1.90	-	V	
4	Saturation voltage	Vsat	Ta=25°C	-	2.05	2.10	V	
5	Response time	Rise time	Tr	Ta=25°C	-	250	350	ms
		Fall time	Tf	Ta=25°C	-	200	300	ms
		On time	T _{ON}	Ta=25°C	-	300	450	ms
6		Off time	T _{OFF}	Ta=25°C	-	250	350	ms
7	Viewing Angle	6H	• 4	Cr = 2 Ta=25°C	45	-	-	Deg.
8		12H	• 2		25	-	-	Deg.
9		3H	• 3		45	-	-	Deg.
10		9H	• 4		45	-	-	Deg.
11	Frame frequency	f _M	Ta=25°C	32	64	128	Hz	

4.3 Electrical Characteristics

No	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Supply Voltage for Logic	$V_{DD}-V_{SS}$	-	2.5	-	5.5	V
2	Supply Voltage for LCD Driver	$V_{DD}-V_o$ (V_{LCD})	Ta=25 °C	19.3	19.5	19.7	V
3	Supply Current for Logic	I _{DD}	Ta=25 °C $V_{DD}=5.0V$	-	23	26	mA
4	Frame Frequency	f _M	Ta=25°C	-	80	-	Hz

5	Input High Voltage	V_{IH}	-	$0.8XV_{DD}$	-	V_{DD}	V
6	Input Low Voltage	V_{IL}	-	GND	-	$0.2XV_{DD}$	V
7	Output High Voltage	V_{OH}	-	$V_{DD}-0.4$	-	-	V
8	Output Low Voltage	V_{OL}	-	-	-	+0.4	V

4.3 Timing Characteristics

- Segment

(Segment Mode 1) ($V_{SS} = V_S = 0\text{ V}$, $V_{DD} = +5.0\pm 0.5\text{ V}$, $V_0 = +15.0\text{ to }+42.0\text{ V}$, $T_{OPR} = -25\text{ to }+85\text{ }^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	$t_r, t_f \leq 10\text{ns}$	50			ns	1
Shift clock "H" pulse width	t_{WCKH}		15			ns	
Shift clock "L" pulse width	t_{WCKL}		15			ns	
Data setup time	t_{DS}		10			ns	
Data hold time	t_{DH}		12			ns	
Latch pulse "H" pulse width	t_{WLPH}		15			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		30			ns	
Latch pulse rise to shift clock rise time	t_{LS}		25			ns	
Latch pulse fall to shift clock fall time	t_{LH}		25			ns	
Enable setup time	t_S		10			ns	
Input signal rise time	t_r				50	ns	2
Input signal fall time	t_f				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			μs	
Output delay time (1)	t_D	$CL = 15\text{ pF}$			30	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	$CL = 15\text{ pF}$			1.2	μs	
Output delay time (3)	t_{PD3}	$CL = 15\text{ pF}$			1.2	μs	

NOTES:

1. Takes the cascade connection into consideration.
2. $(t_{WCK} - t_{WCKH} - t_{WCKL})/2$ is maximum in the case of high speed operation.

(Segment Mode 2) ($V_{SS} = V_S = 0\text{ V}$, $V_{DD} = +3.0\text{ to }+4.5\text{ V}$, $V_0 = +15.0\text{ to }+42.0\text{ V}$, $T_{OPR} = -25\text{ to }+85\text{ }^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	$t_r, t_f \leq 10\text{ns}$	66			ns	1
Shift clock "H" pulse width	t_{WCKH}		23			ns	
Shift clock "L" pulse width	t_{WCKL}		23			ns	
Data setup time	t_{DS}		15			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		50			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_r				50	ns	2
Input signal fall time	t_f				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			μs	
Output delay time (1)	t_D	$CL = 15\text{ pF}$			41	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	$CL = 15\text{ pF}$			1.2	μs	
Output delay time (3)	t_{PD3}	$CL = 15\text{ pF}$			1.2	μs	

NOTES:

1. Takes the cascade connection into consideration.
2. $(t_{WCK} - t_{WCKH} - t_{WCKL})/2$ is maximum in the case of high speed operation.

5	Input High Voltage	V_{IH}	-	$0.8XV_{DD}$	-	V_{DD}	V
6	Input Low Voltage	V_{IL}	-	GND	-	$0.2XV_{DD}$	V
7	Output High Voltage	V_{OH}	-	$V_{DD}-0.4$	-	-	V
8	Output Low Voltage	V_{OL}	-	-	-	+0.4	V

4.3 Timming Characteristics

- Segment

(Segment Mode 1) ($V_{SS} = V_S = 0\text{ V}$, $V_{DD} = +5.0\pm 0.5\text{ V}$, $V_0 = +15.0\text{ to }+42.0\text{ V}$, $T_{OPR} = -25\text{ to }+85\text{ }^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	$t_r, t_f \leq 10\text{ns}$	50			ns	1
Shift clock "H" pulse width	t_{WCKH}		15			ns	
Shift clock "L" pulse width	t_{WCKL}		15			ns	
Data setup time	t_{DS}		10			ns	
Data hold time	t_{DH}		12			ns	
Latch pulse "H" pulse width	t_{WLPH}		15			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		30			ns	
Latch pulse rise to shift clock rise time	t_{LS}		25			ns	
Latch pulse fall to shift clock fall time	t_{LH}		25			ns	
Enable setup time	t_S		10			ns	
Input signal rise time	t_r				50	ns	2
Input signal fall time	t_f				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			μs	
Output delay time (1)	t_D	$CL = 15\text{ pF}$			30	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	$CL = 15\text{ pF}$			1.2	μs	
Output delay time (3)	t_{PD3}	$CL = 15\text{ pF}$			1.2	μs	

NOTES:

1. Takes the cascade connection into consideration.
2. $(t_{WCK} - t_{WCKH} - t_{WCKL})/2$ is maximum in the case of high speed operation.

(Segment Mode 2) ($V_{SS} = V_S = 0\text{ V}$, $V_{DD} = +3.0\text{ to }+4.5\text{ V}$, $V_0 = +15.0\text{ to }+42.0\text{ V}$, $T_{OPR} = -25\text{ to }+85\text{ }^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	$t_r, t_f \leq 10\text{ns}$	66			ns	1
Shift clock "H" pulse width	t_{WCKH}		23			ns	
Shift clock "L" pulse width	t_{WCKL}		23			ns	
Data setup time	t_{DS}		15			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		50			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_r				50	ns	2
Input signal fall time	t_f				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			μs	
Output delay time (1)	t_D	$CL = 15\text{ pF}$			41	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	$CL = 15\text{ pF}$			1.2	μs	
Output delay time (3)	t_{PD3}	$CL = 15\text{ pF}$			1.2	μs	

NOTES:

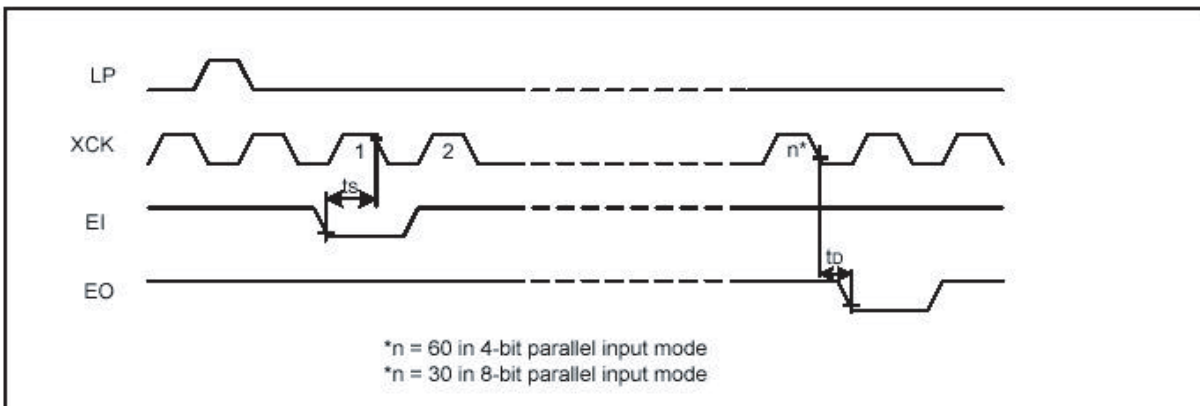
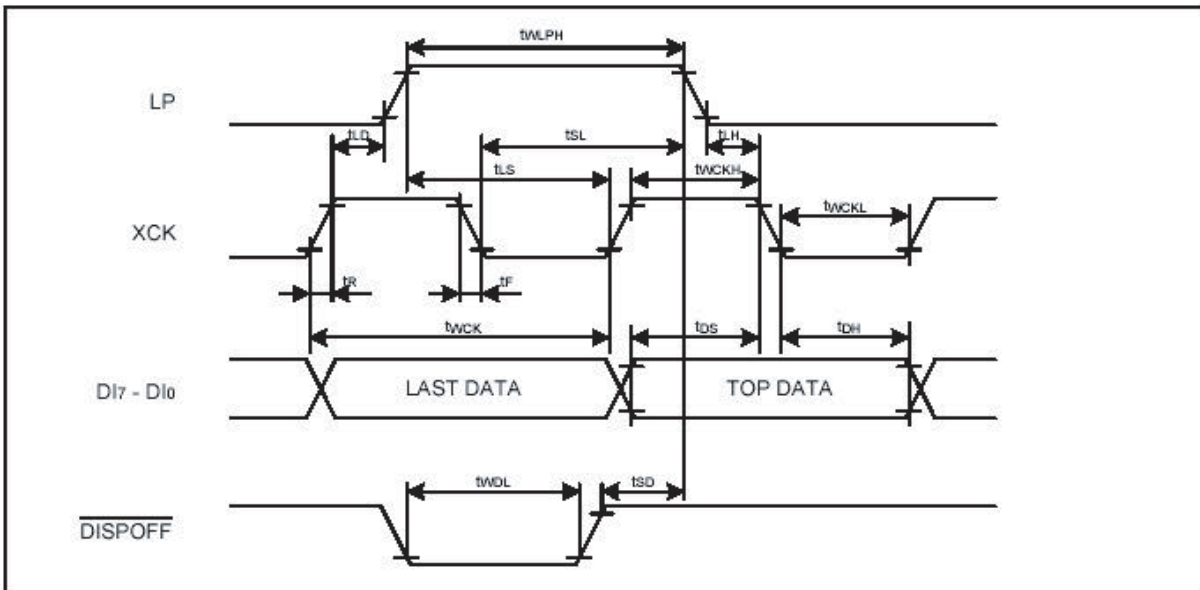
1. Takes the cascade connection into consideration.
2. $(t_{WCK} - t_{WCKH} - t_{WCKL})/2$ is maximum in the case of high speed operation.

(Segment Mode 3) ($V_{SS} = V_S = 0\text{ V}$, $V_{DD} = +2.5\text{ to }+3.0\text{ V}$, $V_0 = +15.0\text{ to }+42.0\text{ V}$, $T_{OPR} = -25\text{ to }+85\text{ }^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{wck}	$t_r, t_f \leq 10\text{ns}$	82			ns	1
Shift clock "H" pulse width	t_{wckH}		28			ns	
Shift clock "L" pulse width	t_{wckL}		28			ns	
Data setup time	t_{ds}		20			ns	
Data hold time	t_{dh}		23			ns	
Latch pulse "H" pulse width	t_{wLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		65			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_s		15			ns	
Input signal rise time	t_r				50	ns	2
Input signal fall time	t_f				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			μs	
Output delay time (1)	t_o	$CL = 15\text{ pF}$			57	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	$CL = 15\text{ pF}$			1.2	μs	
Output delay time (3)	t_{PD3}	$CL = 15\text{ pF}$			1.2	μs	

NOTES:

1. Takes the cascade connection into consideration.
2. $(t_{wck} - t_{wckH} - t_{wckL})/2$ is maximum in the case of high speed operation.



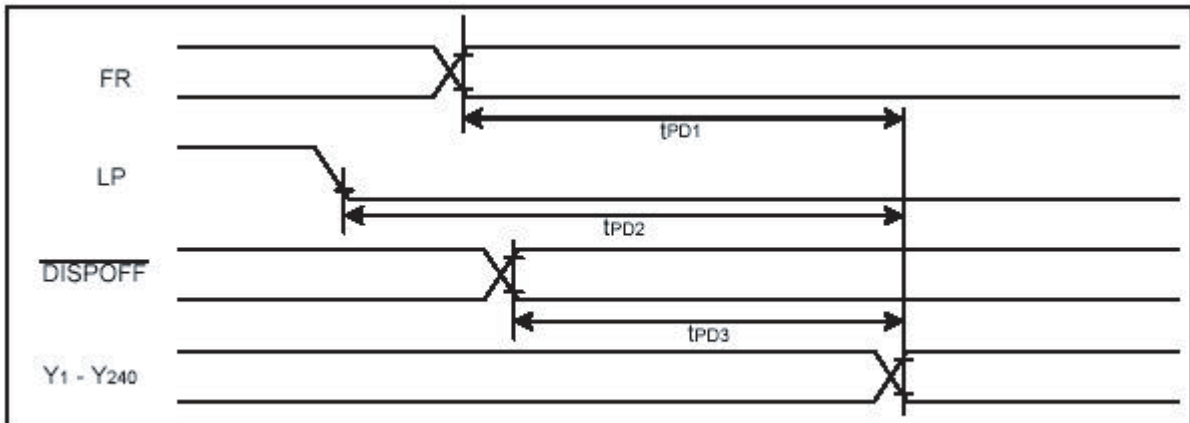


Fig. 8 Timing Characteristics (3)

- Common

(Common Mode) ($V_{SS} = 0\text{ V}$, $V_{DD} = +2.5\text{ to }+5.5\text{ V}$, $V_0 = +15.0\text{ to }+30.0\text{ V}$, $T_{OPR} = -25\text{ to }+85^\circ\text{ C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shift clock period	t_{WLP}	$t_r, t_f \leq 20\text{ ns}$	250			ns
Shift clock "H" pulse width	t_{WLPH}	$V_{DD} = +5.0 \pm 0.5\text{ V}$	15			ns
		$V_{DD} = +2.5\text{ to }4.5\text{ V}$	30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
DISPOFF removal time	t_{SD}		100			ns
DISPOFF "L" pulse width	t_{WDL}		1.2			μs
Output delay time (1)	t_{DL}	$CL = 15\text{ pF}$			200	ns
Output delay time (2)	t_{PD1}, t_{PD2}	$CL = 15\text{ pF}$			1.2	μs
Output delay time (3)	t_{PD3}	$CL = 15\text{ pF}$			1.2	μs

