DMOS Microstepping Driver with Translator

Features and Benefits

- Low $R_{DS(on)}$ outputs
- Short-to-ground protection
- Shorted load protection
- Automatic current decay mode detection/selection
- Mixed and slow current decay modes
- Synchronous rectification for low power dissipation
- Internal UVLO and thermal shutdown circuitry
- Crossover-current protection

Package: 24 pin TSSOP with exposed thermal pad (suffix LP)

Approximate scale

Description

The A3987 is a complete microstepping motor driver with built-in translator for easy operation. It is designed to operate bipolar stepper motors in full, half, quarter, and sixteenth step modes, with output drive capability of 50 V and ±1.5 A. The A3987 includes a fixed off-time current regulator, which has the ability to operate in slow or mixed decay modes.

The translator is the key to the easy implementation of the A3987. Simply inputting one pulse on the step input drives the motor to take one microstep. There are no phase sequence tables, high frequency control lines, or complex interfaces to program. The A3987 interface is an ideal fit for applications where a complex microprocessor is unavailable or over-burdened.

The A3987 chopping control automatically selects the current decay mode (slow or mixed). When a STEP signal occurs, the translator determines if that step results in a higher or lower current in each of the motor phases. If the change is to a higher current, then the decay mode is set to slow decay. If the change is to a lower current, then the decay mode is set to 30.1% fast decay. This current decay control scheme results in reduced audible motor noise, increased step accuracy, and reduced power dissipation.

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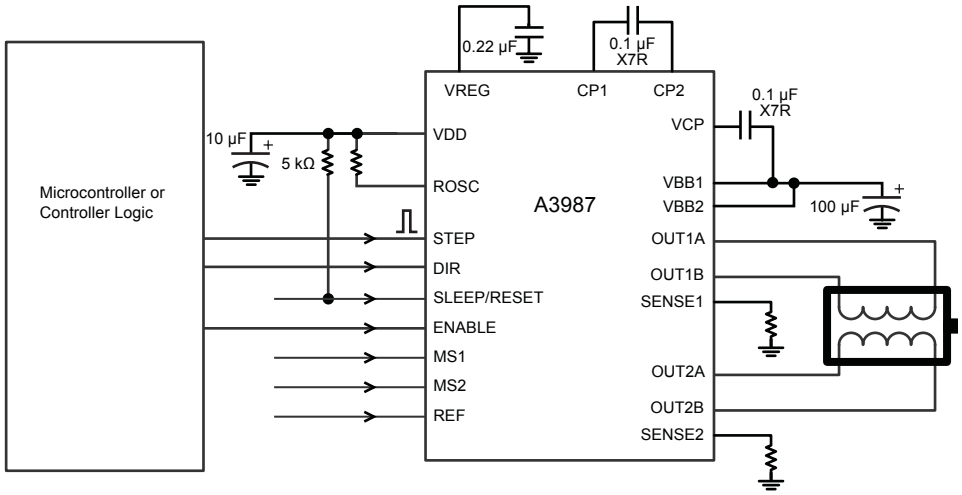
Typical Application Diagram



Description (continued)

Internal synchronous rectification control circuitry is provided to improve power dissipation during PWM operation.

Internal circuit protection includes: thermal shutdown with hysteresis, undervoltage lockout (UVLO), and crossover current protection. Special power-up sequencing is not required.

The A3987 is supplied in a thin profile (1.2 mm maximum height) 24-lead TSSOP (suffix LP) with exposed thermal tab. The package is lead (Pb) free with 100% matte tin leadframe plating.

Selection Guide

Part Number	Package	Packing
A3987SLP-T	24-pin TSSOP with exposed thermal pad	62 pieces / tube
A3987SLPTR-T	24-pin TSSOP with exposed thermal pad	3000 pieces / reel

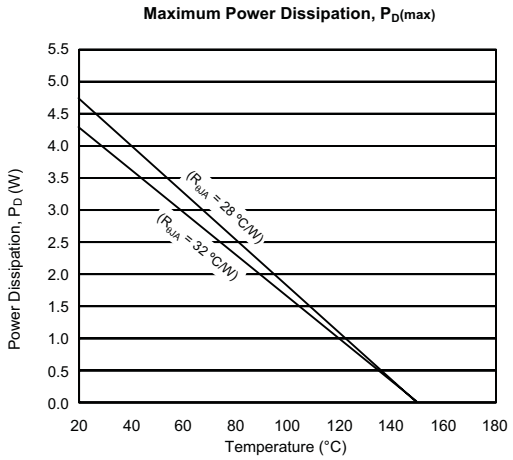
Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		50	V
Output Current	I_{OUT}	Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.	±1.5	A
Logic Supply Voltage	V_{DD}		7.0	V
Logic Input Voltage Range	V_{IN}		–0.3 to V_{DD} + 0.3	V
VBBx to OUTx			50	V
Sense Voltage	V_{SENSE}		0.5	V
Reference Voltage	V_{REF}		0 to 4	V
Nominal Operating Temperature	T_A	Range S	–20 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

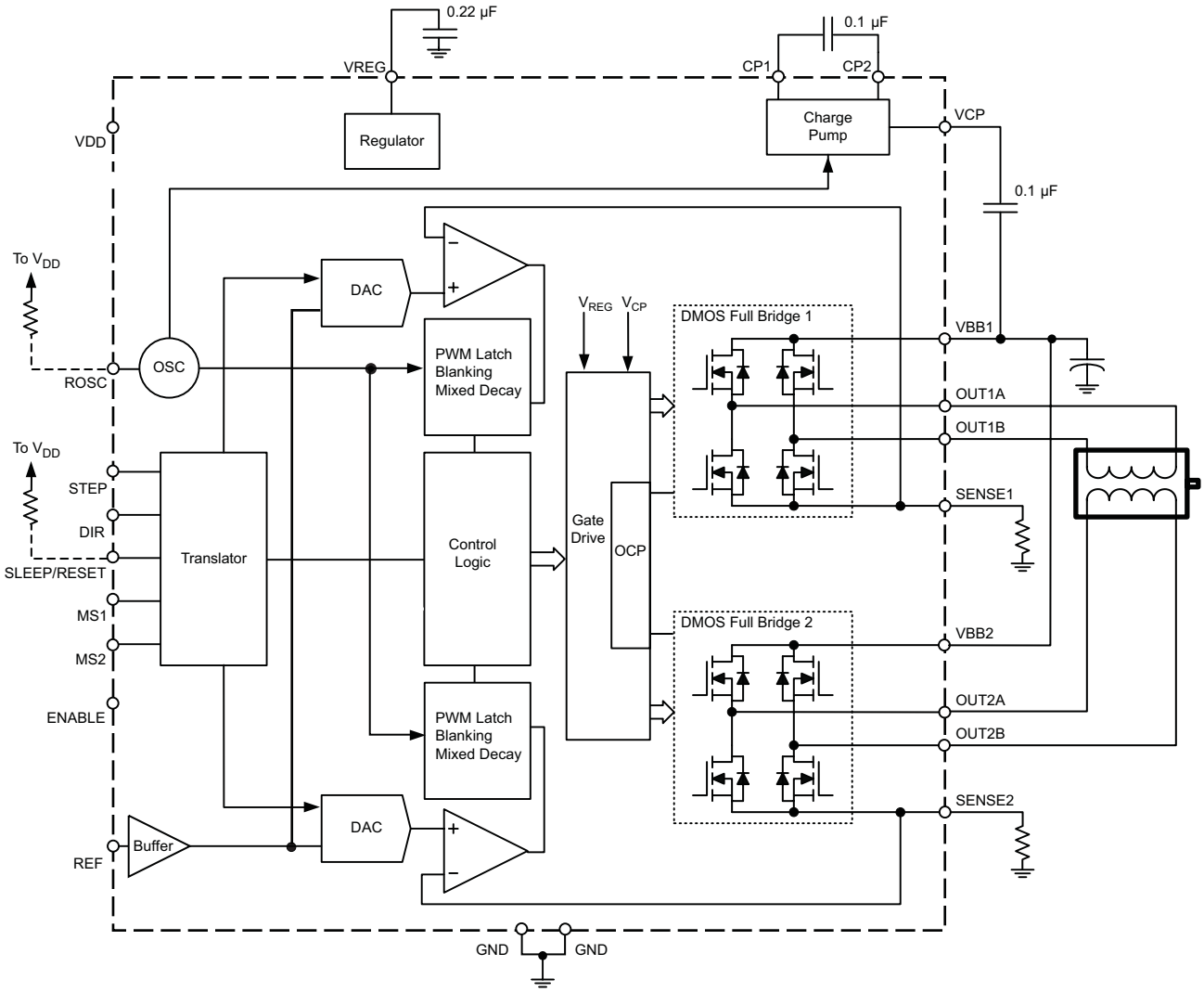
Thermal Characteristics*

Characteristic	Symbol	Notes	Rating	Units
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	28	°C/W
		2-layer PCB with 3.8 in.^{2} 2 oz. copper each side	32	°C/W

*Additional thermal data available on the Allegro website.



Functional Block Diagram



ELECTRICAL CHARACTERISTICS[1] valid at T_A = 25°C, V_{BB} = 50 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Units
Output Drivers						
Load Supply Voltage Range	V_{BB}	Operating	8	–	50	V
		During sleep mode	0	–	50	V
Logic Supply Voltage Range	V_{DD}	Operating	3.0	–	5.5	V
Output On Resistance	$R_{DS(on)}$	Source driver, I_{OUT} = –1.5 A	–	0.54	0.6	Ω
		Sink driver, I_{OUT} = 1.5 A	–	0.54	0.6	Ω
Body Diode Forward Voltage	V_F	Source diode, I_F = –1.5 A	–	–	1.2	V
		Sink diode, I_F = 1.5 A	–	–	1.2	V
Motor Supply Current	I_{BB}	f_{PWM} < 50 kHz	–	–	4	mA
		Operating, outputs disabled	–	–	2	mA
		Sleep (idle) mode	–	–	20	µA
Logic Supply Current	I_{DD}	f_{PWM} < 50 kHz	–	–	12	mA
		Outputs off	–	–	10	mA
		Sleep mode	–	–	100	µA
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		V_{DD} × 0.7	–	–	V
	$V_{IN(0)}$		–	–	V_{DD} × 0.3	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = V_{DD} × 0.7	–20	<1.0	20	µA
	$I_{IN(0)}$	V_{IN} = V_{DD} × 0.3	–20	<1.0	20	µA
Input Hysteresis			150	–	600	mV
Blank Time	t_{BLANK}	f_{osc} = 4 MHz	0.7	1	1.3	ms
Fixed Offtime	t_{OFF}	ROSC tied to ground	15	25	35	ms
		R_{OSC} = 59 KΩ	23	30	37	ms
Reference Input Voltage Range			0.8	–	4	V
Reference Input Current	I_{REF}		–3	0	3	mA
GM Error[3]	Err	V_{REF} = 4 V, DAC = 37.5%	–	–	±15	%
		V_{REF} = 4 V, DAC = 70.31%	–	–	±10	%
		V_{REF} = 4 V, DAC = 100%	–	–	±5	%
Crossover Dead Time	t_{DT}		300	650	900	ns
Reset Pulse Width	t_{RP}		0.2	–	1	µs
Sleep Pulse Width	t_S		>2.5	–	–	µs
UVLO Enable Threshold	V_{UVLO}	V_{DD} rising	2.35	2.7	3	V
UVLO Hysteresis	V_{UVHYS}		0.05	0.10	–	V

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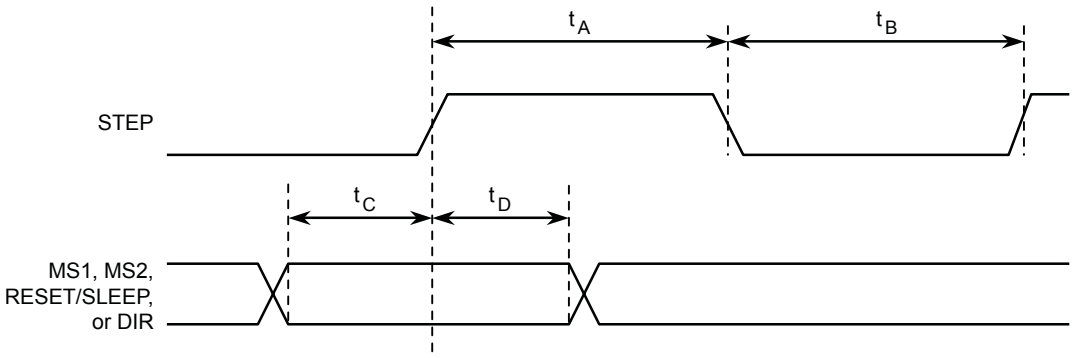
ELECTRICAL CHARACTERISTICS[1] (continued) valid at T_A = 25°C, V_{BB} = 50 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Units
Protection Circuitry						
Overcurrent Protection Threshold[4]	I_{ocpst}		2	–	–	A
Overcurrent Blanking	t_{ocp}		1		3	µs
Thermal Shutdown Temperature	T_{TSD}		–	165	–	°C
Thermal Shutdown Hysteresis	T_{TSDhys}		–	15	–	°C

[1]Negative current is defined as coming out of (sourcing) the specified device pin.
[2]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.
[3]$V_{ERR} = [(V_{REF}/8) – V_{SENSE}]/(V_{REF}/8)$.
[4]OCP is tested at T_A = 25°C in a restricted range and guaranteed by characterization.



Time Duration	Symbol	Typ.	Unit
STEP minimum, HIGH pulse width	t_A	1	µs
STEP minimum, LOW pulse width	t_B	1	µs
Setup time, input change to STEP	t_C	200	ns
Hold time, input change to STEP	t_D	200	ns

Figure 1. Logic Interface Timing Diagram

Table 1. Microstep Resolution Truth Table

MS1	MS2	Microstep Resolution	Excitation Mode
L	L	Full step	2 phase
H	L	Half step	1-2 phase
L	H	Quarter step	W1-2 phase
H	H	Sixteenth step	4W1-2 phase

Table 2. Step Sequencing Settings

Home microstep position at Step Angle 45°; DIR = H

Full Step (#)	Half Step (#)	1/4 Step (#)	1/16 Step (#)	Phase 1 Current (% of I_{TRIP}(max))	Phase 2 Current (% of I_{TRIP}(max))	Step Angle (°)	Full Step (#)	Half Step (#)	1/4 Step (#)	1/16 Step (#)	Phase 1 Current (% of I_{TRIP}(max))	Phase 2 Current (% of I_{TRIP}(max))	Step Angle (°)
	1	1	1	0.00	100.00	0.0		5	9	33	0.00	–100.00	180.0
			2	9.38	100.00	5.6				34	–9.38	–100.00	185.6
			3	18.75	98.44	11.3				35	–18.75	–98.44	191.3
			4	29.69	95.31	16.9				36	–29.69	–95.31	196.9
		2	5	37.50	92.19	22.5			10	37	–37.50	–92.19	202.5
			6	46.88	87.50	28.1				38	–46.88	–87.50	208.1
			7	56.25	82.81	33.8				39	–56.25	–82.81	213.8
			8	64.06	76.56	39.4				40	–64.06	–76.56	219.4
1	2	3	9	70.31	70.31	45.0	3	6	11	41	–70.31	–70.31	225.0
			10	76.56	64.06	50.6				42	–76.56	–64.06	230.6
			11	82.81	56.25	56.3				43	–82.81	–56.25	236.3
			12	87.50	46.88	61.9				44	–87.50	–46.88	241.9
		4	13	92.19	37.50	67.5			12	45	–92.19	–37.50	247.5
			14	95.31	29.69	73.1				46	–95.31	–29.69	253.1
			15	98.44	18.75	78.8				47	–98.44	–18.75	258.8
			16	100.00	9.38	84.4				48	–100.00	–9.38	264.4
	3	5	17	100.00	0.00	90.0		7	13	49	–100.00	0.00	270.0
			18	100.00	–9.38	95.6				50	–100.00	9.38	275.6
			19	98.44	–18.75	101.3				51	–98.44	18.75	281.3
			20	95.31	–29.69	106.9				52	–95.31	29.69	286.9
		6	21	92.19	–37.50	112.5			14	53	–92.19	37.50	292.5
			22	87.50	–46.88	118.1				54	–87.50	46.88	298.1
			23	82.81	–56.25	123.8				55	–82.81	56.25	303.8
			24	76.56	–64.06	129.4				56	–76.56	64.06	309.4
2	4	7	25	70.31	–70.31	135.0	4	8	15	57	–70.31	70.31	315.0
			26	64.06	–76.56	140.6				58	–64.06	76.56	320.6
			27	56.25	–82.81	146.3				59	–56.25	82.81	326.3
			28	46.88	–87.50	151.9				60	–46.88	87.50	331.9
		8	29	37.50	–92.19	157.5			16	61	–37.50	92.19	337.5
			30	29.69	–95.31	163.1				62	–29.69	95.31	343.1
			31	18.75	–98.44	168.8				63	–18.75	98.44	348.8
			32	9.38	–100.00	174.4				64	–9.38	100.00	354.4
	5	9	33	0.00	–100.00	180.0		1	1	1	0.00	100.00	360.0

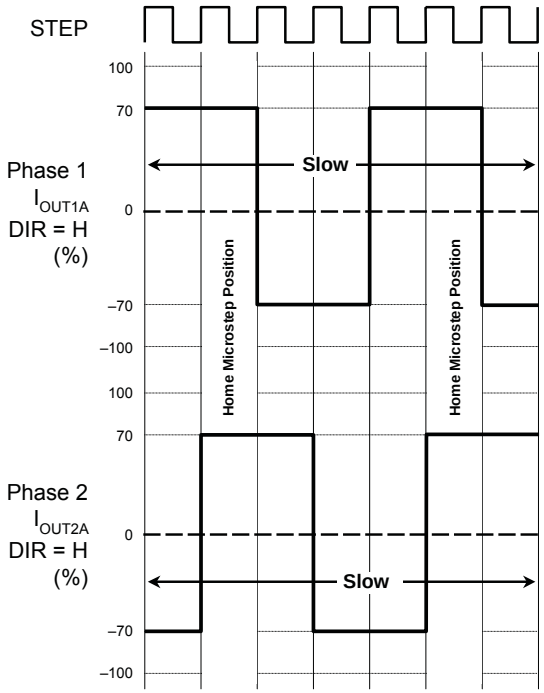


Figure 2. Decay Mode for Full-Step Increments

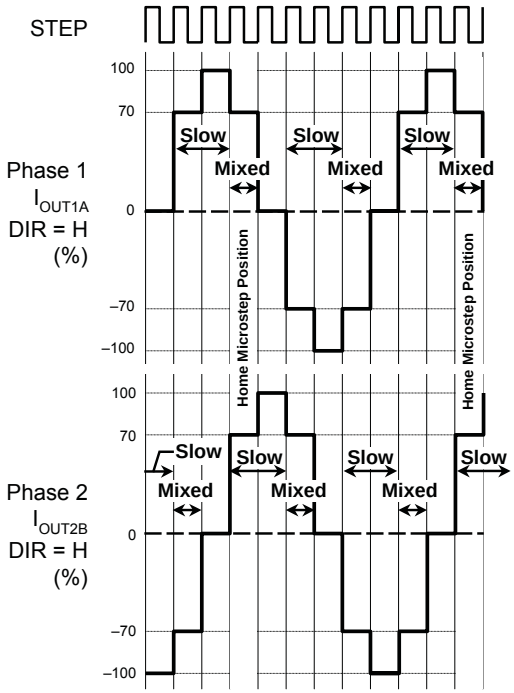


Figure 3. Decay Modes for Half-Step Increments

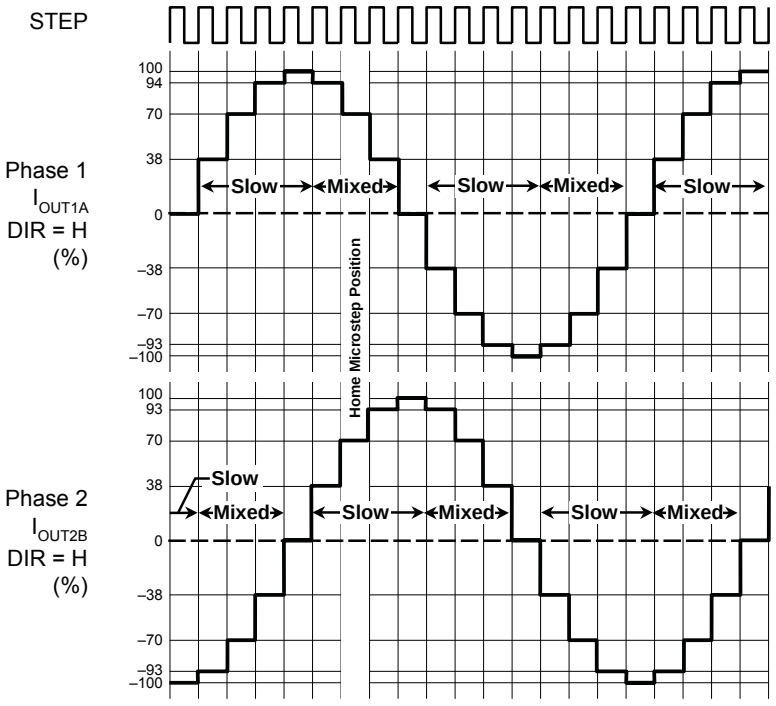


Figure 4. Decay Modes for Quarter-Step Increments

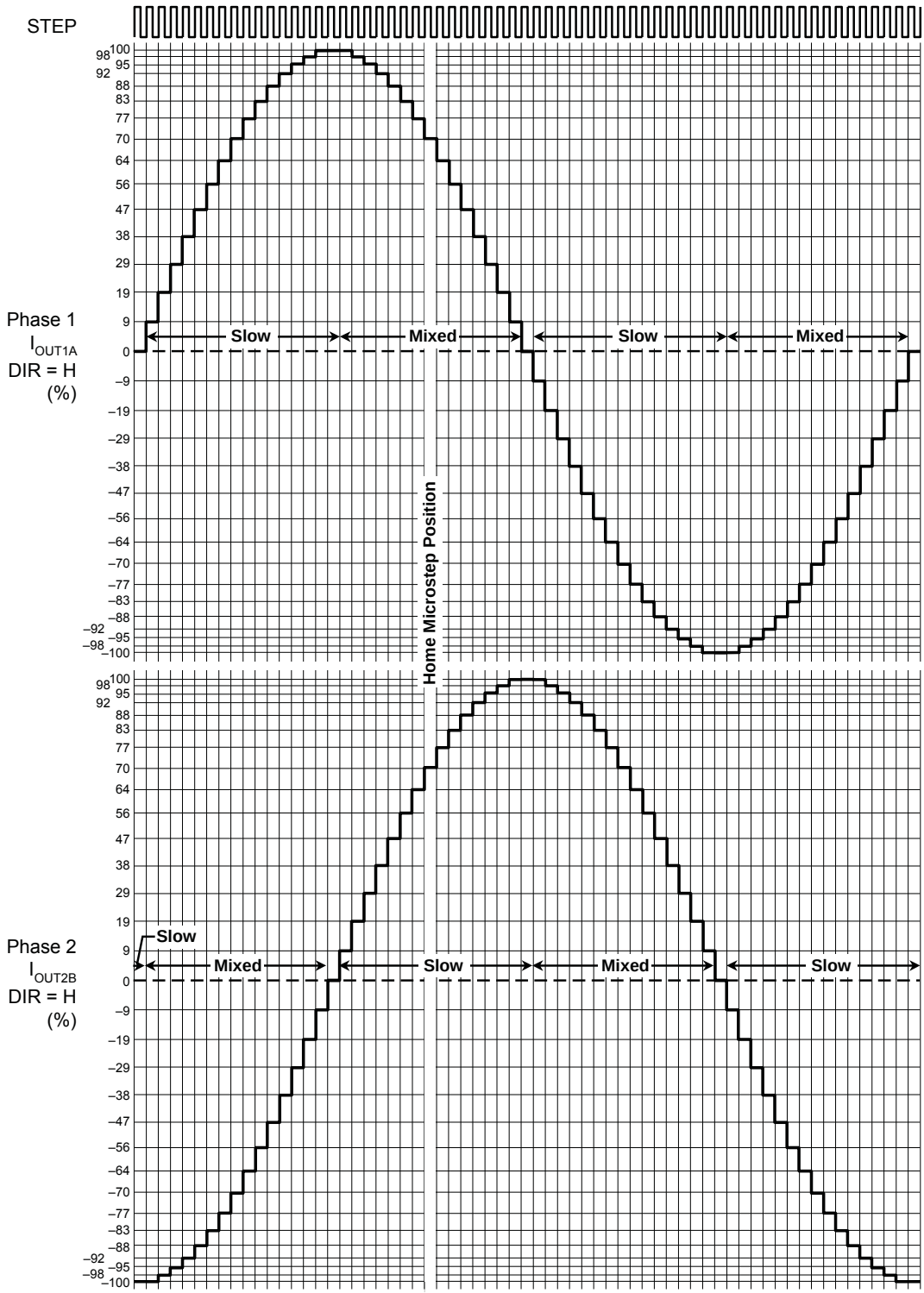


Figure 5. Decay Modes for Sixteenth-Step Increments

Functional Description

Device Operation The A3987 is a complete microstepping motor driver with built-in translator for easy operation with a minimum of control lines. The A3987 is designed to operate bipolar stepper motors in full, half, quarter, and sixteenth step modes. The full bridges on the dual outputs are composed entirely of N-channel DMOS FETS, and the full bridge currents are regulated by fixed off-time, pulse width modulated (PWM) control circuitry. For each full bridge, the individual step currents are set by the combination of: a common external reference voltage, V_{REF}; an external current sense resistor, R_{SENSEx}; and the output voltage of an internal DAC that is controlled by the output of the translator.

At power-up or reset, the translator sets the DACs and phase current polarity to the initial home state (see figures 2 through 5 for home state conditions), and also sets the current regulator for both output phases to mixed decay mode. When a command signal occurs on the STEP input, the translator automatically sequences the DACs to the next level (see table 2 for the current level sequence) and current polarity. The microstep resolution is set by inputs MS1 and MS2 (see in table 1 for state settings). If logic inputs are pulled up to VDD, it is good practice to use a high value pull-up resistor in order to limit current to the logic inputs should an overvoltage event occur. If the new DAC output level is lower than the previous level, then the decay mode for that full bridge will be set to mixed decay. If the new DAC level is higher or equal to the previous level, then the decay mode for that full bridge will be slow decay. This automatic current decay selection improves microstepping performance by reducing the distortion of the current waveform due to the motor BEMF.

Low-Power Mode Select (SLEEP/RESET) An active-low control input used to minimize power consumption when the A3987 is not in use. This disables much of the internal circuitry including the output FETs and internal regulator. A logic high allows normal device operation and power-up in the home state. When coming out of sleep mode, a 1 ms delay is required before issuing a STEP command, to allow the internal regulator to stabilize. The outputs can also be reset to the home state without entering sleep mode. To do so, pulse this input low for a duration between t_{RP}(min) and t_{RP}(max).

Step Input (STEP) A low-to-high transition on the STEP input sequences the translator and advances the motor one increment. The translator controls the input to the DACs and the direction of current flow in each winding. The size of the increment is determined by the state of inputs MS1 and MS2.

Microstep Select (MS1 and MS2) Inputs MS1 and MS2 select the microstepping format (see table 1 for state settings). Changes to these inputs do not take effect until the next STEP command. It is good practice to use a pull-up resistor to VDD in order to limit input current should an external overvoltage occur. A minimum of 5 kΩ is recommended.

Direction Input (DIR) The state of the DIR input determines the direction of rotation of the motor. A logic change on the DIR pin will not take effect until the next STEP command is issued.

Internal PWM Current Control Each full bridge is controlled by a fixed off-time PWM current control circuit that limits the load current to a desired value (I_{TRIP}). Initially, a diagonal pair of source and sink FETs are enabled and current flows through the motor winding and the corresponding current sense resistor, R_{SENSEx}. When the voltage across R_{SENSE} equals the DAC output voltage, the current sense comparator resets the PWM latch, which turns off the source drivers (in slow decay mode) or the sink and source drivers (in fast or mixed decay modes).

The maximum value of current limiting is set by the selection of R_{SENSE} and the voltage at the REF input, with a transconductance function approximated by:

$$I_{TRIP}(max) = V_{REF} / 8 \times R_{SENSE} \ .$$

The DAC output reduces the V_{REF} output to the current sense comparator in precise steps:

$$I_{TRIP} = (\%\ I_{TRIP}(max) / 100) \times I_{TRIP}(max) \ ,$$

(see table 2 for % I_{TRIP}(max) at each step).

Note: It is critical that the absolute maximum voltage rating (0.5 V) on the SENSE pins is not exceeded.

Fixed Off-Time The internal PWM current control circuitry uses a 4 MHz master oscillator to control the duration of time that the drivers remain off. The fixed off-time, t_{OFF}, is determined by the selection of an external resistor connected from the ROSC timing terminal to VDD. If the ROSC terminal is tied directly to GND, t_{OFF} defaults to 25 µs. The off-time is approximated by:

$$t_{OFF} \approx R_{OSC} / 1.981 \times 10^9$$

The master oscillator period is used to derive PWM off-time, dead time, and blanking time.

Blanking This function blanks the output of the current sense comparator when the outputs are switched by the internal current control circuitry. The comparator output is blanked to prevent false overcurrent detections due to reverse recovery currents of

the internal body diodes, and switching transients related to the capacitance of the load. The blank time, t_{BLANK}, is internally set to approximately 1 µs.

Charge Pump (CP1 and CP2) The charge pump is used to generate a gate supply greater than V_{BBx} to drive the source FET gates. A 0.1 µF ceramic capacitor is required between CP1 and CP2 for pumping purposes. A 0.1µF ceramic capacitor is required between VCP and the VBB terminals to act as a reservoir to operate the high-side FETs.

Internal Regulator (VREG) The VREG terminal should be decoupled with a 0.22 µF capacitor to ground. This internally generated voltage is used to operate the sink FET outputs. VREG is internally monitored, and in the case of a fault condition, the outputs of the device are disabled.

Enable Input (ENABLE) This input activates all of the FET outputs. When logic high, the outputs are disabled, and when logic low, the outputs are enabled. Inputs to the translator (STEP, DIR, MS1, and MS2) are always active, except in Sleep mode, regardless of the ENABLE input state.

Shutdown In the event of a fault (either excessive junction temperature, or low voltage on VCP), the outputs of the device are disabled until the fault condition is removed. At power-up, the undervoltage lockout (UVLO) circuit disables the drivers and resets the translator to the home state.

Mixed Decay Operation The full bridges can operate in mixed decay mode when set by the step sequence (see figures 3 through 5). As the trip point is reached, the device goes into fast decay mode for 30.1% of the fixed off-time, t_{OFF}. After this fast decay portion, t_{FD}, the device switches to slow decay mode for the remainder of the fixed off-time period.

Synchronous Rectification When a PWM off-cycle is triggered by an internal fixed off-time cycle, load current will recirculate according to the decay mode selected by the control logic. The A3987 synchronous rectification feature turns on the appropriate FETs during current decay, effectively shorting out the body diodes in the low $R_{DS(on)}$ driver. This lowers power dissipation significantly, and can eliminate the need for external Schottky diodes for many applications. To prevent reversal of load current, synchronous rectification is turned off when a zero current level is detected.

Short-to-Ground Should a motor winding short to ground, the current through the short will rise until the overcurrent threshold, I_{COPST}, a minimum of 2 A, is exceeded. The driver turns off after a short propagation delay and latches the fault. The device will remain disabled until the SLEEP/RESET input goes high or VDD power is removed. As shown in figure 6, a short-to-ground produces a single overcurrent event.

Shorted Load During a shorted load event, the current path is through the sense resistor. During this fault condition the device will be protected, however, the fault will not be latched. When the full bridge turns on, the current will rise and exceed the overcurrent threshold. After the blank time,t_{BLANK}, of approximatly 1 µs, the driver will look at the voltage on the SENSE*x* pin. The voltage on the SENSE*x* pin will be larger than the voltage set by the REF pin, and the full bridge will turn off for the time set by the ROSC pin. Figure 7 shows a shorted load condition with an off-time of 30 µs.

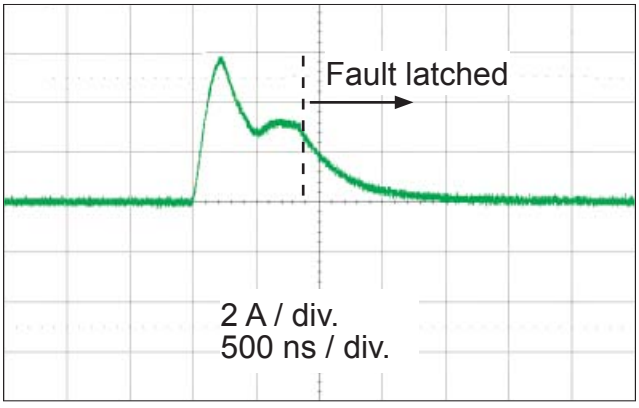


Figure 6. Short-to-ground event

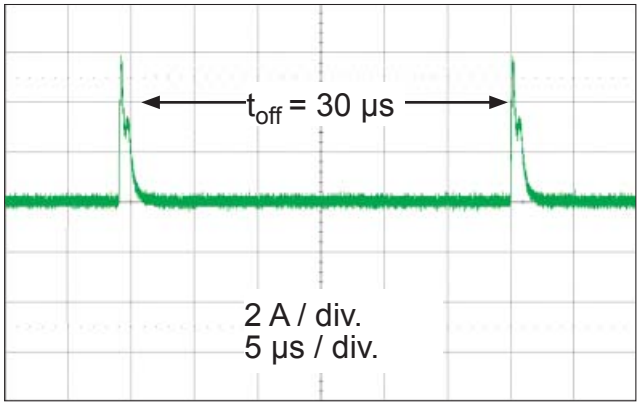


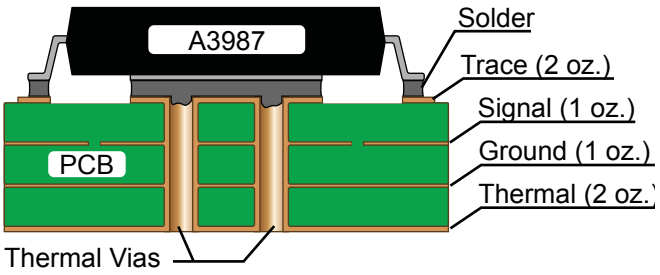
Figure 7. Short-to-load event

Layout. The printed circuit board should use a heavy ground-plane. For optimum electrical and thermal performance, the A3987 must be soldered directly onto the board. On the underside of the A3987 package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.

In order to minimize the effects of ground bounce and offset issues, it is important to have a low impedance single-point ground, known as a *star ground*, located very close to the device. By making the connection between the pad and the ground plane directly under the A3987, that area becomes an ideal location for a star ground point. A low impedance ground will prevent ground bounce during high current operation and ensure that the supply voltage remains stable at the input terminal. The recommended PCB layout, shown in figure 8, illustrates how to create a star ground under the device, to serve both as a low impedance ground point and thermal path.

The two input capacitors should be placed in parallel, and as close to the device supply pins as possible. The ceramic capacitor (CIN1) should be closer to the pins than the bulk capacitor (CIN2). This is necessary because the ceramic capacitor will be responsible for delivering the high frequency current components.

The sense resistors, RSx , should have a very low impedance path to ground, because they must carry a large current while supporting very accurate voltage measurements by the current sense comparators. Long ground traces will cause additional voltage drops, adversely affecting the ability of the comparators to accurately measure the current in the windings. As shown in figure 8, the SENSEx pins have very short traces to the RSx resistors and very thick, low impedance traces directly to the star ground underneath the device. If possible, there should be no other components on the sense circuits.



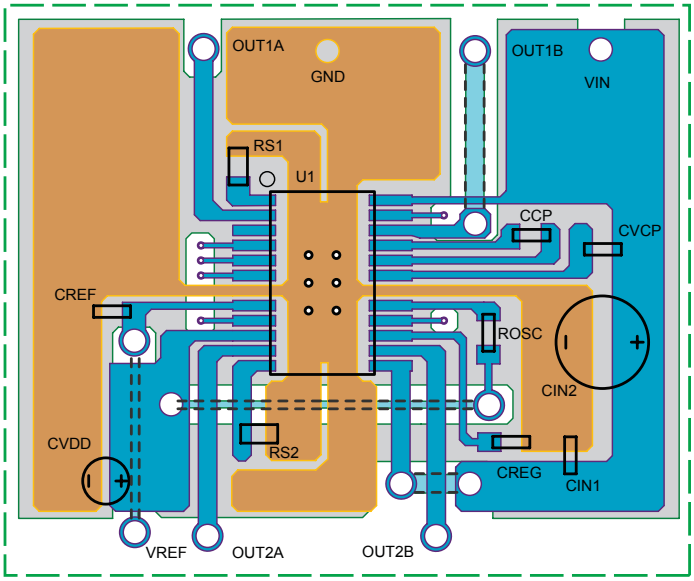
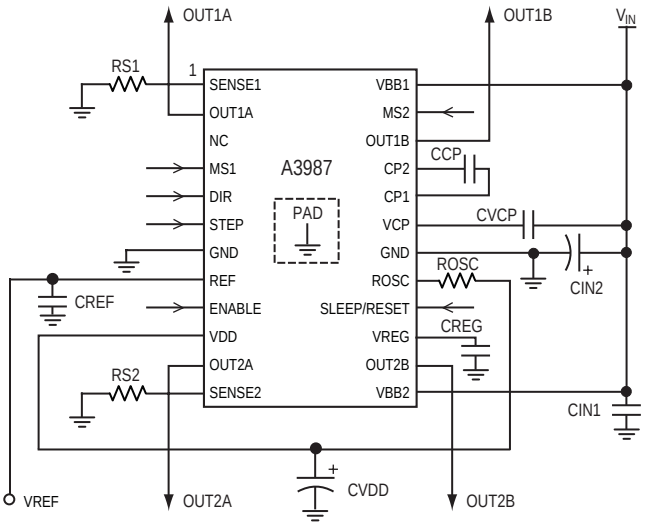
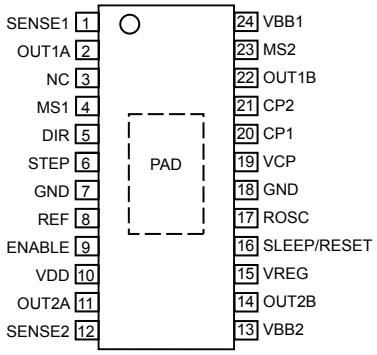


Figure 8. Printed circuit board layout with typical application circuit, shown at right. The copper area directly under the A3987 (U1) is soldered to the exposed thermal pad on the underside of the device.



The thermal vias serve also as electrical vias, connecting it to the ground plane on the other side of the PCB , so the two copper areas together form the star ground.

Device Pin-out Diagrams



Terminal List Table

Number	Name	Pin Description
1	SENSE1	Sense resistor terminal for Full Bridge 1
2	OUT1A	DMOS Full Bridge 1, output A
3	NC	No connection
4	MS1	Logic input
5	DIR	Logic input
6	STEP	Logic input
7, 18	GND	Ground terminals
8	REF	G_m reference input
9	ENABLE	Logic input
10	VDD	Logic supply
11	OUT2A	DMOS Full Bridge 2, output A
12	SENSE2	Sense resistor terminal for Full Bridge 2
13	VBB2	Load supply
14	OUT2B	DMOS Full Bridge 2, output B
15	VREG	Internal regulator
16	SLEEP/RESET	Logic input
17	ROSC	Oscillator input
19	VCP	Reservoir capacitor terminal
20	CP1	Charge pump capacitor terminal
21	CP2	Charge pump capacitor terminal
22	OUT1B	DMOS Full Bridge 1, output B
23	MS2	Logic input
24	VBB1	Load supply
–	PAD	Exposed thermal pad for enhanced thermal dissipation.

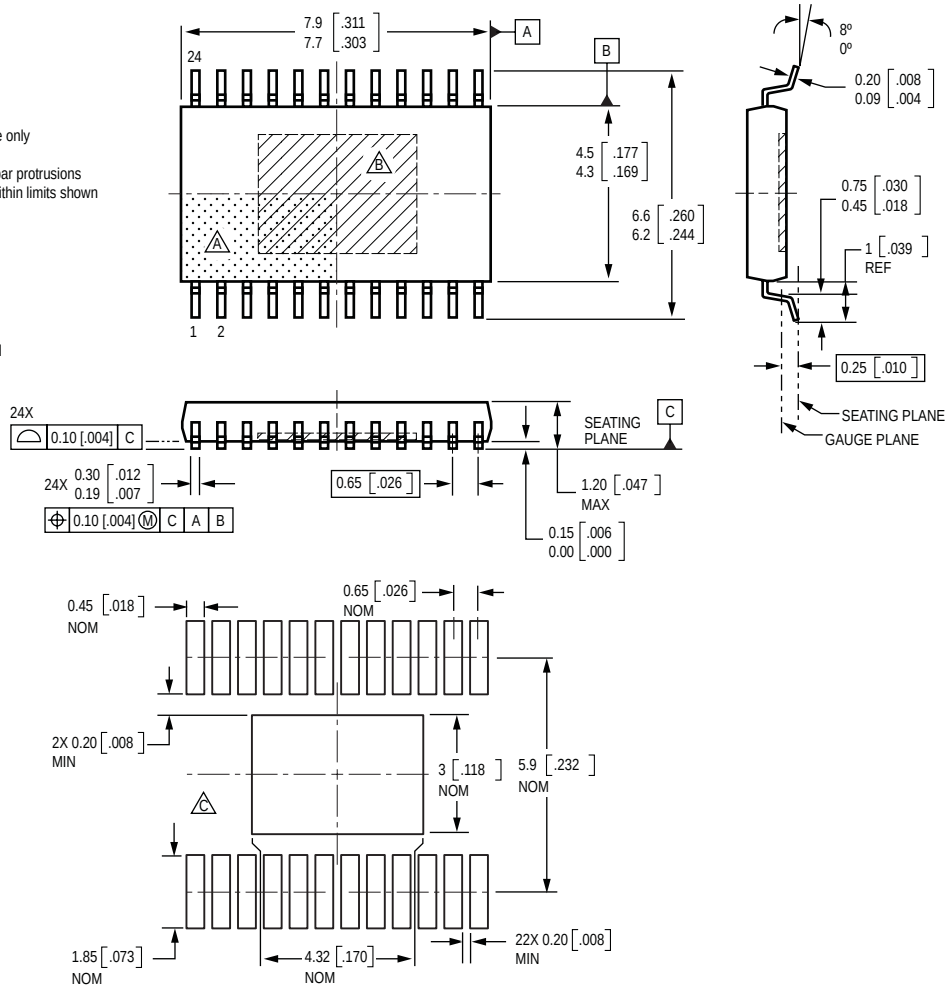
Package LP, 24 Pin TSSOP with Exposed Thermal Pad

Preliminary dimensions, for reference only
Dimensions in millimeters
U.S. Customary dimensions (in.) in brackets, for reference only
(reference JEDEC MO-153 ADT)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)



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