ALDEC 8051 IP Core Data Sheet

Overview

The 8051 core is the HDL model of the Intel™ 8-bit 8051 micro controller. The model is fully compatible with the Intel 8051 standard.

Features

- Opcode and Cycle Equivalent to Intel standard 8051
- Support for Intel Hex file format
- Up to 4K Bytes Internal Program Memory (ROM)
- Up to 128 Bytes Internal Data Memory (RAM)
- Up to 64K Bytes External Program Memory address space
- Up to 64K Bytes External Data Memory address space
- Up to 128 Special Function Registers (SFR)
- 32 bi-directional and individually addressable I/O Lines
- Two 16-bit timer/counters
- Full Duplex UART (Serial Port)
- 6-Source/5-Vector Interrupt Structure with Two Priority Levels

Pinout

Table 1: **Core Signal Pinout**

Name	Direction	Polarity	Description
CLK [1)]	Input	-	Clock input
EA [2)]	Input	Low	External Access
RST [2)]	Input	High	Synchronous reset
ALE [2)]	Output	High	Address Latch Enable
PSEN [2)]	Output	Low	Program Store Enable
P0[7:0] [3)]	Bidirectional	-	Port P0
P1[7:0] [3)]	Bidirectional	-	Port P1
P2[7:0] [3)]	Bidirectional	-	Port P2
P3[7:0] [3)]	Bidirectional	-	Port P3

Notes:

1) XTAL1 and XTAL2 original device pins were replaced with one CLK (clock) input signal. The clock frequency value has no limitations during the functional simulation.
2) EA, RST, ALE and PSEN signals behave exactly the same as the original device and are compatible with the Intel 8051 standard.
3) In the synthesizable model, each bidirectional pin is defined in the core interface as two separated VHDL ports. Optionally, using the Aldec VHDL/Verilog Interface, it can be merged to one bidirectional VHDL port. The behavioral model has bidirectional ports.

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Block Diagram

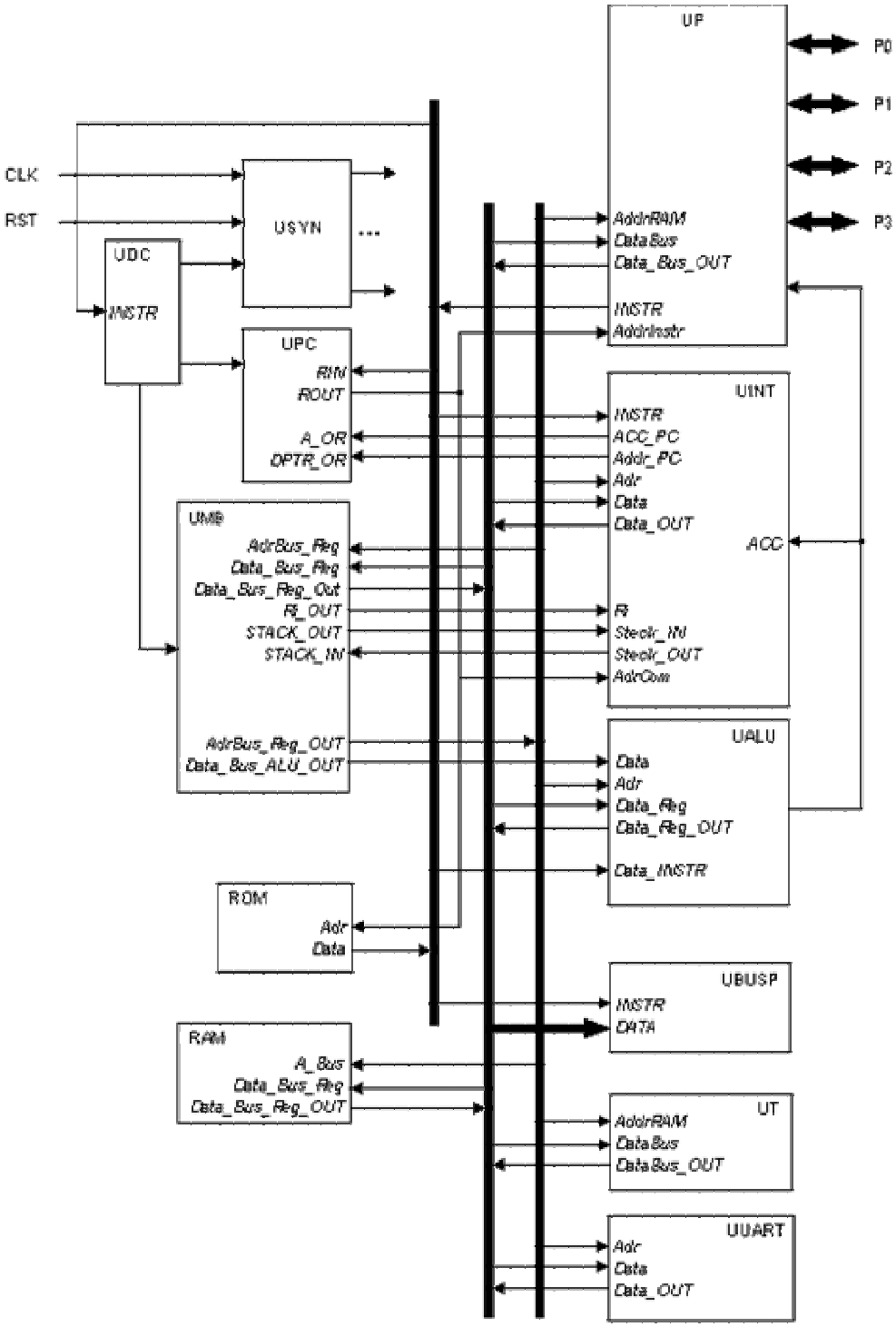

Figure 1: **Core Structure**

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Deliverables

Available at No Cost:

- Verilog and/or VHDL Simulation Model (Encrypted for Aldec simulator only)
- Data Sheet
- Application Notes

Available Upon ordering:

- VHDL/Verilog source code
- Internal program memory
- ROM Generator tool
- RAM memory
- Technology-dependent EDIF and VHDL/Verilog netlists
- Aldec 8051 VHDL/Verilog Interface
- Verification Test Bench source code
- RTL Source compilation and simulation scripts
- Synthesis scripts
- Integration Manual
- User-Guide

Ordering Information

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