74LVC2G74

Single D-type flip-flop with set and reset; positive edge trigger

Rev. 01 — 3 November 2005 Product data sheet

1. General description

The 74LVC2G74 is a high-performance, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC2G74 is a single positive edge triggered D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}D$) and ($\overline{R}D$) inputs, and complementary Q and $\overline{Q}$ outputs.

This device is fully specified for partial power down applications using I_{OFF}.
The I_{OFF} circuitry disables the output, preventing damaging backflow current through the device when it is powered down.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable, one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action at all inputs makes the circuit highly tolerant to slower input rise and fall times.

2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant inputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ±24 mA output drive (V_{CC} = 3.0 V)
- ESD protection:
  - HBM EIA/JESD22-A114-C exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

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3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay						
	CP to Q, $\overline{Q}$	C_L = 50 pF; V_{CC} = 3.3 V		-	3.5	-	ns
	$\overline{SD}$ to Q, $\overline{Q}$	C_L = 50 pF; V_{CC} = 3.3 V		-	3.0	-	ns
	$\overline{RD}$ to Q, $\overline{Q}$	C_L = 50 pF; V_{CC} = 3.3 V		-	3.0	-	ns
f_{max}	maximum input clock frequency	C_L = 50 pF; V_{CC} = 3.3 V		-	280	-	MHz
C_i	input capacitance			-	4.0	-	pF
C_{PD}	power dissipation capacitance	V_{CC} = 3.3 V	[1] [2]	-	15	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC2G74DP	–40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G74DC	–40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G74GT	–40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1

5. Marking

Table 3: Marking

Type number	Marking code
74LVC2G74DP	V74
74LVC2G74DC	V74
74LVC2G74GT	V74

6. Functional diagram

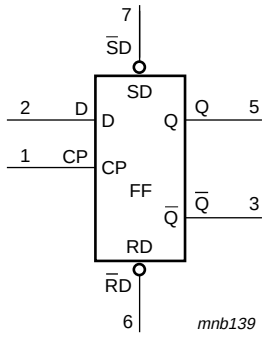


Fig 1. Logic symbol

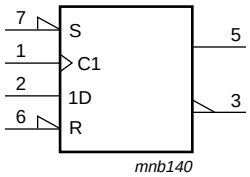


Fig 2. IEC logic symbol

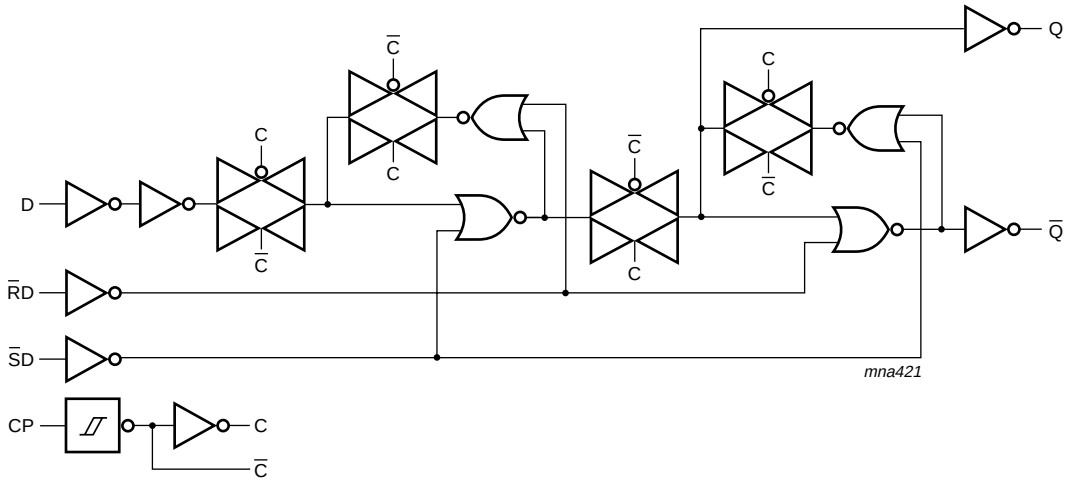


Fig 3. Logic diagram

7. Pinning information

7.1 Pinning

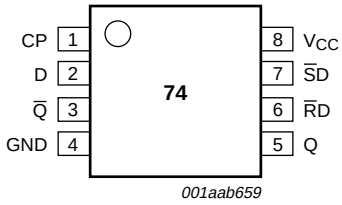
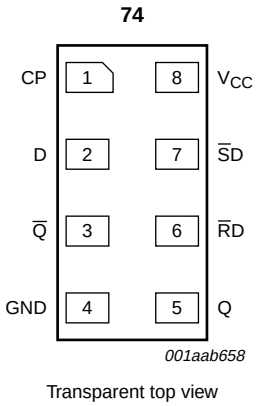


Fig 4. Pin configuration TSSOP8 and VSSOP8



Transparent top view

Fig 5. Pin configuration XSON8

7.2 Pin description

Table 4: Pin description

Symbol	Pin	Description
CP	1	clock input (LOW-to-HIGH, edge-triggered)
D	2	data input
$\overline{Q}$	3	complement flip-flop output
GND	4	ground (0 V)
Q	5	true flip-flop output
$\overline{RD}$	6	asynchronous reset-direct input (active LOW)
$\overline{SD}$	7	asynchronous set-direct input (active LOW)
V_{CC}	8	supply voltage

8. Functional description

8.1 Function table

Table 5: Function table for asynchronous operation [1]

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

Table 6: Function table for synchronous operation [1]

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
↑ = LOW-to-HIGH CP transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition.

9. Limiting values

Table 7: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		-	–50	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	active mode	[1] [2]	–0.5	V_{CC} + 0.5	V
		Power-down mode	[1] [2]	–0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	quiescent supply current			-	±100	mA
I_{GND}	ground current			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C		-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

10. Recommended operating conditions

Table 8: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	active mode	0	-	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	-	5.5	V
T_{amb}	ambient temperature		–40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	0	-	10	ns/V

11. Static characteristics

Table 9: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]						
V_{IH}	HIGH-state input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OH}	HIGH-state output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} − 0.1	-	-	V
		I_O = −4 mA; V_{CC} = 1.65 V	1.2	1.54	-	V
		I_O = −8 mA; V_{CC} = 2.3 V	1.9	2.15	-	V
		I_O = −12 mA; V_{CC} = 2.7 V	2.2	2.50	-	V
		I_O = −24 mA; V_{CC} = 3.0 V	2.3	2.62	-	V
		I_O = −32 mA; V_{CC} = 4.5 V	3.8	4.11	-	V
V_{OL}	LOW-state output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.10	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	0.07	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	0.12	0.30	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	0.17	0.40	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	0.33	0.55	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	0.39	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 5.5 V	-	±0.1	±5	µA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	±0.1	±10	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	0.1	10	µA
ΔI_{CC}	additional quiescent supply current (per pin)	V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	5	500	µA
C_i	input capacitance		-	4.0	-	pF

Table 9: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OH}	HIGH-state output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} − 0.1	-	-	V
		I_O = −4 mA; V_{CC} = 1.65 V	0.95	-	-	V
		I_O = −8 mA; V_{CC} = 2.3 V	1.7	-	-	V
		I_O = −12 mA; V_{CC} = 2.7 V	1.9	-	-	V
		I_O = −24 mA; V_{CC} = 3.0 V	2.0	-	-	V
		I_O = −32 mA; V_{CC} = 4.5 V	3.4	-	-	V
V_{OL}	LOW-state output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.10	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.70	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.80	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 5.5 V	-	-	±20	µA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	-	±20	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	40	µA
ΔI_{CC}	additional quiescent supply current (per pin)	V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	-	5000	µA

[1] All typical values are measured at T_{amb} = 25 °C.

12. Dynamic characteristics

Table 10: Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]						
t_{PHL}, t_{PLH}	propagation delay					
	CP to Q, $\overline{Q}$	see Figure 6				
		V_{CC} = 1.65 V to 1.95 V	1.5	6.0	13.4	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	3.5	7.1	ns
		V_{CC} = 2.7 V	1.0	3.5	7.1	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.5 [2]	5.9	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	2.5	4.1	ns
	$\overline{SD}$ to Q, $\overline{Q}$	see Figure 7				
		V_{CC} = 1.65 V to 1.95 V	1.5	6.0	12.9	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	3.5	7.0	ns
		V_{CC} = 2.7 V	1.0	3.5	7.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.0 [2]	5.9	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	2.5	4.1	ns
	$\overline{RD}$ to Q, $\overline{Q}$	see Figure 7				
		V_{CC} = 1.65 V to 1.95 V	1.5	5.0	12.9	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	3.5	7.0	ns
		V_{CC} = 2.7 V	1.0	3.5	7.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.0 [2]	5.9	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	2.5	4.1	ns
t_W	pulse width					
	clock CP HIGH or LOW	see Figure 6				
		V_{CC} = 1.65 V to 1.95 V	6.2	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	2.7	-	-	ns
		V_{CC} = 2.7 V	2.7	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.7	1.3 [2]	-	ns
		V_{CC} = 4.5 V to 5.5 V	2.0	-	-	ns
	set $\overline{SD}$ (LOW) and reset $\overline{RD}$ (LOW)	see Figure 7				
		V_{CC} = 1.65 V to 1.95 V	6.2	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	2.7	-	-	ns
		V_{CC} = 2.7 V	2.7	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.7	1.6 [2]	-	ns
		V_{CC} = 4.5 V to 5.5 V	2.0	-	-	ns

Table 10: Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rec}	recovery time					
	set $\overline{SD}$ or reset $\overline{RD}$	see Figure 7				
		V_{CC} = 1.65 V to 1.95 V	1.9	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.4	-	-	ns
		V_{CC} = 2.7 V	1.3	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	–3.0 [2]	-	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	-	-	ns
t_{su}	setup time					
	D to CP	see Figure 6				
		V_{CC} = 1.65 V to 1.95 V	2.9	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	ns
		V_{CC} = 2.7 V	1.7	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.3	0.5 [2]	-	ns
		V_{CC} = 4.5 V to 5.5 V	1.1	-	-	ns
t_h	hold time					
	D to CP	see Figure 6				
		V_{CC} = 1.65 V to 1.95 V	0.0	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	0.3	-	-	ns
		V_{CC} = 2.7 V	0.5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	0.6 [2]	-	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	-	-	ns
f_{max}	maximum input clock frequency	see Figure 6				
		V_{CC} = 1.65 V to 1.95 V	80	-	-	MHz
		V_{CC} = 2.3 V to 2.7 V	175	-	-	MHz
		V_{CC} = 2.7 V	175	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V	175	280 [2]	-	MHz
		V_{CC} = 4.5 V to 5.5 V	200	-	-	MHz

Table 10: Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay					
	CP to Q, $\overline{Q}$	see Figure 6				
		V_{CC} = 1.65 V to 1.95 V	1.5	-	13.4	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	-	7.1	ns
		V_{CC} = 2.7 V	1.0	-	7.1	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	-	5.9	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	-	4.1	ns
	$\overline{SD}$ to Q, $\overline{Q}$	see Figure 7				
		V_{CC} = 1.65 V to 1.95 V	1.5	-	12.9	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	-	7.0	ns
		V_{CC} = 2.7 V	1.0	-	7.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	-	5.9	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	-	4.1	ns
	$\overline{RD}$ to Q, $\overline{Q}$	see Figure 7				
		V_{CC} = 1.65 V to 1.95 V	1.5	-	12.9	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	-	7.0	ns
		V_{CC} = 2.7 V	1.0	-	7.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	-	5.9	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	-	4.1	ns
t_W	pulse width					
	clock CP HIGH or LOW	see Figure 6				
		V_{CC} = 1.65 V to 1.95 V	6.2	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	2.7	-	-	ns
		V_{CC} = 2.7 V	2.7	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.7	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	2.0	-	-	ns
	set $\overline{SD}$ (LOW) and reset $\overline{RD}$ (LOW)	see Figure 7				
		V_{CC} = 1.65 V to 1.95 V	6.2	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	2.7	-	-	ns
		V_{CC} = 2.7 V	2.7	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.7	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	2.0	-	-	ns
t_{rec}	recovery time					
	set $\overline{SD}$ or reset $\overline{RD}$	see Figure 7				
		V_{CC} = 1.65 V to 1.95 V	1.9	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.4	-	-	ns
		V_{CC} = 2.7 V	1.3	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	-	-	ns

Table 10: Dynamic characteristics *…continued*

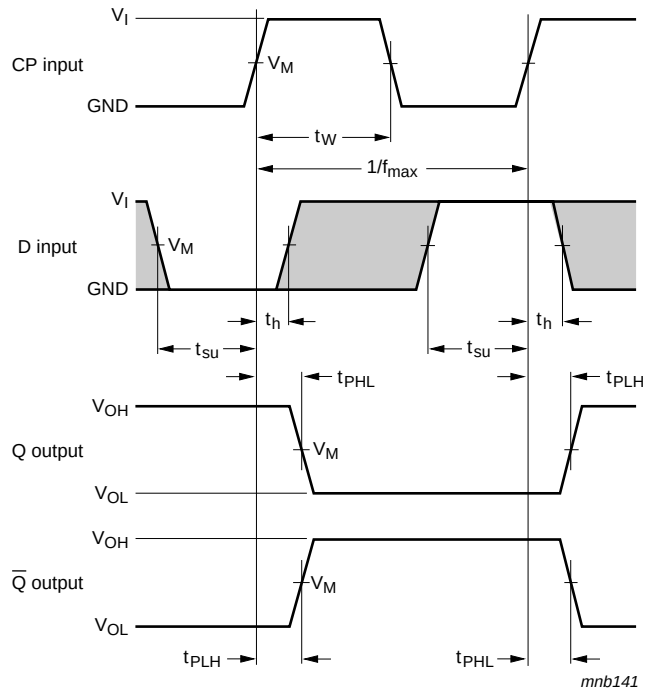
Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{su}	setup time					
	D to CP	see Figure 6				
		V_{CC} = 1.65 V to 1.95 V	2.9	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	ns
		V_{CC} = 2.7 V	1.7	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.3	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	1.1	-	-	ns
t_h	hold time					
	D to CP	see Figure 6				
		V_{CC} = 1.65 V to 1.95 V	0.0	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	0.3	-	-	ns
		V_{CC} = 2.7 V	0.5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	-	-	ns
f_{max}	maximum input clock frequency	see Figure 6				
		V_{CC} = 1.65 V to 1.95 V	80	-	-	MHz
		V_{CC} = 2.3 V to 2.7 V	175	-	-	MHz
		V_{CC} = 2.7 V	175	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V	175	-	-	MHz
		V_{CC} = 4.5 V to 5.5 V	200	-	-	MHz

[1] All typical values are measured at T_{amb} = 25 °C.

[2] These typical values are measured at V_{CC} = 3.3 V.

13. Waveforms



Measurement points are given in Table 11.

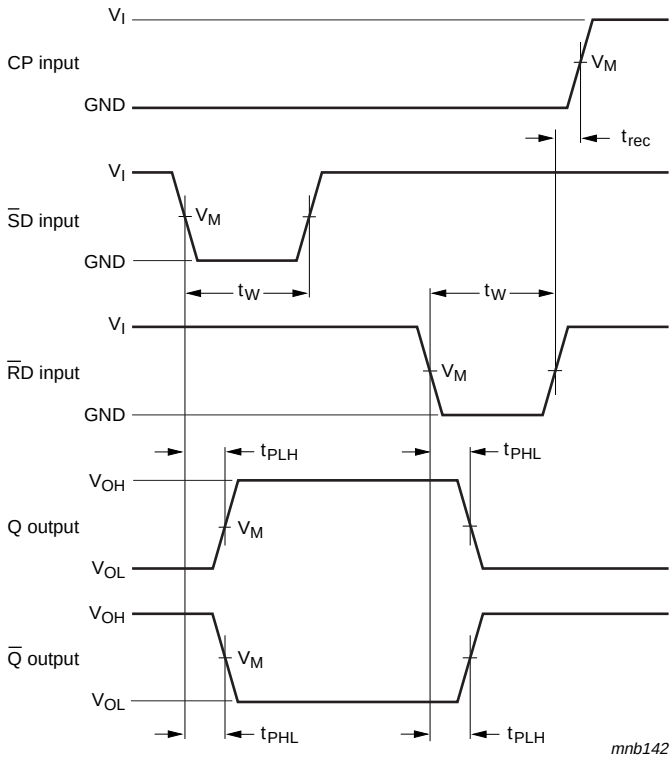
The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 6. The clock input (CP) to output (Q, $\overline{Q}$) propagation delays, the clock pulse width, the D to CP set-up, the CP to D hold times and the maximum clock pulse frequency

Table 11: Measurement points

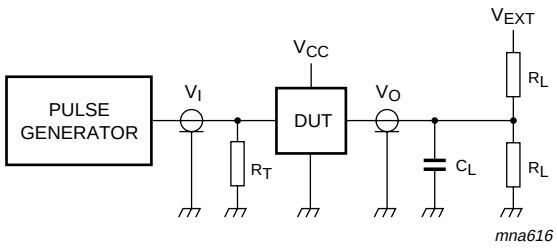
Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Measurement points are given in Table 11.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 7. The set ($\overline{SD}$) and reset ($\overline{RD}$) input to output (Q, $\overline{Q}$) propagation delays, the set and reset pulse widths and the $\overline{RD}$ to CP removal time



Test data is given in Table 12.

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

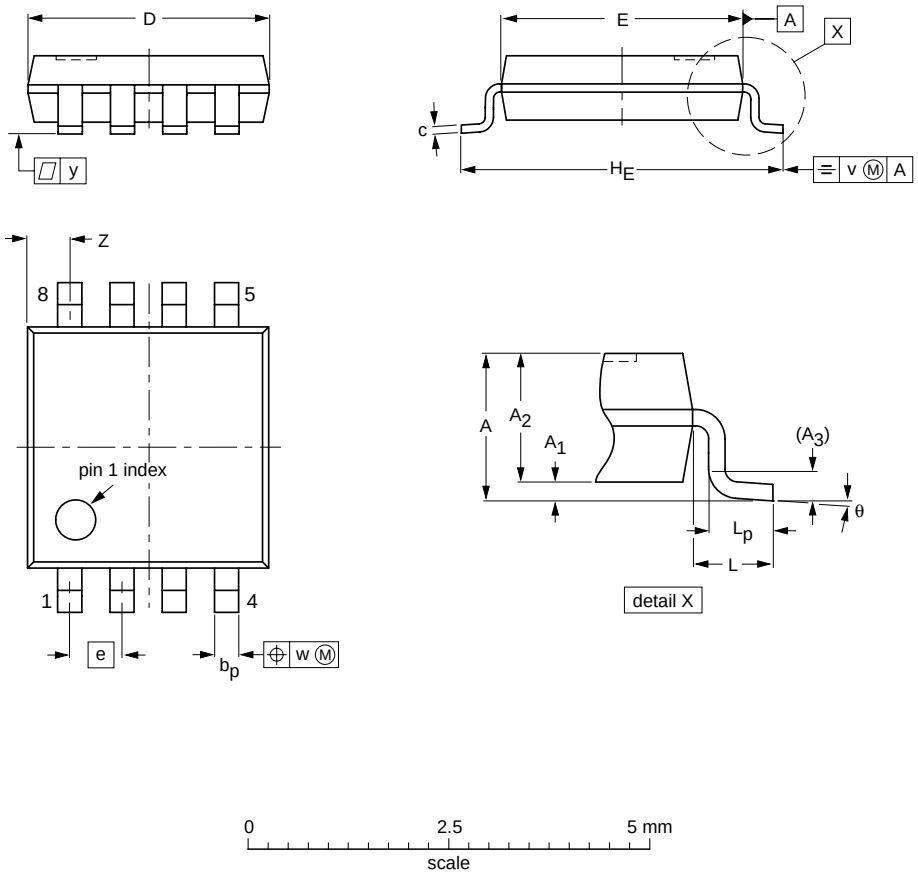
Fig 8. Load circuitry for switching times

Table 12: Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	GND	$2 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

14. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

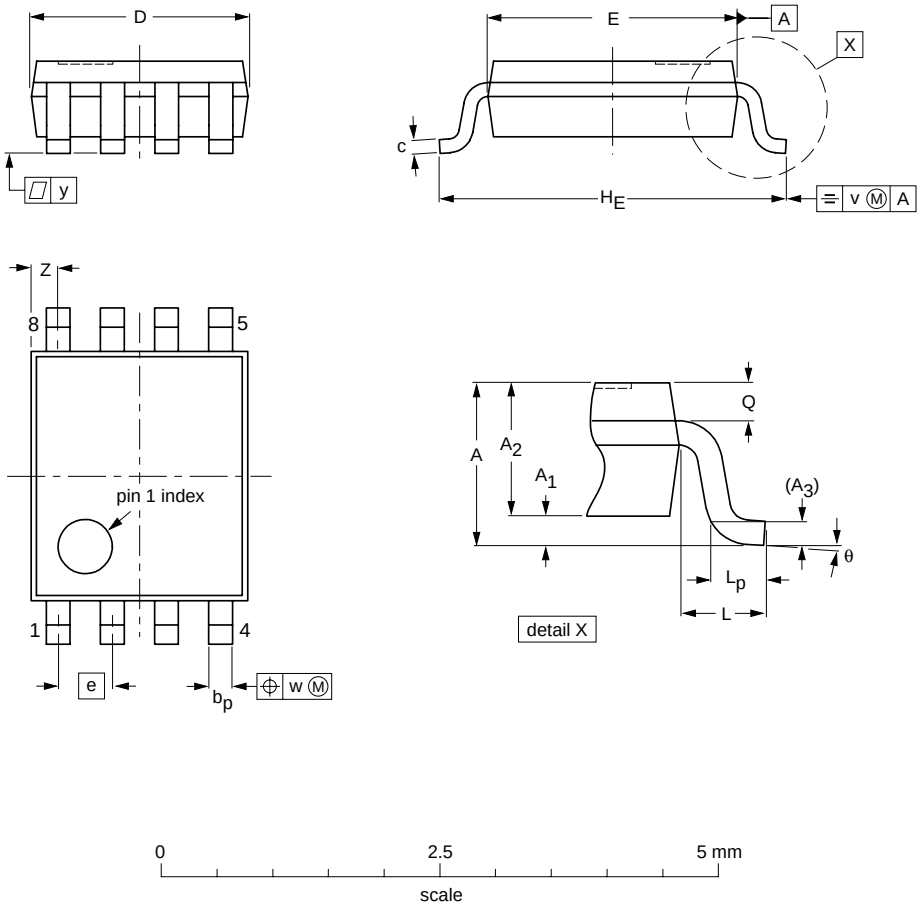
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig 9. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

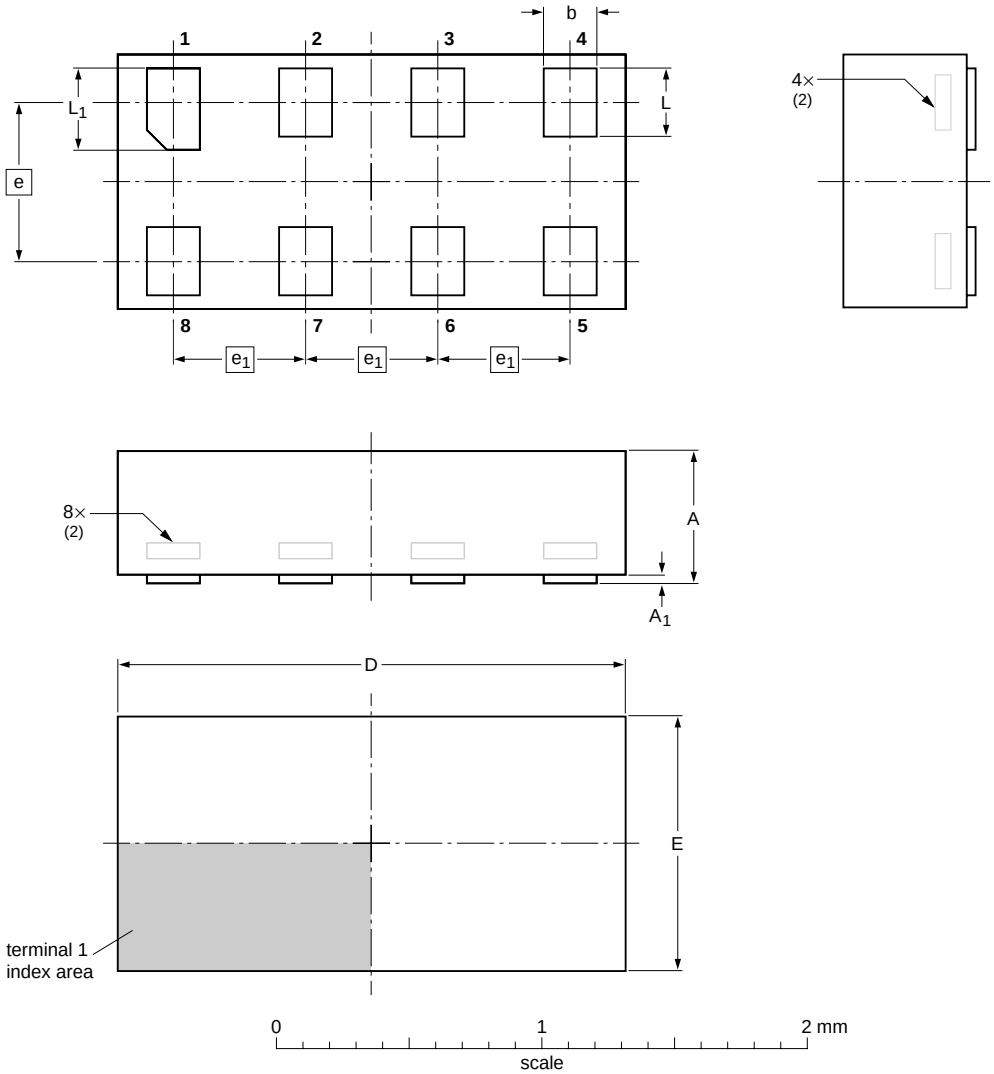
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 10. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A1 max	b	D	E	e	e1	L	L1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~04-07-22~~ 04-11-09

Fig 11. Package outline SOT833-1 (XSON8)

15. Abbreviations

Table 13: Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
TTL	Transistor Transistor Logic
HBM	Human Body Model
ESD	ElectroStatic Discharge
MM	Machine Model
CDM	Charged Device Model
DUT	Device Under Test

16. Revision history

Table 14: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LVC2G74_1	20051103	Product data sheet	-	-	-

17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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22. Contents

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