

74LCX540

Low Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs

Features

- 5V tolerant input and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 6.5ns t_{PD} max ($V_{CC} = 3.3V$), 10 μ A I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal⁽¹⁾
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds JEDEC 78 conditions
- ESD performance
 - Human body model > 2000V
 - Machine model > 200V
- Leadless Pb-Free DQFN package

General Description

The LCX540 is an octal buffer/line driver designed to be employed as a memory and address driver, clock driver and bus oriented transmitter/receiver.

This device is similar in function to the LCX240 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

The LCX540 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The LCX540 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Ordering Information

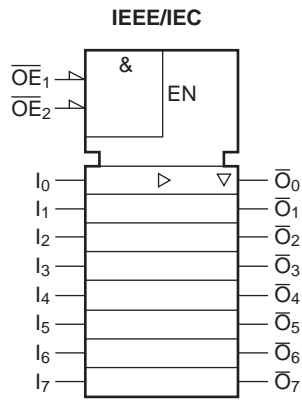
Order Number	Package Number	Package Description
74LCX540WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCX540SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX540BQX ⁽²⁾	MLP020B	Pb-Free 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm
74LCX540MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LCX540MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LCX540MTC_NL ⁽³⁾	MTC20	Pb-Free 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Notes:

1. To ensure the high impedance state during power up or down, \overline{OE} should be tied to V_{CC} through a pull-up resistor: the minimum value of the resistor is determined by the current-sourcing capability of the driver.
2. DQFN package available in Tape and Reel only.
3. "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

Logic Symbol



Pin Descriptions

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs
I_0-I_7	Inputs
$\overline{O}_0-\overline{O}_7$	Outputs

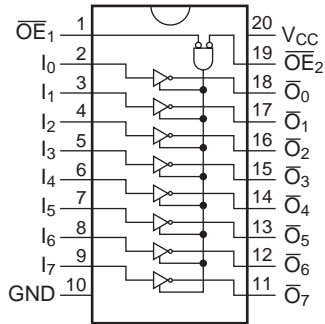
Truth Table

Inputs			Outputs
\overline{OE}_1	\overline{OE}_2	I	\overline{O}_n
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

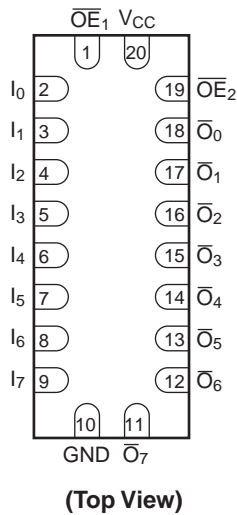
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Connection Diagrams

Pin Assignments for SOIC, SOP, SSOP, TSSOP



Pad Assignment for DQFN



Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Symbol	Parameter	Conditions	Value	Units
V_{CC}	Supply Voltage		-0.5 to +7.0	V
V_I	DC Input Voltage		-0.5 to +7.0	V
V_O	DC Output Voltage	Output in 3-STATE	-0.5 to +7.0	V
		Output in HIGH or LOW State ⁽⁴⁾	-0.5 to $V_{CC} + 0.5$	
I_{IK}	DC Input Diode Current	$V_I < GND$	-50	mA
I_{OK}	DC Output Diode Current	$V_O < GND$	-50	mA
		$V_O > V_{CC}$	+50	
I_O	DC Output Source/Sink Current		± 50	mA
I_{CC}	DC Supply Current per Supply Pin		± 100	mA
I_{GND}	DC Ground Current per Ground Pin		± 100	mA
T_{STG}	Storage Temperature		-65 to +150	°C

Recommended Operating Conditions⁽⁵⁾

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	$V_{CC} = 3.0V - 3.6V$	-	± 24	mA
		$V_{CC} = 2.7V - 3.0V$	-	± 12	
		$V_{CC} = 2.3V - 2.7V$	-	± 8	
T_A	Free-Air Operating Temperature		-40	85	°C
$\Delta t/\Delta V$	Input Edge Rate	$V_{IN} = 0.8V - 2.0V, V_{CC} = 3.0V$	0	10	ns/V

Notes:

- I_O Absolute Maximum Rating must be observed.
- Unused inputs or I/O's must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units
				Min.	Max.	
V _{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7	–	V
			2.7 – 3.6	2.0	–	
V _{IL}	LOW Level Input Voltage		2.3 – 2.7	–	0.7	V
			2.7 – 3.6	–	0.8	
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100μA	2.3 – 3.6	V _{CC} - 0.2	–	V
		I _{OH} = -8mA	2.3	1.8	–	
		I _{OH} = -12mA	2.7	2.2	–	
		I _{OH} = -18mA	3.0	2.4	–	
		I _{OH} = -24mA	3.0	2.2	–	
V _{OL}	LOW Level Output Voltage	I _{OL} = 100μA	2.3 – 3.6	–	0.2	V
		I _{OL} = 8mA	2.3	–	0.6	
		I _{OL} = 12mA	2.7	–	0.4	
		I _{OL} = 16mA	3.0	–	0.4	
		I _{OL} = 24mA	3.0	–	0.55	
I _I	Input Leakage Current	0 ≤ V _I ≤ 5.5V	2.3 – 3.6	–	±5.0	μA
I _{OZ}	3-STATE Output Voltage	0 ≤ V _O ≤ 5.5V, V _I = V _{IH} or V _{IL}	2.3 – 3.6	–	±5.0	μA
I _{OFF}	Power-Off Leakage Current	V _I or V _O = 5.5V	0	–	10	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.3 – 3.6	–	10	μA
		3.6V ≤ V _I , V _O ≤ 5.5V ⁽⁶⁾	2.3 – 3.6	–	±10	
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.3 – 3.6	–	500	μA

AC Electrical Characteristics

Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500Ω						Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2V		
		C _L = 50pF		C _L = 50pF		C _L = 30pF		
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PHL} , t _{PLH}	Propagation Delay	1.5	6.5	1.5	7.5	1.5	7.8	ns
t _{PZL} , t _{PZH}	Output Enable Time	1.5	8.5	1.5	9.5	1.5	10.5	ns
t _{PLZ} , t _{PHZ}	Output Disable Time	1.5	7.5	1.5	8.5	1.5	9.0	ns
t _{OSHL} , t _{OSLH}	Output to Output Skew ⁽⁷⁾	–	1.0	–	–	–	–	ns

Notes

- Outputs disabled or 3-STATE only.
- Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C	Units
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V
		C _L = 30pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	0.6	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	-0.8	V
		C _L = 30pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	-0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0V or V _{CC}	7	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC} , f = 10 MHz	25	pF

AC Loading and Waveforms (Generic for LCX Family)

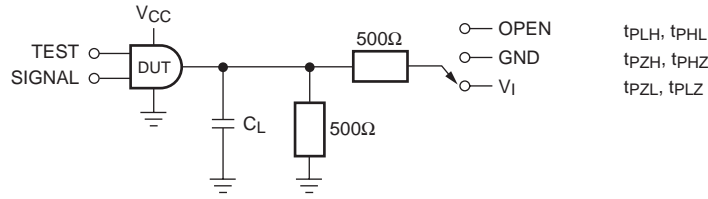
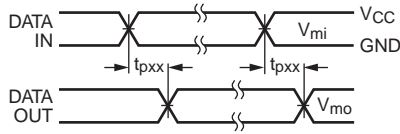
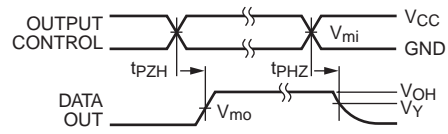


Figure 1. AC Test Circuit (C_L includes probe and jig capacitance)

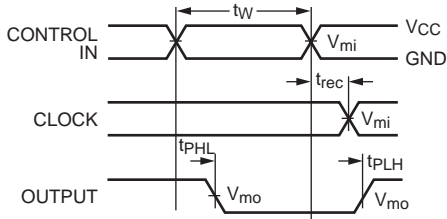
Test	Switch
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH} , t_{PHZ}	GND



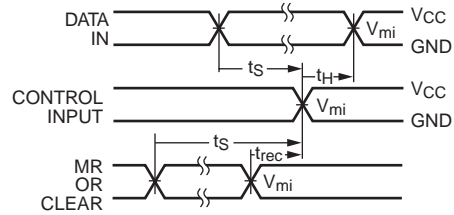
Waveform for Inverting and Non-Inverting Functions



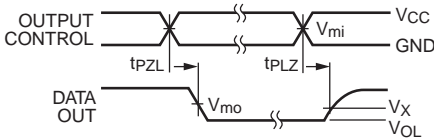
3-STATE Output High Enable and Disable Times for Logic



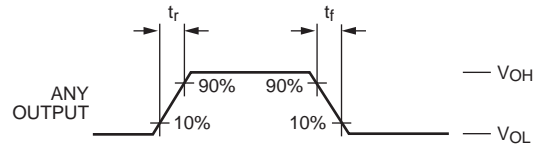
Propagation Delay, Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

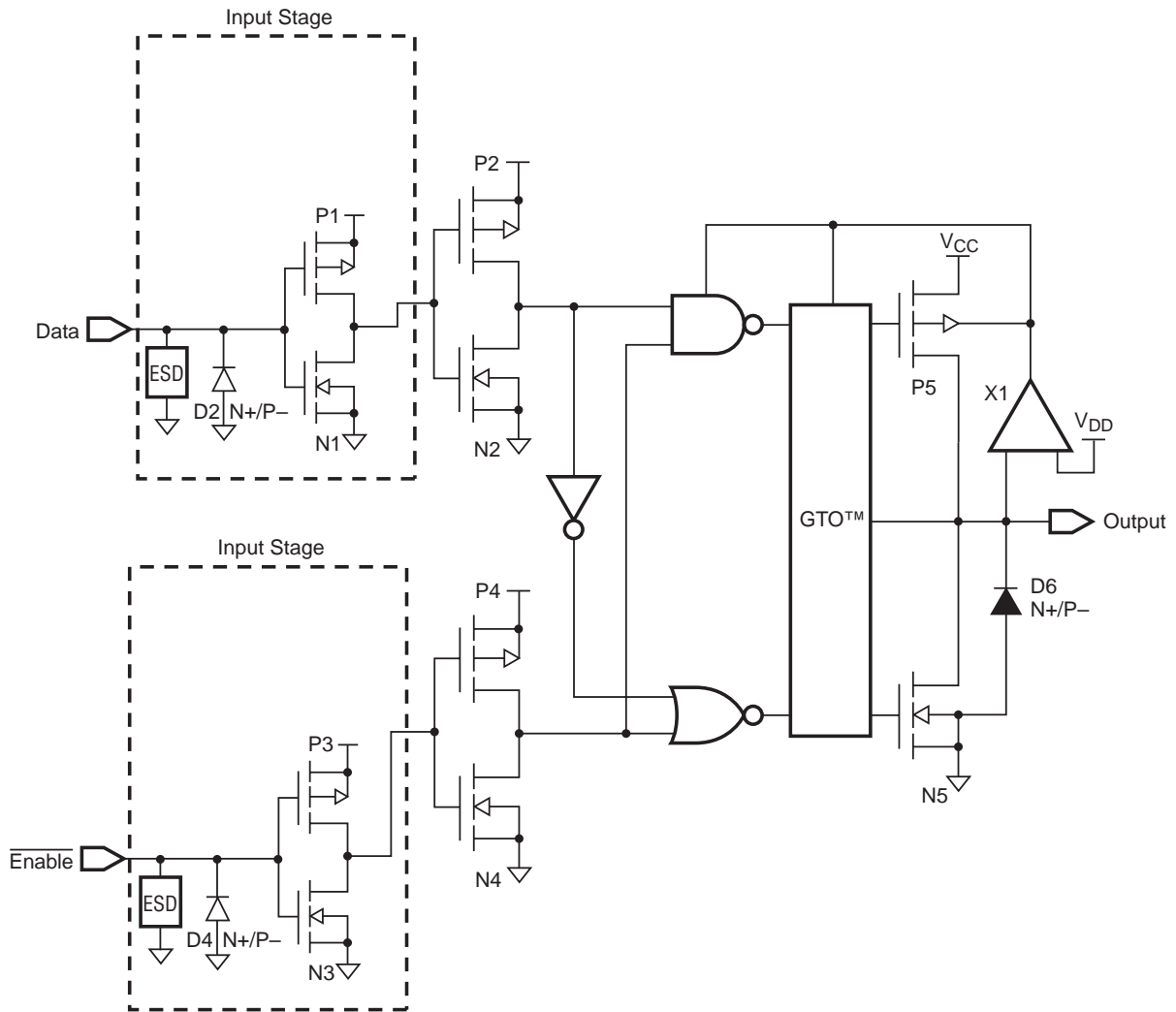


t_{rise} and t_{fall}

Figure 2. Waveforms (Input Characteristics; $f = 1MHz$, $t_r = t_f = 3ns$)

Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
V_{mi}	1.5V	1.5V	$V_{CC} / 2$
V_{mo}	1.5V	1.5V	$V_{CC} / 2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Schematic Diagram (Generic for LCX Family)

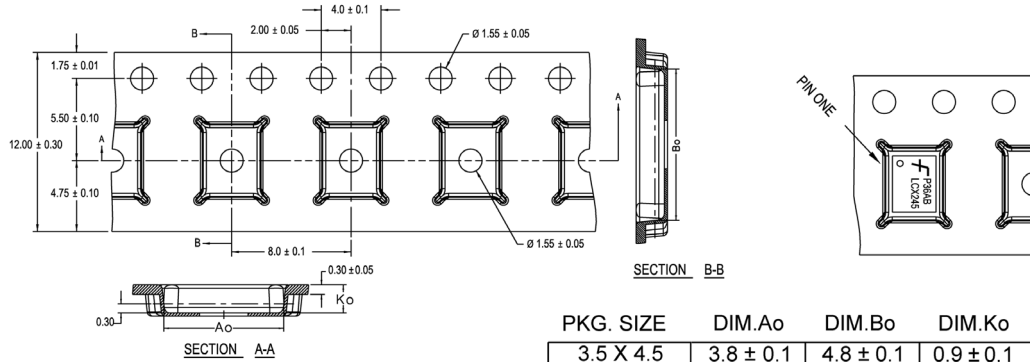


Tape and Reel Specification

Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

Tape Dimensions inches (millimeters)



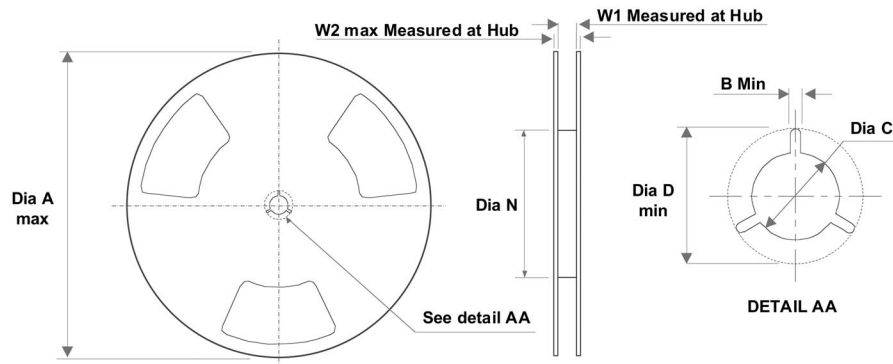
PKG. SIZE	DIM.A _o	DIM.B _o	DIM.K _o
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

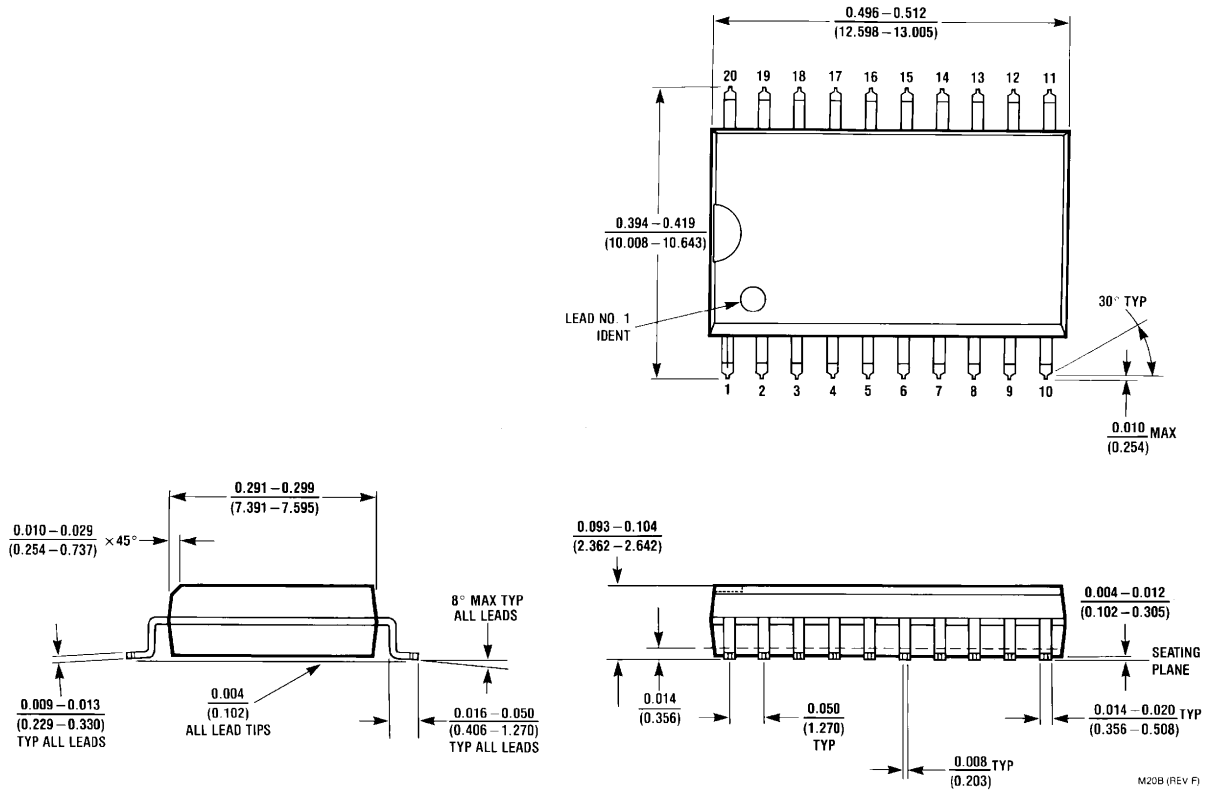
1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. A_o and B_o measured on a plane 0.120[0.30] above the bottom of the pocket.
6. K_o measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

Reel Dimensions inches (millimeters)



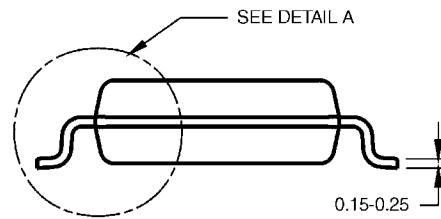
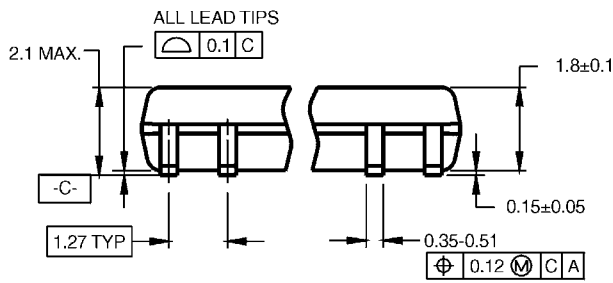
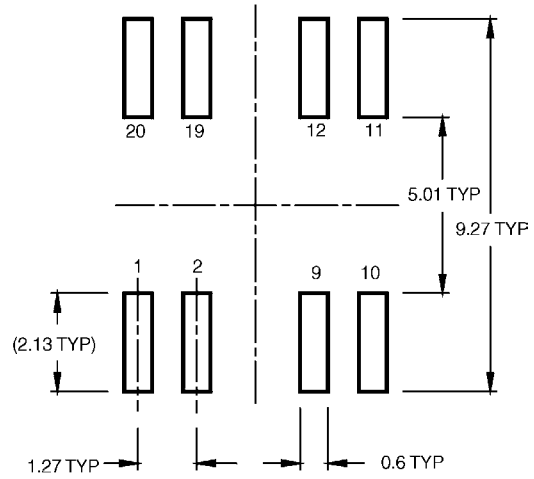
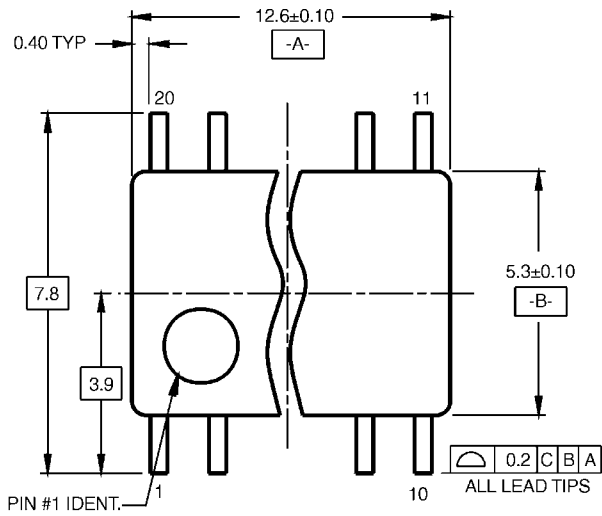
Tape Size	A	B	C	D	N	W1	W2
12mm	13.0 (330.0)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.488 (12.4)	0.724 (18.4)

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC),
JEDEC MS-013, 0.300" Wide Package Number M20B**

Physical Dimensions (Continued) millimeters unless otherwise noted

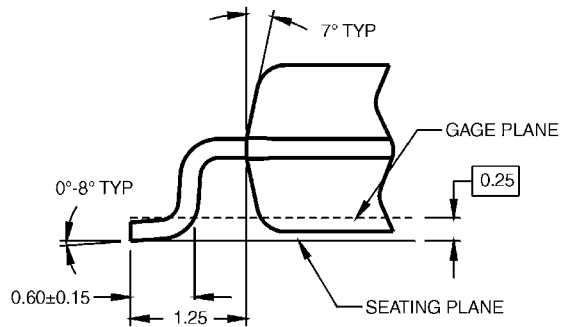


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NOTES:

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- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

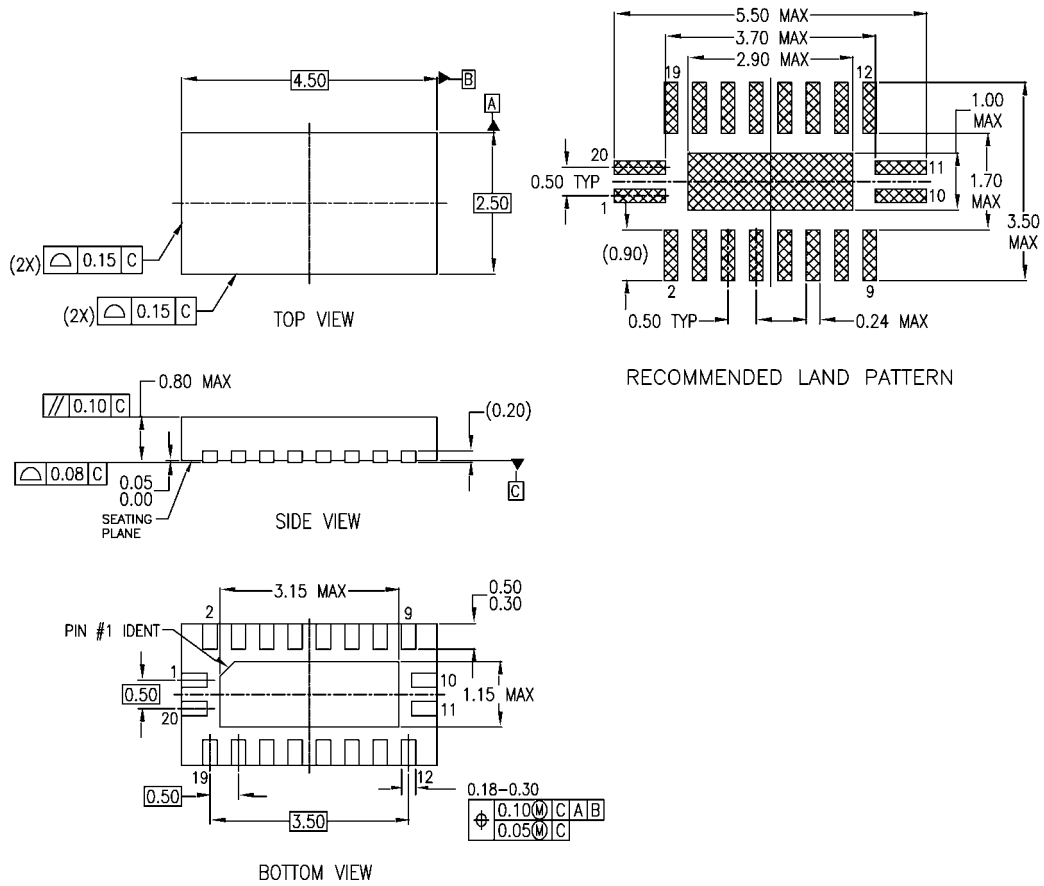
M20DRevB1



DETAIL A

**20-Lead Small Outline Package (SOP),
EIAJ TYPE II, 5.3mm Wide Package Number M20D**

Physical Dimensions (Continued) millimeters unless otherwise noted



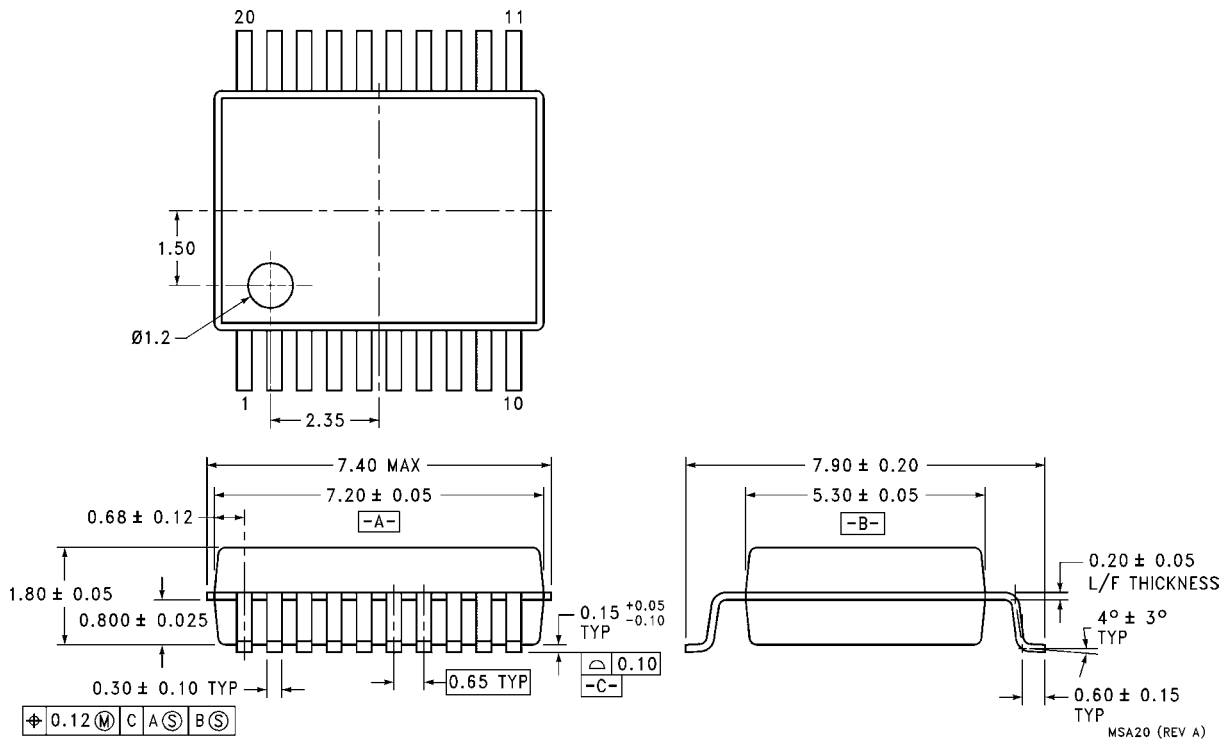
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AC
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP020BrevA

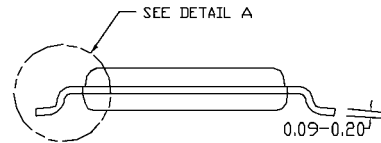
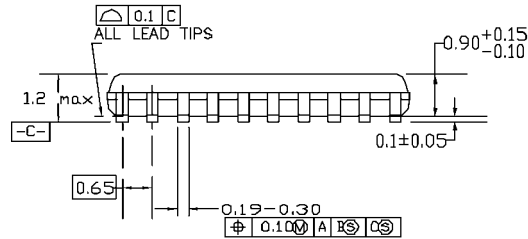
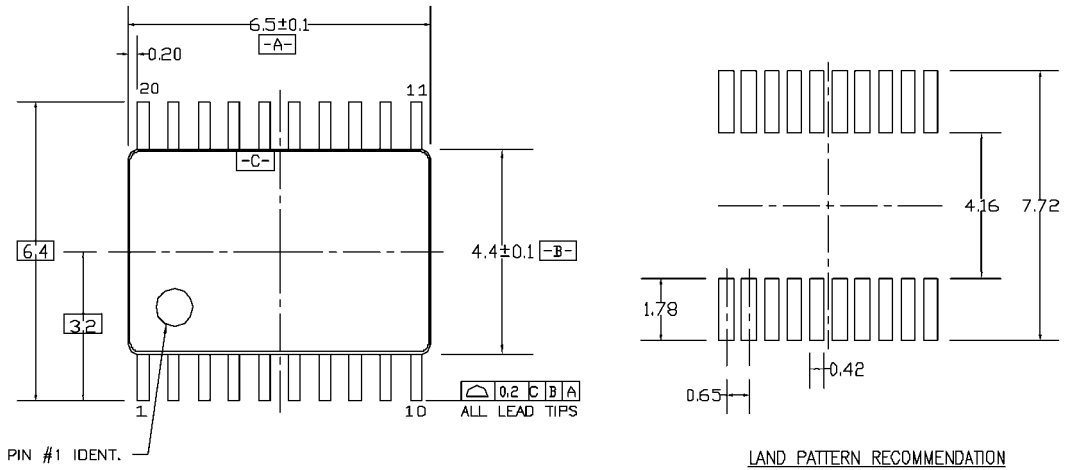
**Pb-Free 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN),
JEDEC MO-241, 2.5 x 4.5mm Package Number MLP020B**

Physical Dimensions (Continued) millimeters unless otherwise noted

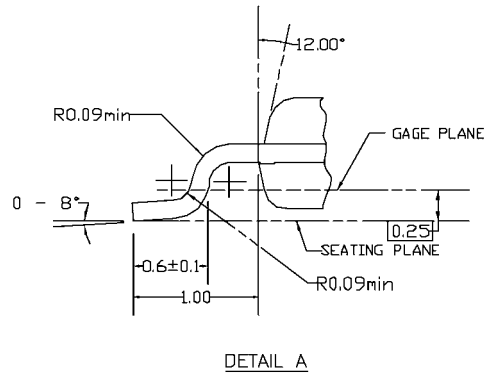


**20-Lead Shrink Small Outline Package (SSOP),
JEDEC MO-150, 5.3mm Wide Package Number MSA20**

Physical Dimensions (Continued) millimeters unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

**20-Lead Thin Shrink Small Outline Package (TSSOP),
JEDEC MO-153, 4.4mm Wide Package Number MTC20**

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CROSSVOLT TM	GTO TM	MICROWIRE TM	Quiet Series TM	TINYOPTO TM
DOME TM	HiSeC TM	MSX TM	RapidConfigure TM	TruTranslation TM
EcoSPARK TM	I ² C TM	MSXPro TM	RapidConnect TM	UHC TM
E ² CMOS TM	i-Lo TM	OCX TM	μSerDes TM	UltraFET [®]
EnSigna TM	ImpliedDisconnect TM	OCXPro TM	ScalarPump TM	UniFET TM
FACT TM	IntelliMAX TM	OPTOLOGIC [®]	SILENT SWITCHER [®]	VCX TM
FACT Quiet Series TM		OPTOPLANAR TM	SMART START TM	Wire TM
Across the board. Around the world. TM		PACMAN TM	SPM TM	
The Power Franchise [®]		POP TM	Stealth TM	
Programmable Active Droop TM		Power247 TM	SuperFET TM	
		PowerEdge TM	SuperSOT TM -3	

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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