STRUCTURE Silicon monolithic integrated circuits

PRODUCT SERIES 3-phase motor pre-driver for LBP

TYPE **BD6761FS**

FUNCTION
- Pre-driver for driving Nch MOS FET
- 180 degree direct PWM driver

○Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limit	Unit
Supply voltage	VCC	36	V
	VG	36	V
Power dissipation	Pd	950※1	mW
Input voltage	VIN	VREG	V
Operating temperature range	Topr	-35～+75	℃
Storage temperature range	Tstg	-40～+150	℃
Junction temperature	Tjmax	150	℃

※1 70mm×70mm×1.6mm glass epoxy board. Derating in done at 7.6mW/℃ for operating above Ta=25℃.

○Recommended operating conditions (Ta=-35～+75℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VCC	16	24	28	V

This product described in this specification isn't judged whether it applies to COCOM regulations.
Please confirm in case of export.
This product isn't designed for protection against radioactive rays.

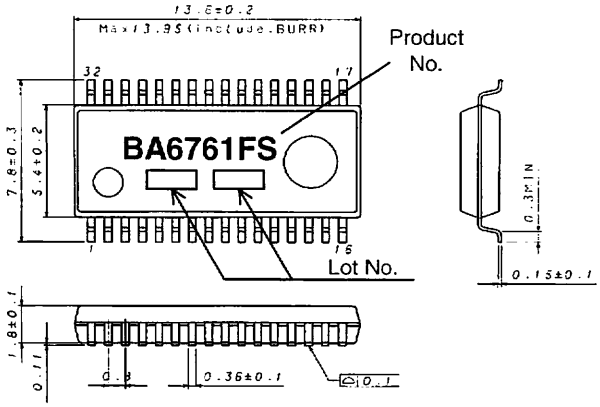
○Electrical characteristics (Unless otherwise specified, Ta=25℃, VCC=24V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
overall						
Circuit current	ICC	10	15	20	mA	
VREG voltage	VREG	5.5	6	6.5	V	IVREG=-1mA
Hall amp						
Input bias current	IHA	–	0.7	3.0	uA	
In-phase input voltage range	VHAR	1.5	–	4.1	V	
Input level	VINH	30	–	250	mVpp	Amplitude per one hall phase
PWM						
High CFE voltage	VHPCFE	3.0	3.5	4.0	V	
Low CFE voltage	VLPCFE	2.1	2.5	2.9	V	
CFE oscillating frequency	FCFE	12	15	18	kHz	RFE=50kΩ CFE=1000pF
PWM on duty offset	DPWM	-1.5	0	1.5	%	
Torque amplifier						
High CPOUT input current	ICPOUTH	–	0	1	uA	
Low CPOUT input current	ICPOUTL	-1	0	–	uA	
Current limit						
Current detection voltage 1	VCL1	0.391	0.435	0.479	V	for current sense amp
Current detection voltage 2	VCL2	0.432	0.480	0.528	V	for current limit comp
VCL2－VCL1	ΔVCL	40	45	50	mV	
FG Amp						
Input bias current	IBFG	-1	–	1	uA	
Input offset voltage	VBFG	-10	–	10	mV	
High output voltage	VHFG	4.5	5.0	VREG	V	IHFGOUT=-0.75mA
Low output voltage	VLFG	–	1.0	1.5	V	ILFGOUT=2mA
Low FGS output voltage	VLFGS	–	0.1	0.3	V	ILFGSOUT=3mA
Open loop gain	GVFG	45	54	–	dB	f=3kHz
Bias voltage	VBIASFG	2.7	3.0	3.3	V	
Hysteresis width	VHYS	100	180	250	mV	
F/R						
High input current	IFRL	30	60	90	uA	F/R=6V
Low input current	IFRH	-10	0	10	uA	F/R=0V
High input level	VIHFR	2.2	–	VREG	V	reverse
Low input level	VILFR	0	–	0.8	V	forward
ACC and DEC						
High ACC input current	IACCH	30	60	90	uA	ACC=6V
Low ACC input current	IACCL	-10	0	10	uA	ACC=0V
High DEC input current	IDECH	30	60	90	uA	DEC=6V
Low DEC input current	IDECL	-10	0	10	uA	DEC=0V
Accelerating current	ISS	-260	-200	-140	uA	RCP=13.5KΩ、ACC=L
Decelerating current	ISO	140	200	260	uA	RCP=13.5KΩ、DEC=L
High ACC input level	VIHACC	2.2	–	VREG	V	
Low ACC input level	VILACC	0	–	0.8	V	
High DEC input level	VIHDEC	2.2	–	VREG	V	
Low DEC input level	VILDEC	0	–	0.8	V	
High-side output						
High-side voltage	VHG	Vcc+5	Vcc+6	Vcc+7	V	
Pull-down resistor	RHD	70	100	130	kΩ	

○Electrical characteristics (Unless otherwise specified, Ta=25℃, VCC=24V)

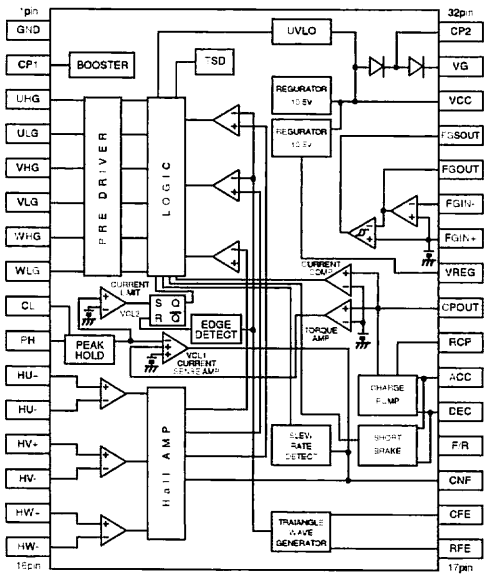
Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Low-side output						
Low-side voltage	VLG	9.5	10.5	11.5	V	
Pull-down resistor	RLD	70	100	130	kΩ	
Booster						
Boost voltage	VG	Vcc+5	Vcc+6	Vcc+7	V	
CP1 oscillating frequency	FCP1	35	62.5	85	kHz	

○Package outline



SSOP-A32 (Unit: mm)

○Block diagram



○Pin No. / Pin name

Pin No.	Pin name	Pin No.	Pin name
1	GND	17	RFE
2	CP1	18	CFE
3	UHG	19	CNF
4	ULG	20	F/R
5	VHG	21	DEC
6	VLG	22	ACC
7	WHG	23	RCP
8	WLG	24	CPOUT
9	CL	25	VREG
10	PH	26	FGIN+
11	HU+	27	FGIN-
12	HU-	28	FGOUT
13	HV+	29	FGSOUT
14	HV-	30	VCC
15	HW+	31	VG
16	HW-	32	CP2

○Operation Notes

(1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range (Topr) may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. The implementation of a physical safety measure such as a fuse should be considered when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

(2) Power supply lines

Regenerated current may flow as a result of the motor's back electromotive force. Insert capacitors between the power supply and ground pins to serve as a route for regenerated current. Determine the capacitance in full consideration of all the characteristics of the electrolytic capacitor, because the electrolytic capacitor may loose some capacitance at low temperatures. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.

(3) Ground potential

Ensure a minimum GND pin potential in all operating conditions.

(4) Setting of heat

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(5) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

(6) ASO

When using the IC, set the output transistor for the motor so that it does not exceed absolute maximum ratings or ASO.

(7) Thermal shutdown circuit

This IC incorporates a TSD (thermal shutdown) circuit (TSD circuit). If the temperature of the chip reaches the following temperature, the motor coil output will be opened. The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

TSD on temperature [°C] (typ.)	Hysteresis temperature [°C] (typ.)
175	35

(8) Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

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