24-Bit Capacitance-to-Digital Converter with Temperature Sensor

Preliminary Technical Data

AD7747

FEATURES

Capacitance-to-digital converter
- **New standard in single chip solutions**
- **Interfaces to single or differential grounded sensors**
- **Resolution down to 40 aF (that is, up to 18.5-bit ENOB)**
- **Accuracy: 8 fF**
- **Linearity: 0.01%**
- **Common-mode (not changing) capacitance up to 17 pF**
- **Full scale (changing) capacitance range ±8 pF**
- **Update rate: 5 Hz to 45 Hz**
- **Simultaneous 50 Hz and 60 Hz rejection at 8.1 Hz update**
- **Active shield for shielding sensor connection**

Temperature sensor on-chip
- **Resolution: 0.1°C, accuracy: ±2°C**

Voltage input channel

Internal clock oscillator

2-wire serial interface (I²C®-compatible)

Power
- **2.7 V to 5.25 V single-supply operation**
- **1 mA current consumption**

Operating temperature: –40°C to +125°C

16-lead TSSOP package

APPLICATIONS

Automotive, industrial, and medical systems for
- **Pressure measurement**
- **Position sensing**
- **Proximity sensing**
- **Level sensing**
- **Flowmeters**
- **Impurity detection**

GENERAL DESCRIPTION

The AD7747 is a high-resolution, Σ–Δ capacitance-to-digital converter (CDC). The capacitance to be measured is connected directly to the device inputs. The architecture features inherent high resolution (24-bit no missing codes, up to 18 bit effective resolution), high linearity (±0.01%), and high accuracy (±8 fF factory calibrated). The AD7747 capacitance input range is ±8 pF (changing), while it can accept up to 17 pF common-mode capacitance (not changing), which can be balanced by a programmable on-chip digital-to-capacitance converter (CAPDAC).

The AD7747 is designed for single ended or differential capacitive sensors with one plate connected to ground. For floating (not grounded) capacitive sensors, the AD7745 or AD7746 are recommended.

The part has an on-chip temperature sensor with a resolution of 0.1°C and accuracy of ±2°C. The on-chip voltage reference and the on-chip clock generator eliminate the need for any external components in capacitive sensor applications. The part has a standard voltage input, which together with the differential reference input allows easy interface to an external temperature sensor, such as an RTD, thermistor, or diode.

The AD7747 has a 2-wire, I²C-compatible serial interface. The part can operate with a single power supply 2.7 V to 5.25 V. It is specified over the automotive temperature range of –40°C to +125°C and are housed in a 16-lead TSSOP package.

FUNCTIONAL BLOCK DIAGRAMS

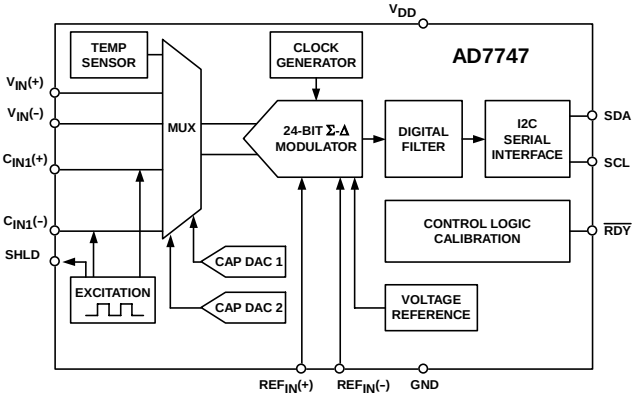

Figure 1.

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REVISION HISTORY

March 2005—Revision PrB: Preliminary sampling, chip rev.S2

July 2006—Revision PrC: Preliminary sampling, chip rev.S3

SPECIFICATIONS

V_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V; GND = 0 V; EXC = ±V_{DD}/2; –40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CAPACITIVE INPUT					
Conversion Input Range		±8.192		pF[1]	Factory calibrated
Integral Nonlinearity (INL)[2]			±0.01	% of FSR	
No Missing Codes[2]	24			Bit	Conversion time ≥ 124 ms
Resolution, p-p		16		Bit	Conversion time 124 ms, see Table 5
Resolution Effective		18.5		Bit	Conversion time 124 ms, see Table 5
Output Noise, rms		15		aF/√Hz	See Table 5
Absolute Error[3]			±8	fF[1]	25°C, V_{DD} = 5 V, after offset calibration
Offset Error[2, 4]			TBD	aF[1]	After system offset calibration, Excluding effect of noise[4]
System Offset Calibration Range[2]			TBD	pF	
Offset Drift vs. Temperature		TBD		aF/°C	
Gain Error[5]		TBD		% of FS	25°C, V_{DD} = 5 V
Gain Drift vs. Temperature[2]		–26		ppm of FS/°C	
Power Supply Rejection		TBD		fF/V	
Normal Mode Rejection		TBD		dB	50 Hz ± 1%, conversion time 124 ms
		TBD		dB	60 Hz ± 1%, conversion time 124 ms
CAPDAC					
Full Range	17	21		pF	
Resolution[6]		330		fF	6-bit CAPDAC
Drift vs. Temperature[2]		26		ppm of FS/°C	
EXCITATION					
Frequency		16		kHz	
AC Voltage Across Capacitance		±V_{DD}/2		V	Configurable via digital interface
Average DC Voltage Across Capacitance		TBD		mV	
ACTIVE SHIELDING					
Allowed Capacitance to GND[2]			50	pF	SHLD pin
TEMPERATURE SENSOR[7]					V_{REF} internal
Resolution		0.1		°C	
Error[2]		±0.5	±2	°C	Internal temperature sensor
		±2		°C	External sensing diode[8]
VOLTAGE INPUT[7]					V_{REF} internal or V_{REF} = 2.5 V
Differential VIN Voltage Range		±V_{REF}		V	
Absolute VIN Voltage[2]	GND – 0.03		V_{DD} + 0.03	V	
Integral Nonlinearity (INL)		±3	±15	ppm of FS	
No Missing Codes[2]	24			Bit	Conversion time = 122.1 ms
Resolution, p-p		16		Bits	Conversion time = 62 ms See Table 6 and Table 7
Output Noise		3		µV rms	Conversion time = 62 ms See Table 6 and Table 7
Offset Error		±3		µV	
Offset Drift vs. Temperature		15		nV/°C	
Full-Scale Error[2, 9]		0.025	0.1	% of FS	
Full-Scale Drift vs. Temperature		5		ppm of FS/°C	Internal reference
		0.5		ppm of FS/°C	External reference

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Average VIN Input Current		300		nA/V	
Analog VIN Input Current Drift		±50		pA/V/°C	
Power Supply Rejection		80		dB	Internal reference, $V_{IN} = V_{REF}/2$
Power Supply Rejection		90		dB	External reference, $V_{IN} = V_{REF}/2$
Normal Mode Rejection		75		dB	50 Hz ± 1%, conversion time = 122.1 ms
		50		dB	60 Hz ± 1%, conversion time = 122.1 ms
Common-Mode Rejection		95		dB	V_{IN} = 1 V
INTERNAL VOLTAGE REFERENCE					
Voltage	1.169	1.17	1.171	V	T_A = 25°C
Drift vs. Temperature		5		ppm/°C	
EXTERNAL VOLTAGE REFERENCE INPUT					
Differential REFIN Voltage[2]	0.1	2.5	V_{DD}	V	
Absolute REFIN Voltage[2]	GND − 0.03		V_{DD} + 0.03	V	
Average REFIN Input Current		400		nA/V	
Average REFIN Input Current Drift		±50		pA/V/°C	
Common-Mode Rejection		80		dB	
SERIAL INTERFACE LOGIC INPUTS (SCL, SDA)					
V_{IH} Input High Voltage	2.1			V	
V_{IL} Input Low Voltage			0.8	V	
Hysteresis		150		mV	
Input Leakage Current (SCL)		±0.1	±1	µA	
OPEN-DRAIN OUTPUT (SDA)					
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = −6.0 mA
I_{OH} Output High Leakage Current		0.1	1	µA	$V_{OUT} = V_{DD}$
LOGIC OUTPUT ($\overline{RDY}$)					
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = 1.6 mA, V_{DD} = 5 V
V_{OH} Output High Voltage	4.0			V	I_{SOURCE} = 200 µA, V_{DD} = 5 V
V_{OL} Output Low Voltage			0.4	V	I_{SINK} = 100 µA, V_{DD} = 3 V
V_{OH} Output High Voltage	V_{DD} − 0.6			V	I_{SOURCE} = 100 µA, V_{DD} = 3 V
POWER REQUIREMENTS					
V_{DD}-to-GND Voltage	4.75		5.25	V	V_{DD} = 5 V, nominal
	2.7		3.6	V	V_{DD} = 3.3 V, nominal
I_{DD} Current		1	TBD	mA	Digital inputs equal to V_{DD} or GND
		TBD		mA	V_{DD} = 5 V
		TBD		mA	V_{DD} = 3.3 V
I_{DD} Current Power-Down Mode			TBD	µA	Digital inputs equal to V_{DD} or GND

[1] Capacitance units: 1 pF = 10^{-12} F; 1 fF = 10^{-15} F; 1 aF = 10^{-18} F.
[2] Specification is not production tested, but is supported by characterization data at initial product release.
[3] Factory calibrated. The absolute error includes factory gain calibration error, integral nonlinearity error, and offset error after system offset calibration, all at 25°C. At different temperatures, compensation for gain drift over temperature is required.
[4] The capacitive input offset can be eliminated using a system offset calibration. The accuracy of the system offset calibration is limited by the offset calibration register LSB size (32 aF) or by converter + system p-p noise during the system capacitive offset calibration, whichever is greater. To minimize the effect of the converter + system noise, longer conversion times should be used for system capacitive offset calibration. The system capacitance offset calibration range is ±1 pF, the larger offset can be removed using CAPDACs.
[5] The gain error is factory calibrated at 25°C. At different temperatures, compensation for gain drift over temperature is required.
[6] The CAPDAC resolution is six bits in the actual CAPDAC full range. Using the on-chip offset calibration or adjusting the capacitive offset calibration register can further reduce the CIN offset or the unchanging CIN component.
[7] The VTCHOP bit in the VT SETUP register must be set to 1 for the specified temperature sensor and voltage input performance.
[8] Using an external temperature sensing diode 2N3906, with nonideality factor n_f = 1.008, connected as in Figure TBD, with total serial resistance <100 Ω.
[9] Full-scale error applies to both positive and negative full scale.

TIMING SPECIFICATIONS

V_{DD} = 2.7 V to 3.6 V, or 4.75 V to 5.25 V; GND = 0 V; Input Logic 0 = 0 V; Input Logic 1 = V_{DD}; –40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL INTERFACE[1, 2]					See Figure 2
SCL Frequency	0		400	kHz	
SCL High Pulse Width, t_{HIGH}	0.6			µs	
SCL Low Pulse Width, t_{LOW}	1.3			µs	
SCL, SDA Rise Time, t_R			0.3	µs	
SCL, SDA Fall Time, t_F			0.3	µs	
Hold Time (Start Condition), $t_{HD;STA}$	0.6			µs	After this period, the first clock is generated
Set-Up Time (Start Condition), $t_{SU;STA}$	0.6			µs	Relevant for repeated start condition
Data Set-Up Time, $t_{SU;DAT}$	0.1			µs	
Set-Up Time (Stop Condition), $t_{SU;STO}$	0.6			µs	
Data Hold Time, $t_{HD;DAT}$ (Master)	0			µs	
Bus-Free Time (Between Stop and Start Condition, t_{BUF})	1.3			µs	

[1] Sample tested during initial release to ensure compliance.
[2] All input signals are specified with input rise/fall times = 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Output load = 10 pF.

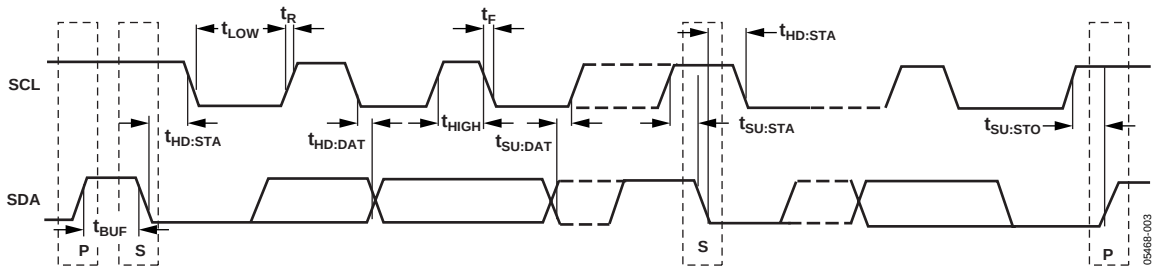

Figure 2. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Positive Supply Voltage V_{DD} to GND	–0.3 V to +6.5 V
Voltage on any Input or Output Pin to GND	–0.3 V to V_{DD} + 0.3 V
ESD Rating (ESD Association Human Body Model, S5.1)	TBD V
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
TSSOP Package θ_{JA}, (Thermal Impedance-to-Air)	128°C/W
TSSOP Package θ_{JC}, (Thermal Impedance-to-Case)	14°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	TBD°C
Infrared (15 sec)	TBD°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

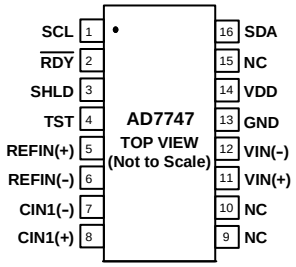

Figure 3. AD7747 Pin Configuration (16-Lead TSSOP)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCL	Serial Interface Clock Input. Connects to the master clock line. Requires pull-up resistor if not already provided in the system.
2	$\overline{\text{RDY}}$	Logic Output. A falling edge on this output indicates that a conversion on enabled channel(s) has been finished and the new data is available. Alternatively, the status register can be read via the 2-wire serial interface and the relevant bit(s) decoded to query the finished conversion. If not used, this pin should be left as an open circuit.
3	SHLD	Capacitive input active AC shielding. To eliminate the CIN parasitic capacitance to ground, the SHLD signal can be used to for shielding the connection between the sensor and CIN. See the max allowed capacitance. If not used, this pin should be left as an open circuit.
4	TST	This pin must be left as an open circuit for proper operation.
5, 6	REFIN(+), REFIN(–)	Differential Voltage Reference Input for the Voltage Channel (ADC). Alternatively, the on-chip internal reference can be used for the voltage channel. These reference input pins are not used for conversion on capacitive channel(s) (CDC). If not used, these pins can be left as an open circuit or connected to GND.
7	CIN1(–)	CDC Negative Capacitive Input in Differential Mode. This pin is internally disconnected in single-ended CDC configuration. If not used, this pin should be left as an open circuit.
8	CIN1(+)	CDC capacitive input (in single ended mode) or positive capacitive input (in differential mode). The measured capacitance is connected between one of the CIN pins and GND. If not used, this pin should be left as an open circuit.
9, 10	NC	Not Connected. These pins should be left as an open circuit.
11, 12	VIN(+), VIN(–)	Differential Voltage Input for the Voltage Channel (ADC). These pins are also used to connect an external temperature sensing diode. If not used, these pins can be left as an open circuit or connected to GND.
13	GND	Ground Pin.
14	VDD	Power Supply Voltage. This pin should be decoupled to GND, using a low impedance capacitor, for example in combination with a 10 µF tantalum and a 0.1 µF multilayer ceramic.
15	NC	Not Connected. This pin should be left as an open circuit.
16	SDA	Serial Interface Bidirectional Data. Connects to the master data line. Requires a pull-up resistor if not provided elsewhere in the system.

TYPICAL PERFORMANCE CHARACTERISTICS

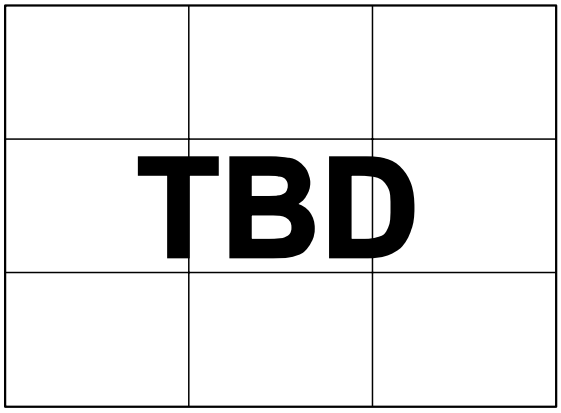

Figure 4.

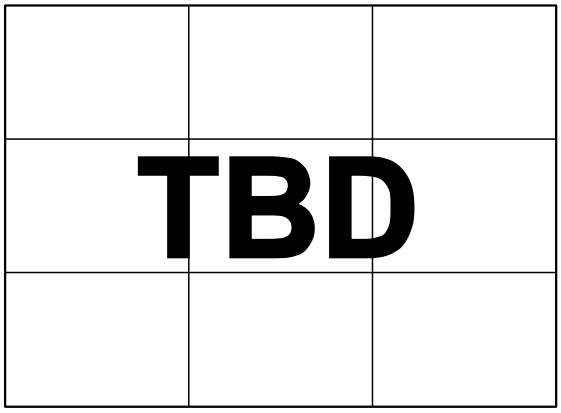

Figure 7.

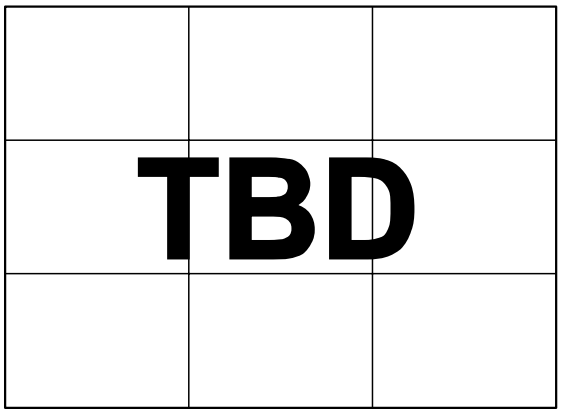

Figure 5.

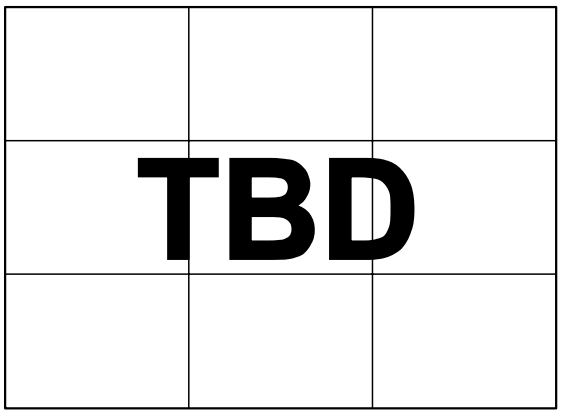

Figure 8.

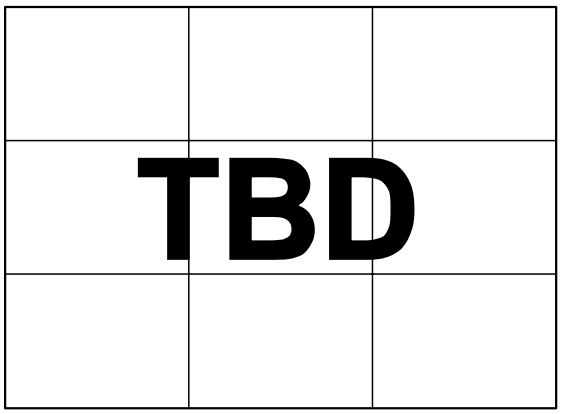

Figure 6.

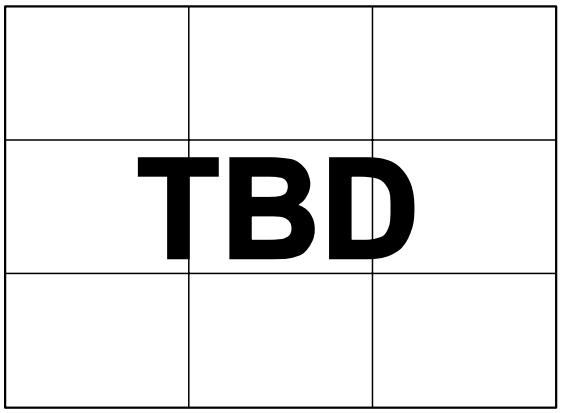

Figure 9.

OUTPUT NOISE AND RESOLUTION SPECIFICATIONS

The AD7747 resolution is limited by noise. The noise performance varies with the selected conversion time.

Table 5 shows typical noise performance and resolution for the capacitive channel. These numbers were generated from 1000 data samples acquired in continuous conversion mode, at an excitation of 16 kHz, $\pm V_{DD}/2$, and with all CIN and EXC pins connected only to the evaluation board (no external capacitors.)

Table 6 and Table 7 show typical noise performance and resolution for the voltage channel. These numbers were generated from 1000 data samples acquired in continuous conversion mode with VIN pins shorted to ground.

RMS noise represents the standard deviation and p-p noise represents the difference between minimum and maximum results in the data. Effective resolution is calculated from rms noise, and p-p resolution is calculated from p-p noise.

Table 5. Typical Capacitive Input Noise and Resolution vs. Conversion Time

Conversion Time (ms)	Output Data Rate (Hz)	–3dB Frequency (Hz)	RMS Noise (aF/√Hz)	RMS Noise (aF)	P-P Noise (aF)	Effective Resolution (Bits)	P-P Resolution (Bits)
22.0	45.5						
23.9	41.9	TBD	TBD	TBD	TBD	TBD	TBD
40.0	25.0						
76.0	13.2						
124.0	8.1	6.9	15	40	250	18.5	16.0
154.0	6.5						
184.0	5.4						
219.3	4.6						

Table 6. Typical Voltage Input Noise and Resolution vs. Conversion Time, Internal Voltage Reference

Conversion Time (ms)	Output Data Rate (Hz)	–3dB Frequency (Hz)	RMS Noise (µV)	P-P Noise (µV)	Effective Resolution (Bits)	P-P Resolution (Bits)
20.1	49.8	26.4	11.4	62	17.6	15.2
32.1	31.2	15.9	7.1	42	18.3	15.7
62.1	16.1	8.0	4.0	28	19.1	16.3
122.1	8.2	4.0	3.0	20	19.5	16.8

Table 7. Typical Voltage Input Noise and Resolution vs. Conversion Time, External 2.5 V Voltage Reference

Conversion Time (ms)	Output Data Rate (Hz)	–3dB Frequency (Hz)	RMS Noise (µV)	P-P Noise (µV)	Effective Resolution (Bits)	P-P Resolution (Bits)
20.1	49.8	26.4	14.9	95	18.3	15.6
32.1	31.2	15.9	6.3	42	19.6	16.8
62.1	16.1	8.0	3.3	22	20.5	17.7
122.1	8.2	4.0	2.1	15	21.1	18.3

SERIAL INTERFACE

The AD7747 supports an I²C-compatible 2-wire serial interface. The two wires on the I²C bus are called SCL (clock) and SDA (data). These two wires carry all addressing, control, and data information one bit at a time over the bus to all connected peripheral devices. The SDA wire carries the data, while the SCL wire synchronizes the sender and receiver during the data transfer. I²C devices are classified as either master or slave devices. A device that initiates a data transfer message is called a master, while a device that responds to this message is called a slave.

To control the AD7747 device on the bus, the following protocol must be followed. First, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that the start byte follows. This 8-bit start byte is made up of a 7-bit address plus an R/W bit indicator.

All peripherals connected to the bus respond to the start condition and shift in the next 8 bits (7-bit address + R/W bit). The bits arrive MSB first. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as the acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. An exception to this is the general call address, which is described later in this document. The idle condition is where the device monitors the SDA and SCL lines waiting for the start condition and the correct address byte. The R/W bit determines the direction of the data transfer. A Logic 0 LSB in the start byte means that the master writes information to the addressed peripheral. In this case the AD7747 becomes a slave receiver. A Logic 1 LSB in the start byte means that the master reads information from the addressed peri-pheral. In this case, the AD7747 becomes a slave transmitter. In all instances, the AD7747 acts as a standard slave device on the I²C bus.

The start byte address for the AD7747 is 0x90 for a write and 0x91 for a read.

READ OPERATION

When a read is selected in the start byte, the register that is currently addressed by the address pointer is transmitted on to the SDA line by the AD7747. This is then clocked out by the master device and the AD7747 awaits an acknowledge from the master.

If an acknowledge is received from the master, the address auto-incrementer automatically increments the address pointer register and outputs the next addressed register content on to the SDA line for transmission to the master. If no acknowledge is received, the AD7747 returns to the idle state and the address pointer is not incremented.

The address pointers' auto-incrementer allow block data to be written or read from the starting address and subsequent incremental addresses.

In continuous conversion mode, the address pointers' auto-incrementer should be used for reading a conversion result. That means, the three data bytes should be read using one multibyte read transaction rather than three separate single byte transactions. The single byte data read transaction may result in the data bytes from two different results being mixed. The same applies for six data bytes if both the capacitive and the voltage/temperature channel are enabled.

The user can also access any unique register (address) on a one-to-one basis without having to update all the registers. The address pointer register contents cannot be read.

If an incorrect address pointer location is accessed or, if the user allows the auto-incrementer to exceed the required register address, the following applies:

- In read mode, the AD7747 continues to output various internal register contents until the master device issues a no acknowledge, start, or stop condition. The address pointers' auto-incrementer's contents are reset to point to the status register at Address 0x00 when a stop condition is received at the end of a read operation. This allows the status register to be read (polled) continually without having to constantly write to the address pointer.
- In write mode, the data for the invalid address is not loaded into the AD7747 registers but an acknowledge is issued by the AD7747.

WRITE OPERATION

When a write is selected, the byte following the start byte is always the register address pointer (subaddress) byte, which points to one of the internal registers on the AD7747. The address pointer byte is automatically loaded into the address pointer register and acknowledged by the AD7747. After the address pointer byte acknowledge, a stop condition, a repeated start condition, or another data byte can follow from the master.

A stop condition is defined by a low-to-high transition on SDA while SCL remains high. If a stop condition is ever encountered by the AD7747, it returns to its idle condition and the address pointer is reset to Address 0x00.

If a data byte is transmitted after the register address pointer byte, the AD7747 loads this byte into the register that is currently addressed by the address pointer register, send an acknowledge, and the address pointer auto-incrementer automatically increments the address pointer register to the next

internal register address. Thus, subsequent transmitted data bytes are loaded into sequentially incremented addresses.

If a repeated start condition is encountered after the address pointer byte, all peripherals connected to the bus respond exactly as outlined above for a start condition, that is, a repeated start condition is treated the same as a start condition. When a master device issues a stop condition, it relinquishes control of the bus, allowing another master device to take control of the bus. Hence, a master wanting to retain control of the bus issues successive start conditions known as repeated start conditions.

AD7747 RESET

To reset the AD7747 without having to reset the entire I²C bus, an explicit reset command is provided. This uses a particular address pointer word as a command word to reset the part and upload all default settings. The AD7747 does not respond to the I²C bus commands (do not acknowledge) during the default values upload for approximately 150 µs (max 200 µs).

The reset command address word is 0xBF.

GENERAL CALL

When a master issues a slave address consisting of seven 0s with the eighth bit (R/W bit) set to 0, this is known as the general call address. The general call address is for addressing every device connected to the I²C bus. The AD7747 acknowledges this address and read in the following data byte.

If the second byte is 0x06, the AD7747 is reset, completely uploading all default values. The AD7747 does not respond to the I²C bus commands (do not acknowledge) during the default values upload for approximately 150 µs (max 200 µs).

The AD7747 does not acknowledge any other general call commands.

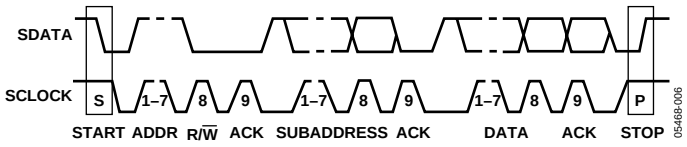

Figure 10. Bus Data Transfer

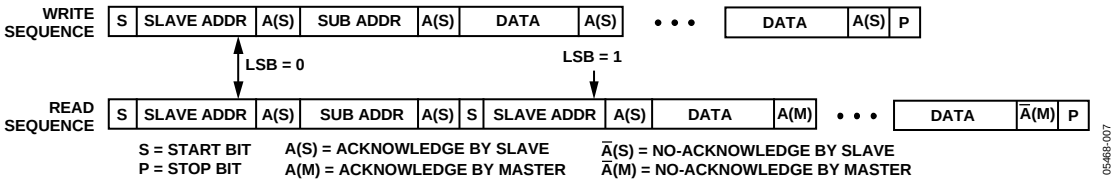

Figure 11. Write and Read Sequences

REGISTER DESCRIPTIONS

The master can write to or read from all of the AD7747 registers except the address pointer register, which is a write-only register. The address pointer register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the address pointer register. After the part has been accessed over the bus and a read/write operation is selected, the address pointer register is set up. The address pointer register determines from or to which register the operation takes place. A read/write operation is performed from/to the target address, which then increments to the next address until a stop command on the bus is performed.

Table 8. Register Summary

	Address Pointer			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Register	**(Dec)**	**(Hex)**	**Dir**	**Default Value**							
Status	0	0x00	R	-	-	-	-	-	RDY	RDYVT	RDYCAP
				0	0	0	0	0	1	1	1
Cap Data H	1	0x01	R	Capacitive channel data—high byte, 0x00							
Cap Data M	2	0x02	R	Capacitive channel data—middle byte, 0x00							
Cap Data L	3	0x03	R	Capacitive channel data—low byte, 0x00							
VT Data H	4	0x04	R	Voltage/temperature channel data—high byte, 0x00							
VT Data M	5	0x05	R	Voltage/temperature channel data—middle byte, 0x00							
VT Data L	6	0x06	R	Voltage/temperature channel data—low byte, 0x00							
Cap Setup	7	0x07	R/W	CAPEN	-	CAPDIFF	-	-	-	-	-
				0	0	0	0	0	0	0	0
VT Setup	8	0x08	R/W	VTEN	VTMD1	VTMD0	EXTREF	-	-	VTSHORT	VTCHOP
				0	0	0	0	0	0	0	0
EXC Setup	9	0x09	R/W	-	-	-	-	EXCDAC	EXCEN	EXCLVL1	EXCLVL0
				0	0	0	0	0	0	1	1
Configuration	10	0x0A	R/W	VTFS1	VTFS0	CAPFS2	CAPFS1	CAPFS0	MD2	MD1	MD0
				1	0	1	0	0	0	0	0
Cap DAC A	11	0x0B	R/W	DACAENA	-	DACA—6-Bit Value					
				0	0	0x00					
Cap DAC B	12	0x0C	R/W	DACBENB	-	DACB—6-Bit Value					
				0	0	0x00					
Cap Offset H	13	0x0D	R/W	Capacitive offset calibration—high byte, 0x80							
Cap Offset L	14	0x0E	R/W	Capacitive offset calibration—low byte, 0x00							
Cap Gain H	15	0x0F	R/W	Capacitive gain calibration—high byte, factory calibrated							
Cap Gain L	16	0x10	R/W	Capacitive gain calibration—low byte, factory calibrated							
Volt Gain H	17	0x11	R/W	Voltage gain calibration—high byte, factory calibrated							
Volt Gain L	18	0x12	R/W	Voltage gain calibration—low byte, factory calibrated							

STATUS REGISTER

Address Pointer 0x00, Read Only, Default Value 0x07

This register indicates the status of the converter. The status register can be read via the 2-wire serial interface to query a finished conversion.

The $\overline{RDY}$ pin reflects the status of the RDY bit. Therefore, the $\overline{RDY}$ pin high-to-low transition can be used as an alternative indication of the finished conversion.

Table 9. Status Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	-	-	-	-	-	RDY	RDYVT	RDYCAP
Default	0	0	0	0	0	1	1	1

Table 10.

Bit	Mnemonic	Description
7-3	-	Not used, always read 0.
2	RDY	RDY = 0 indicates that conversion on the enabled channel(s) has been finished and new unread data is available. If both capacitive and voltage/temperature channels are enabled, the RDY bit is changed to 0 after conversion on both channels is finished. The RDY bit returns to 1 either when data is read or prior to finishing the next conversion. If, for example, only the capacitive channel is enabled, then the RDY bit reflects the RDYCAP bit.
1	RDYVT	RDYVT = 0 indicates that a conversion on the voltage/temperature channel has been finished and new unread data is available.
0	RDYCAP	RDYCAP = 0 indicates that a conversion on the capacitive channel has been finished and new unread data is available.

CAP DATA REGISTER

24 Bits, Address Pointer 0x01, 0x02, 0x03, Read-Only, Default Value 0x000000

Capacitive channel output data. The register is updated after finished conversion on the capacitive channel, with one exception: When the serial interface read operation from the CAP DATA register is in progress, the data register is not updated and the new capacitance conversion result is lost.

The stop condition on the serial interface is considered to be the end of the read operation. Therefore, to prevent data corruption, all three bytes of the data register should be read sequentially using the register address pointer auto-increment feature of the serial interface.

To prevent losing some of the results, the CAP DATA register should be read before the next conversion on the capacitive channel is finished.

The 0x000000 code represents negative full scale (–8.192 pF), the 0x800000 code represents zero scale (0 pF), and the 0xFFFFFF code represents positive full scale (+8.192 pF).

VT DATA REGISTER

24 Bits, Address Pointer 0x04, 0x05, 0x06, Read-Only, Default Value 0x000000

Voltage/temperature channel output data. The register is updated after finished conversion on the voltage channel or temperature channel, with one exception: When the serial interface read operation from the VT DATA register is in progress, the data register is not updated and the new voltage/temperature conversion result is lost.

The stop condition on the serial interface is considered to be the end of the read operation. Therefore, to prevent data corruption, all three bytes of the data register should be read sequentially using the register address pointer auto-increment feature of the serial interface.

For voltage input, Code 0 represents negative full scale ($-V_{REF}$), the 0x800000 code represents zero scale (0 V), and the 0xFFFFFF code represents positive full scale ($+V_{REF}$).

To prevent losing some of the results, the VT DATA register should be read before the next conversion on the voltage/temperature channel is finished.

For the temperature sensor, the temperature can be calculated from code using the following equation:

$$Temperature\ (°C) = (Code/2048) - 4096$$

CAP SET-UP REGISTER

Address Pointer 0x07, Default Value 0x00

Capacitive channel setup.

Table 11. CAP Set-Up Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	CAPEN	-	CAPDIFF	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

Table 12.

Bit	Mnemonic	Description
7	CAPEN	CAPEN = 1 enables capacitive channel for single conversion, continuous conversion, or calibration.
6	-	This bit must be 0 for proper operation.
5	CAPDIFF	DIFF = 1 sets differential mode on the selected capacitive input.
4-0	-	These bits must be 0 for proper operation.

VT SET-UP REGISTER

Address Pointer 0x08, Default Value 0x00

Voltage/Temperature channel setup.

Table 13. VT Set-Up Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	VTEN	VTMD1	VTMD0	EXTREF	-	-	VTSHORT	VTCHOP
Default	0	0	0	0	0	0	0	0

Table 14.

<table>
<tr><th>Bit</th><th>Mnemonic</th><th colspan="3">Description</th></tr>
<tr><td>7</td><td>VTEN</td><td colspan="3">VTEN = 1 enables voltage/temperature channel for single conversion, continuous conversion, or calibration.</td></tr>
<tr><td>6
5</td><td>VTMD1
VTMD0</td><td colspan="3">Voltage/temperature channel input configuration.</td></tr>
<tr><td></td><td></td><td>VTMD1</td><td>VTMD0</td><td>Channel Input</td></tr>
<tr><td></td><td></td><td>0</td><td>0</td><td>Internal temperature sensor</td></tr>
<tr><td></td><td></td><td>0</td><td>1</td><td>External temperature sensor diode</td></tr>
<tr><td></td><td></td><td>1</td><td>0</td><td>V_{DD} monitor</td></tr>
<tr><td></td><td></td><td>1</td><td>1</td><td>External voltage input (VIN)</td></tr>
<tr><td>4</td><td>EXTREF</td><td colspan="3">EXTREF = 1 selects an external reference voltage connected to REFIN(+), REFIN(–) for the voltage input or the V_{DD} monitor.
EXTREF = 0 selects the on-chip internal reference. The internal reference must be used with the internal temperature sensor for proper operation.</td></tr>
<tr><td>3-2</td><td>-</td><td colspan="3">These bits must be 0 for proper operation.</td></tr>
<tr><td>1</td><td>VTSHORT</td><td colspan="3">VTSHORT = 1 internally shorts the voltage/temperature channel input for test purposes.</td></tr>
<tr><td>0</td><td>VTCHOP = 1</td><td colspan="3">VTCHOP = 1 sets internal chopping on the voltage/temperature channel.
The VTCHOP bit must be set to 1 for the specified voltage/temperature channel performance.</td></tr>
</table>

EXC SET-UP REGISTER

Address Pointer 0x09, Default Value 0x03

Capacitive channel excitation setup.

Table 15. EXC Set-Up Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	-	-	-	-	EXCDAC	EXCEN	EXCLVL1	EXCLVL0
Default	0	0	0	0	0	0	1	1

Table 16.

Bit	Mnemonic	Description				
7-4	-	These bits must be 0 for proper operation.				
3	EXCDAC	CAPDAC excitation. This bit must be set to 1 for the proper capacitive channel operation				
2	EXCEN	CIN and AC SHLD excitation. This bit must be set to 1 for the proper capacitive channel operation				
1 0	EXCLVL1, EXCLVL0	Excitation Voltage Level.				
		EXCLVL1	**EXCLVL0**	**Voltage on Cap**	**EXC Pin Low Level**	**EXC Pin High Level**
		0	0	$\pm V_{DD}/8$	$V_{DD} \times 3/8$	$V_{DD} \times 5/8$
		0	1	$\pm V_{DD}/4$	$V_{DD} \times 1/4$	$V_{DD} \times 3/4$
		1	0	$\pm V_{DD} \times 3/8$	$V_{DD} \times 1/8$	$V_{DD} \times 7/8$
		1	1	$\pm V_{DD}/2$	0	V_{DD}

CONFIGURATION REGISTER

Address Pointer 0x0A, Default Value 0xA0

Converter update rate and mode of operation setup.

Table 17. Configuration Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	VTF1	VTF0	CAPF2	CAPF1	CAPF0	MD2	MD1	MD0
Default	0	0	0	0	0	0	0	0

Table 18.

Bit	Mnemonic	Description
7 6	VTF1 VTF0	Voltage/temperature channel digital filter setup—conversion time/update rate setup.

VTF1	VTF0	VTCHOP = 1 Conversion Time (ms)	Update Rate (Hz)	–3 dB Frequency (Hz)
0	0	20.1	49.8	26.4
0	1	32.1	31.2	15.9
1	0	62.1	16.1	8.0
1	1	122.1	8.2	4.0

5 4 3	CAPF2 CAPF1 CAPF0	Capacitive channel digital filter setup—conversion time/update rate setup.

CAPF2	CAPF1	CAPF0	CAP CHOP = 0 Conversion Time (ms)	Update Rate	–3 dB Frequency (Hz)
0	0	0	22.0	45.5	
0	0	1	23.9	41.9	
0	1	0	40.0	25.0	
0	1	1	76.0	13.2	
1	0	0	124.0	8.1	
1	0	1	154.0	6.5	
1	1	0	184.0	5.5	
1	1	1	219.3	4.6	

2 1 0	MD2 MD1 MD0	Converter mode of operation setup.

MD2	MD1	MD0	Mode
0	0	0	Idle
0	0	1	Continuous conversion
0	1	0	Single conversion
0	1	1	Power-Down
1	0	0	-
1	0	1	Capacitance system offset calibration
1	1	0	Capacitance or voltage system gain calibration
1	1	1	

CAP DAC A REGISTER

Address Pointer 0x0B, Default Value 0x00

Capacitive DAC setup.

Table 19. Cap DAC A Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	DACAENA	-	DACA—6-Bit Value					
Default	0	0	0x00					

Table 20.

Bit	Mnemonic	Description
7	DACAENA	DACAENA = 1 connects capacitive DACA to the positive capacitance input.
6	-	This bit must be 0 for proper operation.
5-1	DACA	DACA value, Code 0x00 ≈ 0 pF, Code 0x3F ≈ full range.

CAP DAC B REGISTER

Address Pointer 0x0C, Default Value 0x00

Capacitive DAC setup.

Table 21. Cap DAC B Register Bit Map

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	DACAENB	-	DACB—6-Bit Value					
Default	0	0	0x00					

Table 22.

Bit	Mnemonic	Description
7	DACBENB	DACBENB = 1 connects capacitive DACB to the negative capacitance input.
6	-	This bit must be 0 for proper operation.
5-1	DACB	DACB value, Code 0x00 ≈ 0 pF, Code 0x3F ≈ full range.

CAP OFFSET CALIBRATION REGISTER

16 Bits, Address Pointer 0x0D, 0x0E, Default Value 0x8000

The capacitive offset calibration register holds the capacitive channel zero-scale calibration coefficient. The coefficient is used to digitally remove the capacitive channel offset. The register value is updated automatically following the execution of a capacitance offset calibration. The capacitive offset calibration resolution (cap offset register LSB) is less than TBD aF; the full range is TBD pF.

CAP GAIN CALIBRATION REGISTER

16 Bits, Address Pointer 0x0F, 0x10, Default Value 0xXXXX

Capacitive gain calibration register. The register holds the capacitive channel full-scale factory calibration coefficient.

VOLT GAIN CALIBRATION REGISTER

16 Bits, Address Pointer 0x11,0x12, Default Value 0xXXXX

Voltage gain calibration register. The register holds the voltage channel full-scale factory calibration coefficient.

CIRCUIT DESCRIPTION

ACTIVE AC SHIELD CONCEPT

The AD7747 measures capacitance between CIN and ground. That means any capacitance to ground on signal path between AD7747 CIN pin(s) and sensor is included in the AD7747 conversion result.

The parasitic capacitance of the sensor connections can easily be in the same, if not even higher order than the capacitance of the sensor itself. If that parasitic capacitance is stable, it can be treated as a non-changing capacitive offset. However, the parasitic capacitance of sensor connections is often changing as result of mechanical movement, changing ambient temperature, ambient humidity, etc. These changes would be seen as drift in the conversion result and may significantly compromise the system accuracy.

To eliminate the CIN parasitic capacitance to ground, the AD7747 SHLD signal can be used for shielding the connection between the sensor and CIN. The SHLD output is basically the same signal waveform as the excitation of the CIN pin, the SHLD is driven to the same voltage potential as the CIN pin. Therefore, there is no AC current between CIN and SHLD pins and any capacitance between these pins doesn't get involved in the CIN charge transfer. Ideally, the CIN to SHLD capacitance doesn't have any contribution to the AD7747 result.

To get the best result, locate the AD7747 as close as possible to the capacitive sensor. Keep the connection between the sensor and AD7747 CIN pin and also the return path between sensor ground and the AD7747 GND pin short. Shield the PCB track to CIN pin and connect the shielding to the AD7747 SHLD pin. Also, if a shielded cable is used for sensor connection, the shield should be connected to the AD7747 SHLD pin.

TYPICAL APPLICATION DIAGRAM

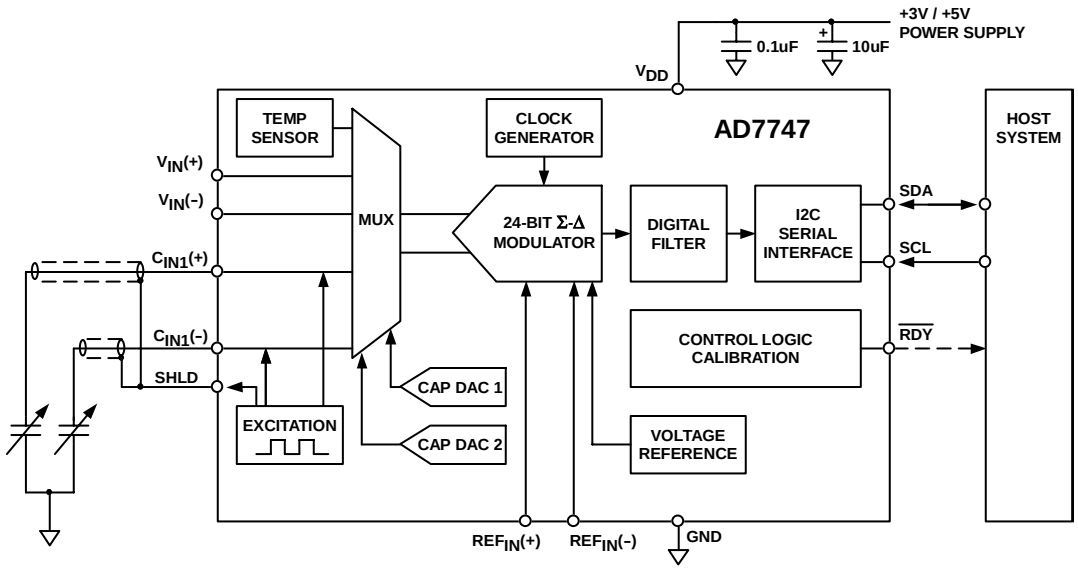

Figure 12. Basic Application Diagram for a Differential Capacitive Sensor

OUTLINE DIMENSIONS

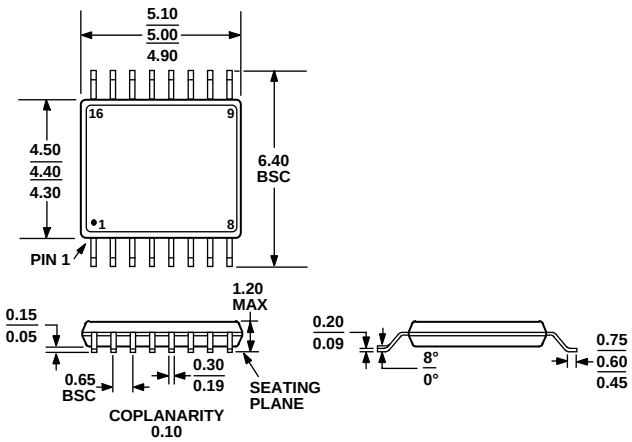

Figure 13. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

NOTES