ES51973
4 1/2 A/D

Features

- 22000 counts, adjustable
- Input signal full scale = 220 mV (sensitivity = 10 uV/count)
- Conversion rate selectable
- On chip buzzer driving, frequency selectable
- Low battery detection
- Zero calibration for eliminating offset error
- Using 5V or 3V microprocessor
- I/O port with microprocessor (3 pins)
- Two formats for data acquisition
- single 5V or 6V DC power supply (V+ to V-)
- 28 pin SOP package

General Description

The ES51973 is a 22000 counts dual-slope analog-to-digital converter (ADC). The conversion rate, buzzer frequency and resolution can be selected or decided by an external microprocessor. The conversion rate can vary from 2 times/sec to 100 times/sec under 4 MHz operating clock. The buzzer frequency can be chosen to be audible from 400 KHz to 6 MHz. In addition, other functions for low battery detection, on chip buzzer driving, and I/O port with microprocessor are also provided.

Absolute Maximum Ratings

Characteristic	Rating
Positive Supply Voltage (V+ to AGND)	3.5V
Negative Supply Voltage (V- to AGND)	-3.5V
Analog I/O Voltage	((V-) - 0.5V) to ((V+) + 0.5V)
Digital I/O Voltage	((V-) - 0.5V) to ((V+) + 0.5V)
Power Dissipation	800mW
Operating Temperature	0°C to 70°C
Storage Temperature	-25°C to 125°C
Lead Temperature (soldering, 10sec)	270°C

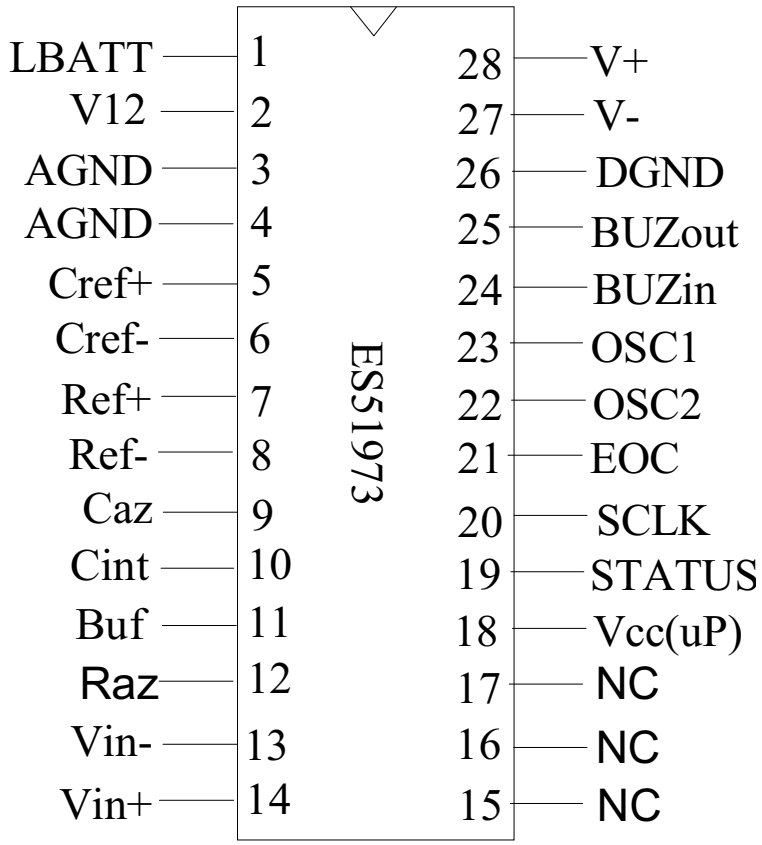
Electrical Characteristics

TA=25°C, DGND=AGND=0V, operating clock = 4 MHz.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V+	Positive Power Supply		2.3	2.5	3.3	V
V-	Negative Power Supply		-2.3	-2.5	-3.3	V
I(V+)	Operation Supply Current	Normal power on (V+ to V-)	-	1.0	1.7	mA
I(GND)	Supply Current of DGND to V-	ΔV between DGND and V- is -0.2V	5	10	-	mA
Zero	Zero Input Reading	1 MΩ input resistor, null to zero by uP.	-0	0	+0	count
NLV1	Nonlinearity	Best case straight line conversion rate = 10 times/s	-0.02	-	0.02	%F.S.
REV1	Rollover Error	1 MΩ input resistor conversion rate = 10 times/s	-0.02	-	0.02	%F.S.
V12	Band Gap Voltage Reference	100 kΩ between V12 and AGND	-1.31	-1.23	-1.10	V
LBATT	Low Battery Detection	LBATT to V12	-60	0	60	mV
	PEAK Hold value accuracy (10us)	使用 10nF 聚乙酯薄膜電容 (polyester, Mylar)	-1.2 -25	-	+1.2 +25	%F.S. ±count
TCRF	Reference Voltage (V12) Temperature Coefficient	100 kΩ between V12 and AGND (0°C to 70°C)	-	50	-	ppm/°C

Pin Configuration

SOP 28pin package:



Pin Description

Pin No.	Symbol	Type	Description
1	LBATT	A, I	Low battery voltage detection.
2	V12	A, O	Reference voltage output.
3	AGND	G	Analog ground, as the voltage reference 0V.
4	AGND	G	Analog ground, as the voltage reference 0V.
5	Cref+	A, I/O	Positive connection for reference capacitor.
6	Cref-	A, I/O	Negative connection for reference capacitor.
7	Ref+	A, I	Differential reference high voltage input.
8	Ref-	A, I	Differential reference low voltage input.
9	Caz	A, O	Auto-zero capacitor connection. (0.47uF)
10	Cint	A, O	Integration capacitor connection. (33nF)
11	Buf	A, O	Integration resistor connection output. (100kΩ)
12	Raz	A, O	Integration resistor connection output. (10kΩ)
13	Vin-	A, I	Analog differential low signal input.
14	Vin+	A, I	Analog differential high signal input.
15	NC		
16	NC		
17	NC		
18	Vcc(uP)	D, I	The high level of digital I/O signals, which is connected to Vcc pin of microprocessor.
19	STATUS	D, I/O	ES51973 sends current status to microprocessor or receives controlled status from microprocessor.
20	SCLK	D, I	Clock input from microprocessor.
21	EOC	D, O	An indicator for integration and de-integration time (format 1) or conversion end (format 2).
22	OSC2	D, O	Crystal oscillator (output) connection.
23	OSC1	D, I	Crystal oscillator (input) connection.
24	BUZin	D, I	Buzzer control input. When connected to DGND, turns the buzzer on. (default state is pull low to V-)
25	BUZout	D, O	Buzzer output. Audio frequency output which drives a piezoelecric buzzer swing between V+ and V-.
26	DGND	G	Digital ground.
27	V-	P	Negative supply voltage, connected to cathode of battery typically.
28	V+	P	Positive supply voltage, V+ to V- is 5.0V typically.

A : Analog , D : Digital , P : Power , G : Ground , I : Input , O : Output

Operation Mode

(1) Operation of ES51973 and the external microprocessor

ES51973 is a microprocessor based data acquisition ADC. ES51973 performs A-to-D conversion and the microprocessor acquires the results via interface pins: SCLK, EOC and STATUS. There are two formats for data acquisition. In format 1, ES51973 raises the logic level of EOC to high during the integration phase (INT) and de-integration phase (DINT). The microprocessor can acquire the conversion result by counting the time period as EOC is high. And the microprocessor can obtain the operation status of ES51973 such as conversion rate, buzzer frequency, sign bit, etc. from pin STATUS. The value of STATUS is read in serial with clock pin, SCLK which is controlled by microprocessor.

In addition to counting the time period of EOC, ES51973 provides another way, the format 2 to obtain the conversion result. In format 2 the conversion result is computed by ES51973 itself and the microprocessor can obtain the output count from pin STATUS.

The decision to choose format 1 or format 2 depends on application. Format 2 is simple for general application. On the other hand, a microprocessor must set up a timer to estimate the duration of EOC in format 1. Thus the maximum count or resolution could be changed by choosing the counting frequency of the timer. For example the maximum counts of ES51973 operating in format 2 with 4 MHz operating clock is 22,000. The same resolution is obtained in format 1 with timer counting period, 2 us/count. A higher resolution, say 44,000 counts, could be achieved by speeding up the counting frequency twice.

In addition to change operation format, ES51973 allow a user to change the conversion rate, buzzer frequency on the fly. Their changing methods will be described in following sections.

(2) Buzzer frequency

ES51973 provides buzzer output at pin BUZin (active high) is used to control whether BUZout should output buzzer wave or not. The default buzzer frequency is 2 KHz with 4 MHz operating frequency (crystal oscillator frequency at pins OSC1 and OSC2).

ES51973 provides eight buzzer frequency selection options and the external micro-processor can choose one frequency that is audible by setting the values of bits, B2, B1 and B0 in the STATUS word used in communication between ES51973 and the external microprocessor. The communication protocol will be described in detail in section (6). The

buzzer frequency is determined by the following formula:

$$fbuz = \frac{fosc1}{40 \times F_1(B2, B1, B0)} \quad (Hz)$$

where, fosc1 : ES51973 operation frequency.
fbuz : the frequency of BUZout.
B2, B1, B0 : provided by external microprocessor.
$F_1(\ .\ )$: the fbuz's ratio factor.

According to the formula, a user can select a favorite buzzer frequency among the audible frequency range. The values of B2, B1 and B0 are 0, 1 and 0 respectively in default. The buzzer frequencies and the ratios determined by B2, B1 and B0 with various operating frequencies are shown in the following table.

B2 B1 B0 (fbuz) / $F_1(\ .\ )$ (fosc1)		6M	4M	2M	1.2M	1M	800k	600k	400k
1 1 1	3	50.00	33.33	16.67	10.00	8.33	6.67	5.00	3.33
1 1 0	5	30.00	20.00	10.00	6.00	5.00	4.00	3.00	2.00
1 0 1	9	16.67	11.11	5.56	3.33	2.78	2.22	1.67	1.11
1 0 0	15	10.00	6.67	3.33	2.00	1.67	1.33	1.00	0.67
0 1 1	30	5.00	3.33	1.67	1.00	0.83	0.67	0.50	0.33
0 1 0	50	3.00	**2.00**	1.00	0.60	0.50	0.40	0.30	0.20
0 0 1	90	1.67	1.11	0.56	0.33	0.28	0.22	0.17	0.11
0 0 0	150	1.00	0.67	0.33	0.20	0.17	0.13	0.10	0.07

Unit : fosc1 : Hz , fbuz : kHz

In this table the data with gray blocks are recommended frequency values. A user thus can easily choose a buzzer frequency based on the table.

(3) Conversion Rate

The ES51973 provided several conversion rates (CRs) that can be selected by external microprocessor. The way to change conversion rate is similar to that of buzzer ferquncy selection and the CRs are follow the below formula:

$$CR = \frac{fosc1 \times F_2(C2, C1, C0)}{4 \times 10^6} \quad (times / \sec)$$

where, fosc1 : ES51973 operation frequency.
CR : conversion rate.
C2, C1, C0 : provided by external microprocessor.
$F_2(\ .\ )$: the CR's ratio factor.

According to the formula, a user can select a conformable and reasonable conversion rate. The values of C2, C1 and C0 are 0, 1 and 1 respectively in default. Thus the default

conversion rate is 10 times/sec with 4 MHz operating frequency. The following table lists the CRs and the ratios determined by C2, C1 and C0 with various operating frequencies. A user can decide the value of C2, C1 and C0 based on operating frequency and CR.

CRs / fosc1 — C2 C1 C0 / $F_2(.)$				6M	4M	2M	1.2M	1M	800k	600k	400k
1	1	1	100	150	100	50	30	25	20	15	10*
1	1	0	80	120	80	40	24	20	16	12!	8
1	0	1	40	60	40	20	12!	10*	8	6!	4
1	0	0	20	30	20	10*	6!	5*	4!	3!	2!*
0	**1**	**1**	10	15	**10***	5*	3!	2.5*	2!*	1.5!	1!*
0	1	0	8	12!	8	4!	2.4!	2!*	1.6	1.2!	0.8!
0	0	1	4	6!	4!	2!*	1.2!	1!*	0.8!	0.6!	0.4!*
0	0	0	2	3!	2!*	1!*	0.6!	0.5!*	0.4!*	0.3!	0.2!*

Unit : fosc1 : Hz , CR : times/sec

Note: 1. The default status of C2, C1, C0 is (0, 1, 1) and the default conversion rate is 10 times/buzzer if fosc1 = 4.0 MHz.
2. About the index at the back of CR's numbers:
(1) " * " is that rejected with 50 Hz.
(2) " ! " is that rejected with 60 Hz.

(4) Dual Slope A/D—four phases timing

ES51973 is a dual-slope analog-to-digital converter (ADC). Figure 1 is a structure of dual-slope integrator. Its measurement cycle has two distinct phases: input signal integration (INT) phase and reference voltage integration (DINT) phase.

In INT phase, the input signal is integrated for a fixed time period, then A/D enters DINT phase in which an opposite polarity constant reference voltage is integrated until the integrator output voltage becomes to zero. Since both the time period for input signal integration and the amount of reference voltage are fixed, thus the de-integration time is proportional to the input signal. Hence, we can define the mathematical equation about input signal, reference voltage integration (see Figure 1.):

$$\frac{1}{Buf \times C\,\text{int}} \int_0^{T_{INT}} V_{IN}(t)dt = \frac{1}{Buf \times C\,\text{int}} \times V_{REF} \times T_{DINT}$$

where, $V_{IN}(t)$ = input signal

V_{REF} = reference voltage

T_{INT} = integration time (fixed)

T_{DINT} = de-integration time (proportional to $V_{IN}(t)$)

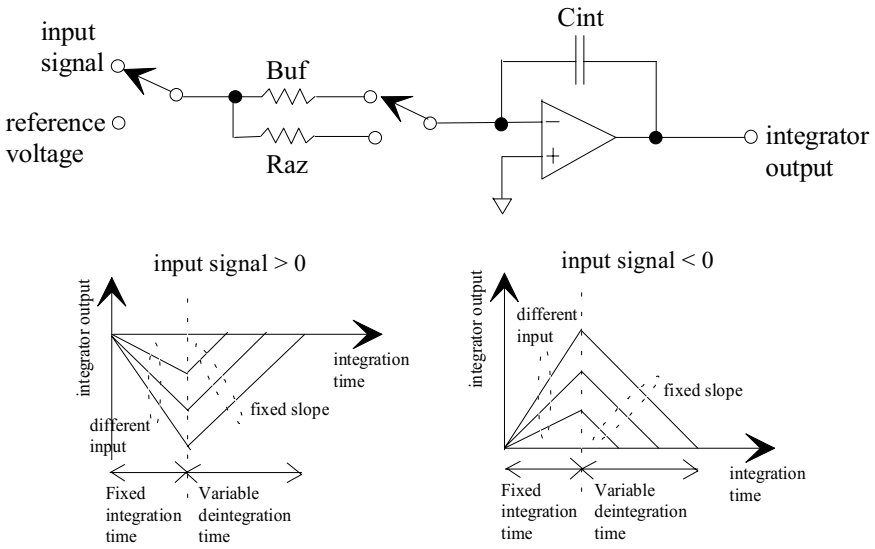


Figure 1. the structure of dual-slope integrator and its output waveform.

If $V_{IN}(t)$ is a constant, we can rewrite above equation:

$$T_{DINT} = \frac{T_{INT}}{V_{REF}} \times V_{IN}$$

Besides the INT phase and DINT phase, ES51973 exploits auto zero (AZ) phase and zero integration (ZI) phase to achieve accurate measurement. In AZ phase, the system offset is stored. The offset error will be eliminated in DINT phase. Thus a higher accuracy could be obtained. In ZI phase, the internal status will be recovered quickly to that of zero input. Thus the succeeding measurements won't be disturbed by current measurement especially in case of overload.

As mentioned above, the measurement cycle of ES51973 contains four phases:

(1) auto zero phase (AZ)

(2) input signal integration phase (INT)

(3) reference voltage integration phase (DINT)

(4) zero integration phase (ZI)

The time ratios of these four phases, AZ, INT, DINT and ZI to the entire measurement cycle are 20%, 20%, 44% and 16% respectively. However the actual duration of each phase depends on conversion rate. Some examples are shown in the table below. A user can easily deduce other cases based on the table.

Voltage:

CR (times/sec)	ZI (ms)	AZ (ms)	INT (ms)	DINT (ms)
5	32	40	40	88
10	**16**	**20**	**20**	**44**
12	13.33	16.67	16.67	36.67
20	8	10	10	22

Note: Vref = -100 mV.

(5) Component Value Selection for ADC

For various application requirements on conversion rate and input full range, we suggest nominal values for external components of ADC in Figure 1 to obtain better performance. Under default condition with operating clock = 4 MHz:

(1) conversion rate = 10 times/sec

(2) reference voltage = -100 mV

(3) input signal full scale = 220 mV (sensitivity = 10 uV)

we suggest that Cint = 33 nF, Buf = 100 kΩ, Raz = 10 kΩ.

If a user selects a different conversion rate rather than default, the integration capacitor Cint value must be changed according to the following rule for better performance:

Cint × (conversion rate) = (33 nF) × (10 times/sec).

It is important that the actual Cint value should be no less than the nominal value. A smaller Cint reduces the input full range. However a larger Cint might have weaker noise immunity than the suggested one.

A user could enlarge the input full range by changing reference voltage (Vref) and the amount of integration resistor (Buf and Raz). For example, if Vref, Buf and Raz are enlarged as twice than the default values then the input full range becomes 440 mV. The input full range can be enlarged up to 1.1 V (5 times than the default case). We list general rules in below which might be helpful in determining component values.

Buf / (reference voltage) = 100 kΩ / (-100 mV)

Raz / (reference voltage) = 10 kΩ / (-100 mV)

(6) Digital Interface between ES51973 and Microprocessor

The pins, EOC, SCLK and STATUS of ES51973 are digital communicating interface between ES51973 and microprocessor. The STATUS is bi-directional, and the others are unilateral: EOC is from ES51973 to microprocessor and SCLK is from microprocessor to ES51973. There are two formats for data acquisition. In format 1, ES51973 raise the logic

level of EOC to high at the duration of INT phase and DINT phase. The duration as EOC is high represents the A-to-D conversion result. As the conversion completes and EOC become logic low, the microprocessor may send 16 clock pulses to pin SCLK and read out the serial data (status) on pin STATUS at the falling edge of the clock pulse. The received status represents the polarity of conversion result and the operation mode of ES51973. The meaning of each bit of the status received from STAUS is shown in the following table. The sending/receiving order is S0, S1, … S15.

S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
TEST	Format	B2	B1	B0	C2	C1	C0	ZERO	NC	NC	NC	LBATT	NC	NC	Sign

Sign : "H" is negative, "L" is positive.

LBATT : low battery detection, "H" is smaller than V12 and "L" is greater than V12 typically. The default is "L".

ZERO : "H" is zero calibration on. The default is "L".

C0~C2 : conversion rate selection. The default is (1, 1, 0).

B0~B2 : buzzer frequency selection. The default is (0, 1, 0).

Format : "L" is format 1, and "H" is format 2. The default is "L".

TEST : "H" is testing mode on. The default is "L".

The communication way between ES51973 and the microprocessor in format 2 is similar to that of format 1. However in format 2, ES51973 provides the A-to-D conversion result by a 16-bits output count instead of the duration of EOC. ES51973 raises the logic level of EOC high at the duration of ZI phase. As the conversion completes and EOC becomes low, the microprocessor sends 32 clock pulses to pin SCLK and read the values of output count and status from STAUS pin at the falling edge of clock pulse. The content of output count is read in order of D0, D1, ... D15 and it is read in front of the status.

Both format 1 and format 2 have two operation mode: mode 1 and mode 2. The communication ways described above are in mode 1 at which ES51973 sends data to the microprocessor. Mode 2 is used in the cases of the microprocessor sends control status to ES51973 to change format, conversion rate, zero calibration, etc. The difference between mode 1 and mode 2 is that there are a start bit and a end bit on the clock sequence for SCLK. As ES51973 detects the start bit it enters mode 2 and receives status from STATUS. ES51973 will go back to mode 1 as it detects the end bit. There are timing restricts on the width of clock pulse, start bit and the end bit. The communication might malfunction if the restrictions are

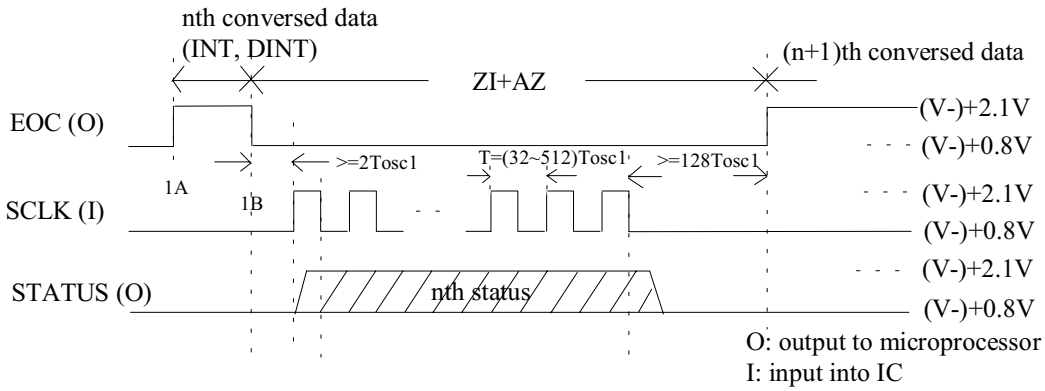
violated.

The communication ways and associated timing restrictions are described in detail as follows.

The EOC, SCLK and STATUS of the ES51973 are used as digital communicating interface between ES51973 and microprocessor. The STATUS is bi-directional interface, and the others are unilateral ones: EOC is from ES51973 to microprocessor and SCLK is from microprocessor to ES51973. There are two formats for using EOC, SCLK and STATUS. The format 1 is used for communications of INT, DINT phases and status, and the another format (format 2) is used for communications of counts (counter from DINT phase) and status.

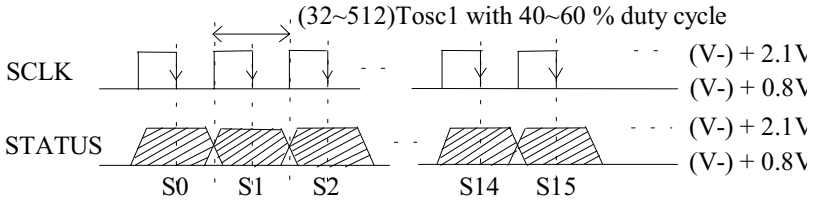
Format 1:

mode 1: ES51973 sends conversed data (INT, DINT) and status to uP.



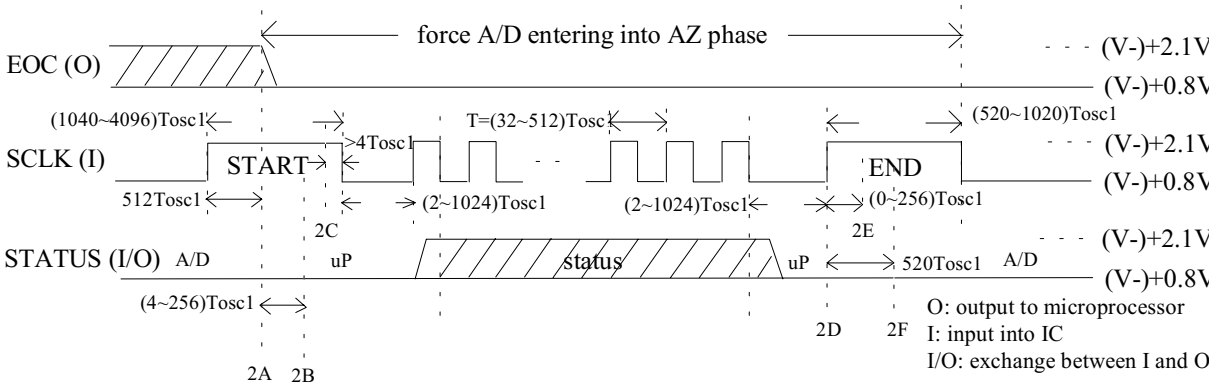
Note: 1. The INT phase begins at 1A, and DINT phase ends at 1B.

2. The microprocessor will sample the status at the falling edge of SCLK and the detail timing between SCLK and STATUS is as follow:



3. There is a strict limitation that the sending of status information must be completed in front of 128Tosc1 of next conversion data at least.
4. When the conversion completes, the INT and DINT phases timings are sent to microprocessor by EOC. And the resolution depends on the clock provided by uP. For example, if the CR is 10 times/sec, the maximum DINT time is 44 ms, and the resolution will be 22000 (11000) counts based on a 500 (250) kHz clock.

mode 2: ES51973 receives controlled status from microprocessor.



Note: 1. The START bit:

After time 2A, the EOC's state is forced to low (V-) and ES51973 enter into AZ phase. And at the same time, STATUS is changed from output pin to input pin with a 3 uA pull low current provided by ES51973 internally. Then microprocessor can send control status to STATUS. It is suggested that microprocessor begins to drive STATUS between 2B and 2C.

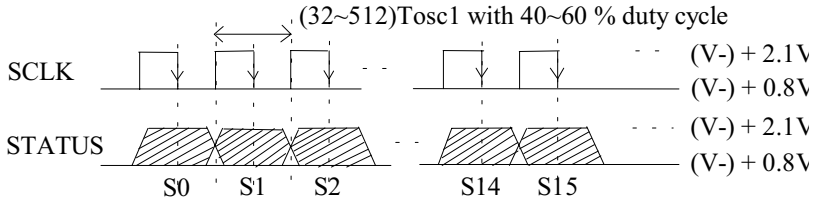
2. The END bit:

The microprocessor stopped driving STATUS between 2D and 2E, and ES51973 will begin to drive STATUS after 2F.

3. Serial Data Format (STATUS):

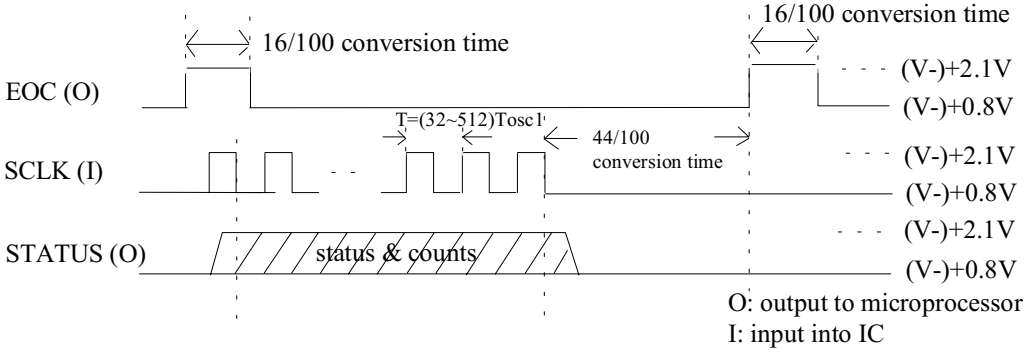
In mode 2, only the status bits ZERO C0, C1, C2, B0, B1, B2, Format and TEST are meaningful. However the microprocessor still needs to send the complete word of status (16 bits) although ES51973 will discard the other bits.

4. The detail timing between SCLK and STATUS is as follow:



Format 2:

mode 1: ES51973 sends the status and counts (counter from DINT) to uP.



Note: 1. Serial Data Format (STATUS):

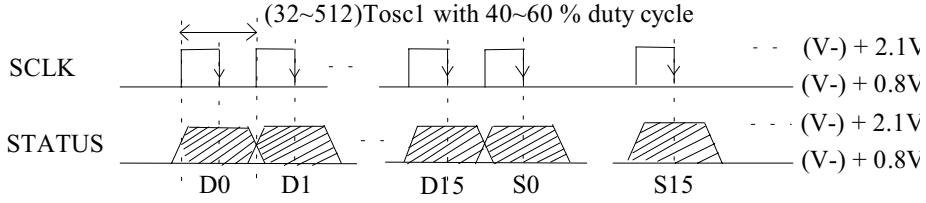
The serial data will includes status (S0~S15, 16 bits) and counts (D0~D15, 16 bits) which counter from DINT phase. The definition of status' format is the same format 1 and sent/received sequence is D0, D1, … , D15, S0, S1, … , S15. Besides, the resolutions which change as (C2, C1, C0) are listed as follow:

C 2	C 1	C 0	fcount	resolution (counts)
1	**1**	**1**	**fosc1 / 2**	**8800**
1	**1**	**0**	**fosc1 / 2**	**11000**
1	**0**	**1**	**fosc1 / 2**	**22000**
1	0	0	fosc1 / 4	22000
0	1	1	fosc1 / 8	22000
0	1	0	fosc1 / 10	22000
0	0	1	fosc1 / 20	22000
0	0	0	fosc1 / 40	22000

Note: (1) fcount : the frequency of counter.

(2) In above bold letters, because the fastest frequency of counter is restricted, the resoultion will be proportional decreased as conversion rates increased.

2. The detail timing between SCLK and STATUS is as follow:



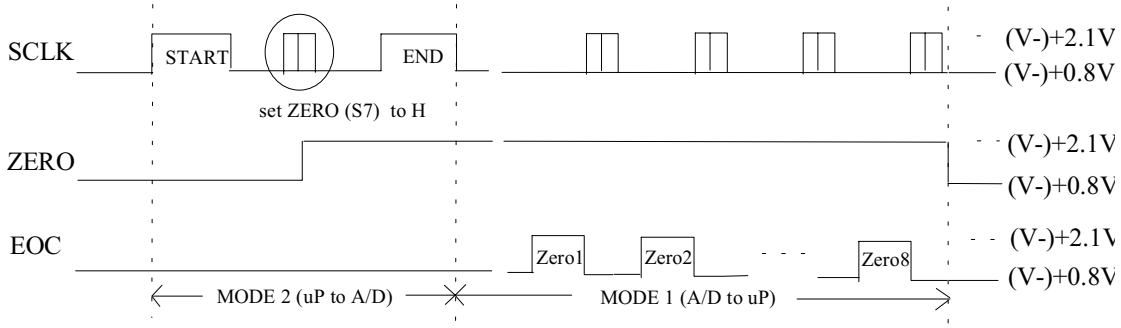
mode 2: The communication protocol is the same as mode 2 of format 1.

(7) Zero_Calibration

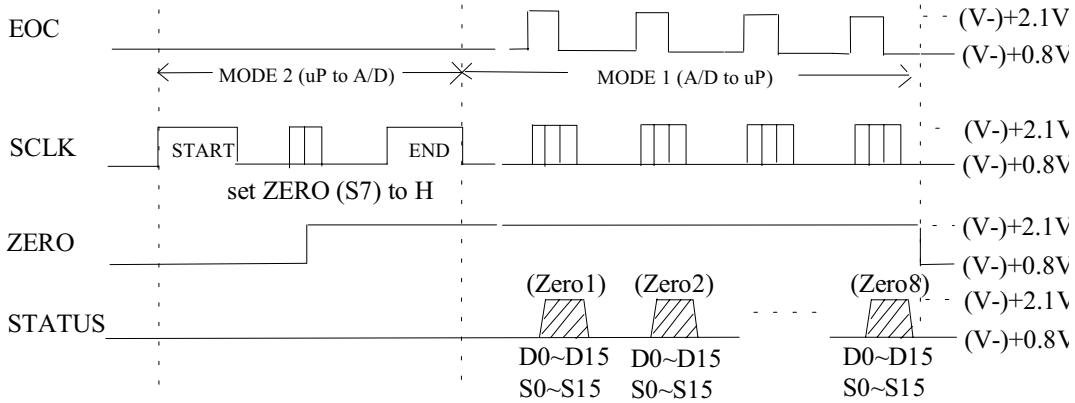
For ES51973 the A-to-D output might have an offset value due to internal delay. The amount of offset depends on conversion rate and external components: Vref, Rint and Cint. However as external components in application board are fixed. The offset will be constant. To eliminate this offset error ES51973 provides zero calibration. To perform zero calibration, the microprocessor should send a status word with ZERO bit as high with mode 1 communication. As ES51973 receives the status word it will short the Vin+ and Vin- (zero input) internally and sends eight measured values to microprocessor. The ZERO bit of the status associated with these zero input count will be high. It is recommended to let the microprocessor remember the last zero input count (Zero8) among the eight data. The offset error can be eliminated by subtracting the zero input count from the subsequent measurements. Hence zero calibration should be executed before normal conversion measurement.

It is worthy to note that ES51973 will leave zero calibration mode as it completes eight zero input measurements which means that the microprocessor need not to send another status to cancel calibration mode. In addition, as the offset value depends on conversion rate, zero calibration should be performed as long as the conversion rate changes.

Operation on Format 1:



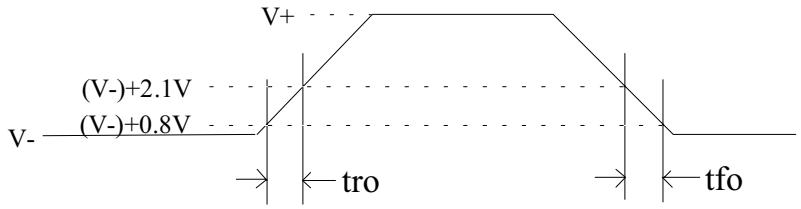
Operation on Format 2:



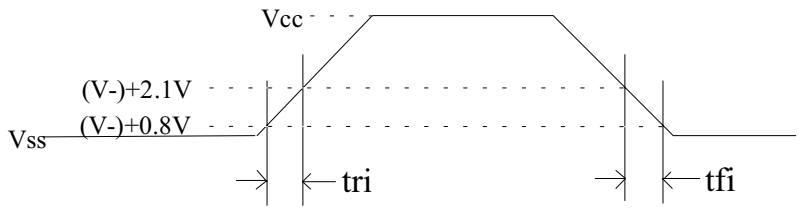
(8) Digital Signals Rising and Falling times

The digital signals include EOC, SCLK, and STATUS, and those rising and falling times are defined as follow:

EOC and STATUS are output to microprocessor:



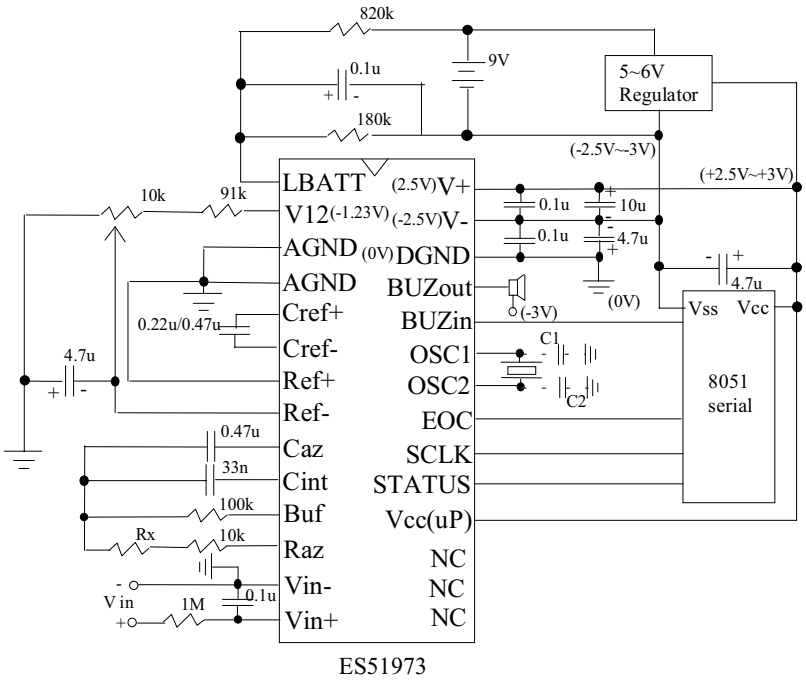
SCLK and STATUS are input from microprocessor:



Note: Vss = V-

Symbol	Condition	Min	Max	Units
tro	A/D to uP	-	20	ns
tfo	A/D to uP	-	20	ns
tri	uP to A/D	-	20	ns
tfi	uP to A/D	-	20	ns

Testing Circuit



Note: 1. Vin+, Vin- are differential inputs.

2. PHin is always reference to AGND.

3. Let the leakage current of CP+ and CP- as small as possible.

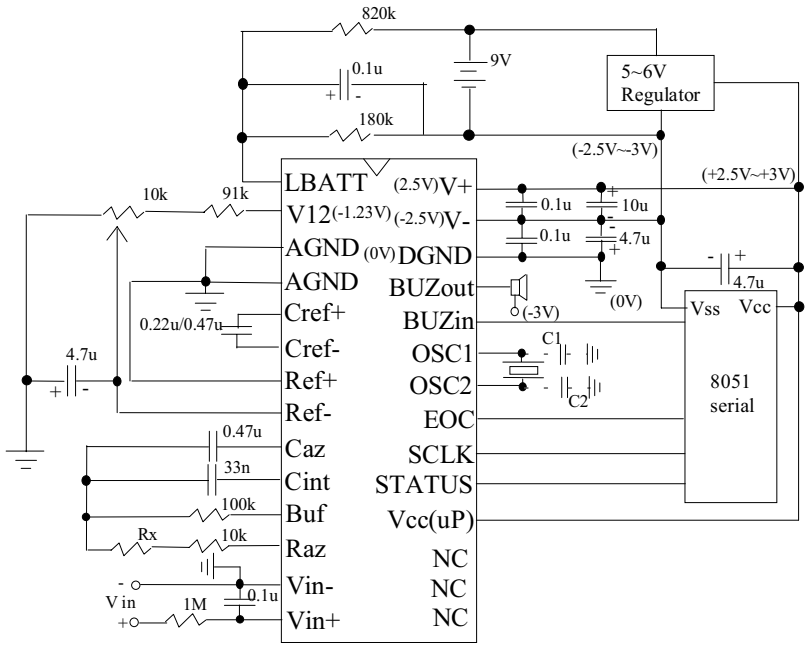
4. LBATT : $(2.5\text{-}1.23)\times\frac{180k+820k}{180k}=7.06\,\text{V}$

5. Rx = 20~100Ω , which is used to compensate the internal resistor.

6. When external crystal is <800 kHz, we wuggest the C1 (6pF) and C2 (8~22pF) to make it work.

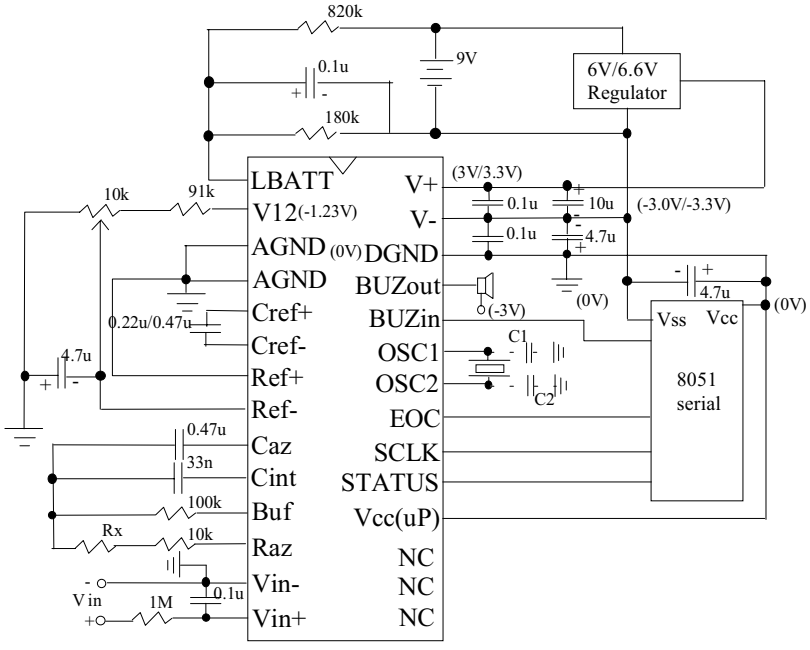
Application Circuit

9V battery and 5V microprocessor:



ES51973

9V battery and 3.3V/3.0V microprocessor:

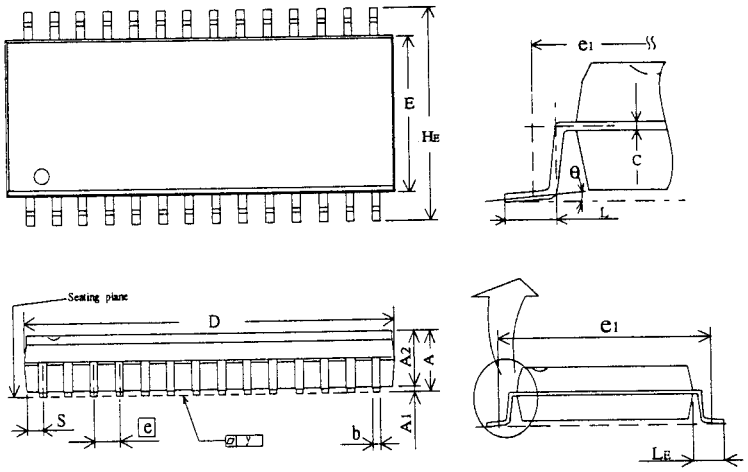


ES51973

Note: Please see the notes of testing circuit.

Package

28 pins SOP package size:



Symbol	Dimension in inch	Dimension in mm
A	0.110 MAX	2.794 MAX
A_1	0.004 MIN	0.102 MIN
A_2	0.093 +/- 0.005	2.362 +/- 0.127
b	$0.016^{+0.004}_{-0.002}$	$0.406^{+0.102}_{-0.051}$
C	$0.010^{+0.004}_{-0.002}$	$0.254^{+0.102}_{-0.051}$
D	0.705TYP (0.725MAX)	17.907TYP (18.415MAX)
E	0.295 +/- 0.005	7.493 +/- 0.127
e	0.050 +/- 0.006	1.270 +/- 0.152
e_1	0.370 NOM	9.398 NOM
H_E	0.406 +/- 0.012	10.312 +/- 0.305
L	0.036 +/-0.008	0.914 +/- 0.203
L_E	0.055 +/- 0.008	1.397 +/- 0.203
S	0.043 MAX	1.092 MAX
y	0.004 MAX	0.102 MAX
θ	0°~ 10°	0°~ 10°