

Features

- Operates from 5V input supply
- 2 Regulated Voltage are provided
 - Standard Buck Switching Power for VMEM (2.5V)
 - Linear Controller with Source-Sink Regulation for VTT(1.25V)
- Simple Single-Loop Control Design
 - Voltage-Mode PWM Control
- Excellent Output Voltage Regulation
 - VMEM Output : $V_{MEM} \pm 1.5\%$ Over Temperature
 - VTT Output : $1/2 V_{IN} \pm 25mV$ Over Temperature
- Fast Transient Response
 - Built-in Feedback Compensation
 - Full 0% to 100% Duty Ratio
- Over-Voltage and Over-Current Fault Monitors
- Constant Frequency Operation(200kHz)
- 16 pins, SSOP Package

Applications

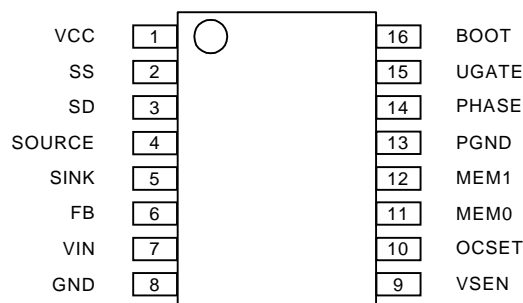
- M/B DDR Power Regulation
- AGP/PCI Graphics Power Regulation
- SSTL-2 Termination

General Description

The APW7055 provides the power control and protections for two output voltages on M/B DDR applications. It integrates one PWM controller , one source-sink linear controller(LC) for DDR source-sink purpose, as well as the monitor and protection functions into a single package. The PWM controller supplies the VMEM(2.5V) with a standard buck converter. The source-sink linear controller regulates VTT(1.25V) power for DDR Termination.

Additional built-in over-voltage protection (OVP) will be started when the VMEM output is above 115% of the internal DAC setting(V_{DAC}) . OVP function will shut-down the upper MOSFET and disable all output voltage . The PWM controller's over-current function monitors the output current by sensing the voltage drop across the upper MOSFET's $r_{DS(ON)}$, eliminating the need for a current sensing resistor .

Pin Description



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Thermal Characteristics

Symbol	Parameter	Value	Unit
R _{JA}	Thermal Resistance in Free Air	75	°C/W
	SOIC SOIC (with 3in ² of Copper)	65	

Electrical Characteristics

1. Recommended operating conditions, Unless otherwise noted.
2. Refer to Block and Simplified Power System Diagrams , and Typical Application Schematic.

Symbol	Parameter	Test Conditions	APW7055			Unit
			Min.	Typ.	Max.	
Supply Current						
I _{CC}	Nominal Supply Current	SD=0V, GATE Drive Open		7		mA
	Shutdown Supply Current	SD=5V		2.7		
Power-on Reset						
V _{CC}	Rising VCC Threshold	Vocset=3V		4.2	4.6	V
	Falling VCC Threshold	Vocset=3V	3.6			
V _{OCSET}	Rising V _{OCSET} Threshold			1.26		V
V _{SD}	Shutdown Input High Voltage		2.0			V
	Shutdown Input Low Voltage				0.8	
Oscillator						
F _{OSC}	Free Running Frequency		185	200	215	kHz
ΔV _{OSC}	Ramp Amplitude			1.9		V
PWM Controller Reference Voltage						
V _{DAC}	DAC Voltage Accuracy		-1.5		+1.5	%
	MEM0-1 Input High Voltage		2.0			V
	MEM0-1 Input Low Voltage				0.8	
Source-Sink Linear Controller						
V _{SOURCE}	Source Regulation Voltage		-10mV	0.495VIN	+10mV	V
V _{SINK}	Sink Regulation Voltage		-10mV	0.505VIN	+10mV	
I _{SOURCE}	Source Drive Current			0.8		mA
I _{SINK}	Sink Drive Current			0.8		
PWM Controllers Gate Drivers						
I _{UGATE}	UGATE Source	V _{CC} =5V, V _{BOOT} =9.5V, V _{UGATE} =6V		1		A
		V _{CC} =12V, V _{BOOT} =9.5V, V _{UGATE} =6V		1		
R _{GATE}	UGATE Sink	V _{CC} =5V, V _{UGATE} =1V		3		Ω
		V _{CC} =12V, V _{UGATE} =6V		3	3.5	

Electrical Characteristics (Cont.)

1. Recommended operating conditions, Unless otherwise noted.
2. Refer to Block and Simplified Power System Diagrams , and Typical Application Schematic.

Symbol	Parameter	Test Conditions	APW7055			Unit
			Min.	Typ.	Max.	
Protection						
	VSEN O.V. trip point (VSEN/V _{DAC})	VSEN Rising		115	120	%
	VSEN O.V. Hysteresis			2		
I _{OCSET}	Ocset Current Source	Vocset=3V	170	200	230	uA
I _{SS}	Soft start Current			28		

Functional Pin Description

VCC (Pin 1)

Provide a +5V bias supply for the IC to this pin. This pin also provides the gate bias charge for the MOS FETs of the source-sink regulator. The voltage at this pin is monitored for Power-On Reset (POR) purposes.

SS (Pin 2)

This pin provides the soft start for the standard buck converter and source-sink regulator. Connect a capacitor from this pin to ground. This capacitor, along with an internal 28uA current source, sets the soft-start interval of the converter and preventing the outputs from overshoot as well as limiting the input current .

SD (Pin 3)

The pin shuts down all the outputs. A TTL-compatible, logic level high signal applied at this pin immediately discharges the soft-start capacitor, disabling all the outputs. When IC re-enabled, the IC undergoes a new soft-start cycle. Left open, this pin is pulled low by an internal pull-down resistor, enabling operation.

SOURCE (Pin 4)

Connect the pin to the upper MOSFET gate drive of the source-sink regulator. This pin is used to drive the

upper external MOSFET as a source regulator.

SINK (Pin 5)

Connect the pin to the lower MOSFET gate drive of the source-sink regulator. This pin is used to drive the lower external MOSFET as a sink regulator.

FB (Pin 6)

Connect this pin to output of the source-sink regulator. This pin provide the voltage feedback path for source and sink regulators. This pin is internally connected to the negative input of the source controller, and also connected to the positive input of the sink controller.

VIN (Pin 7)

Connect this pin to a voltage source. Two voltages, above 0.5VIN, are generated by an internal resistor divider as the reference voltage of the source and sink controllers. The internal resistor divider provides an offset voltage to ensure higher sink regulation voltage and prevent a direct current path through the upper and lower MOSFETs, damaging the two MOSFETs.

GND (Pin 8)

Signal ground for the IC. All voltage levels are measured with respect to this pin voltage protection.

Functional Pin Description (Cont.)

VSEN (Pin 9)

This pin is connected to the standard buck converter's output voltage to provide the voltage feedback path for PWM converter. The OVP(Over-Voltage-Protection) comparator circuit use this signal to monitor output voltage status for over-voltage protection.

OCSET (Pin 10)

Connect a resistor (R_{OCSET}) from this pin to the drain of the standard buck PWM converter's MOSFET. R_{OCSET} , an internal 200mA current source (I_{OCSET}), and the MOSFET's on-resistance($r_{DS(ON)}$) set the converter's over-current (OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

An over-current trip cycles the soft-start function

MEM0-1 (Pin 11-12)

MEM0-1 are TTL-compatible logic level input pins of the 2-bits DAC. The status of these 2 pins set the internal reference voltage(V_{DAC}) for the standard buck converter and also sets the OVP threshold voltage. Table 1 shows the DAC table voltage.

Table 1 DAC Table

APW7055 - A

Pin Name		V_{MEM} Voltage
MEM1	MEM0	
0	0	2.40
0	1	2.45
1	0	2.50
1	1	2.55

APW7055 - B

Pin Name		V_{MEM} Voltage
MEM1	MEM0	
0	0	2.60
0	1	2.65
1	0	2.70
1	1	2.75

PGND (Pin 13)

This is the power ground connection. Tie this pin to the anode of the flywheel diode of the standard buck PWM converter's circuit.

PHASE (Pin 14)

Connect the PHASE pin to the standard buck PWM converter's MOSFET source. This pin is used to monitor the voltage drop across the MOSFET for over-current protection.

UGATE (Pin 15)

Connect this pin to the MOSFET gate of the standard buck PWM converter. This pin provides the gate drive for the external MOSFET.

BOOT (Pin 16)

This pin provides bias voltage to the external MOSFET driver. A bootstrap circuit may be used to pump a boot voltage for enforcing the driving capability of the gate driver and improving the performance of the MOSFET.

Table 1 DAC Table

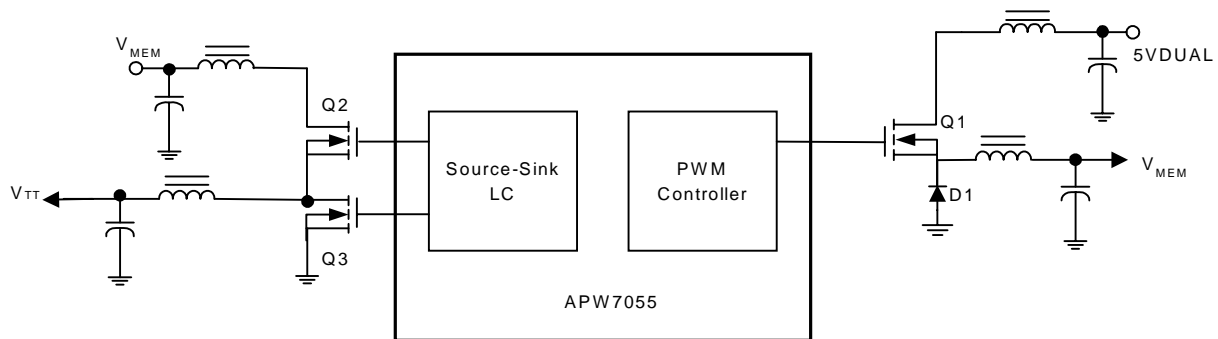
APW7055 - C

Pin Name		V_{MEM} Voltage
MEM1	MEM0	
0	0	2.80
0	1	2.85
1	0	2.90
1	1	2.95

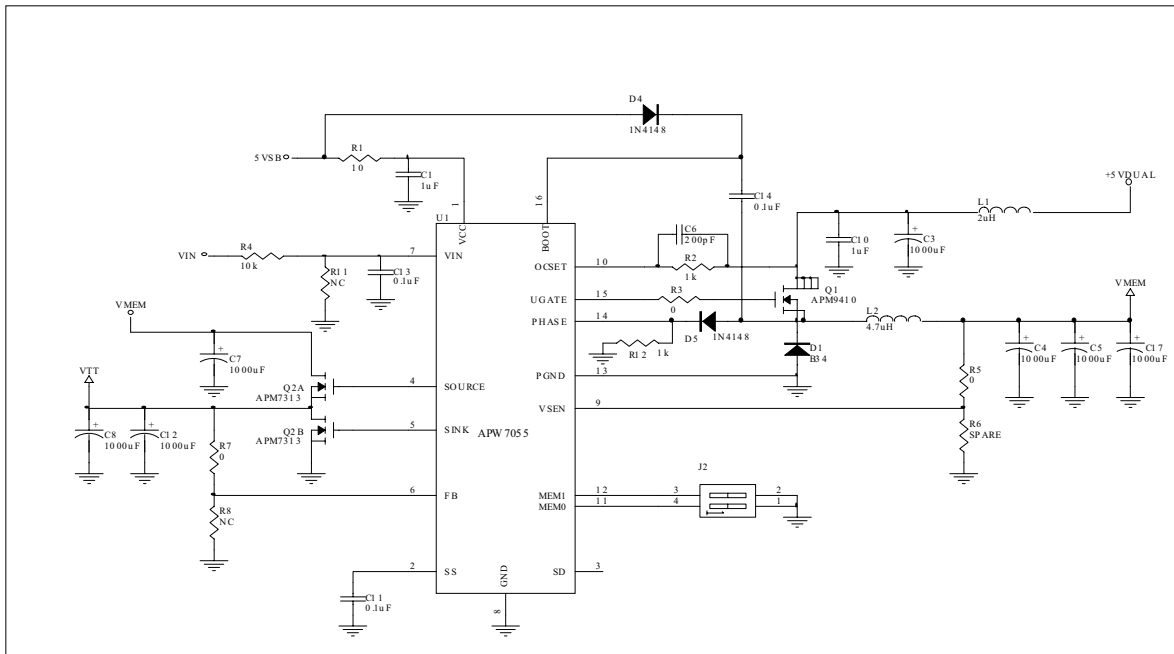
APW7055 - D

Pin Name		V_{MEM} Voltage
MEM1	MEM0	
0	0	3.00
0	1	3.05
1	0	3.10
1	1	3.15

Simplified Power System Diagram

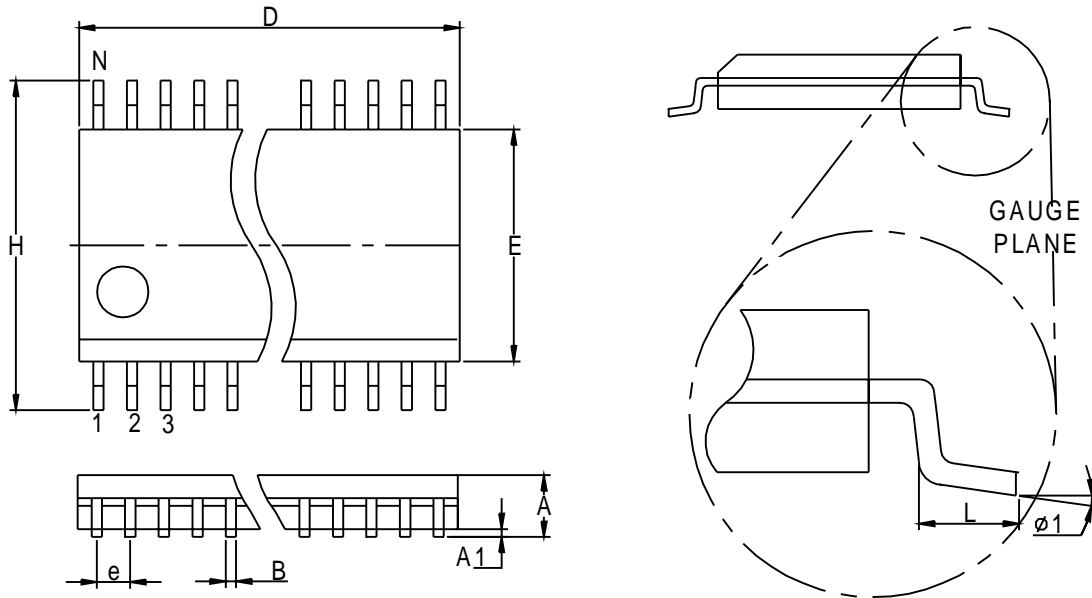


Typical Application Circuit



Package Informaion

SSOP-16

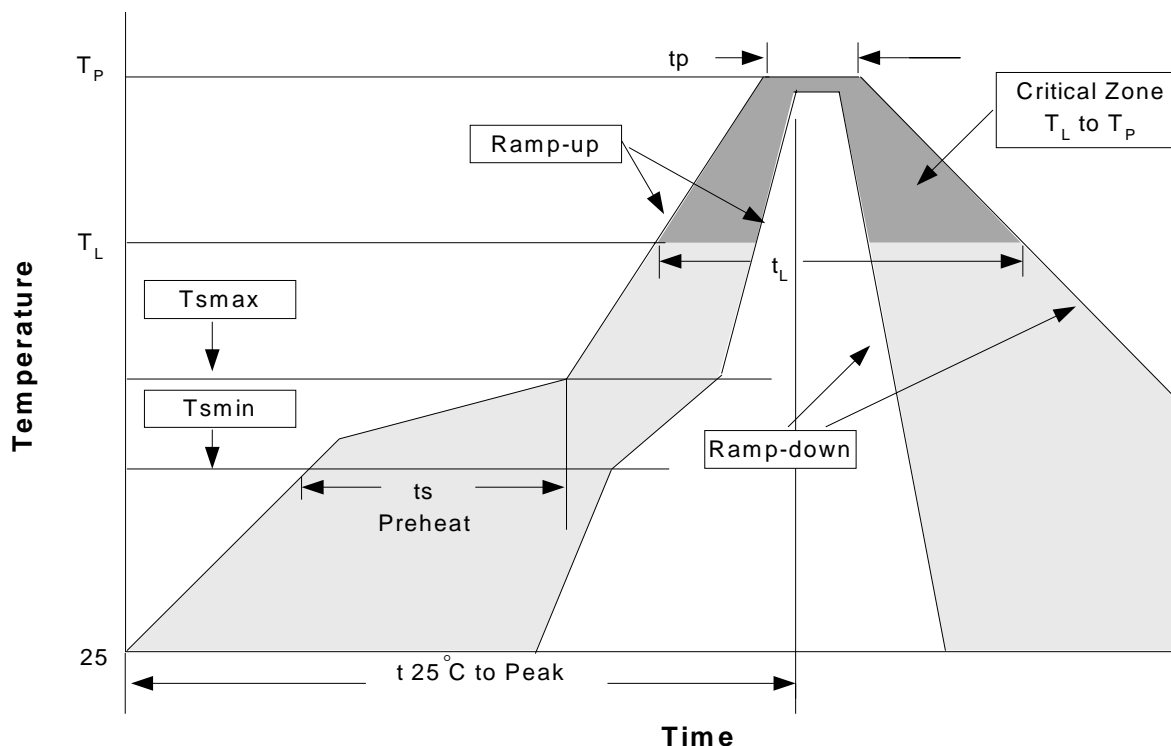


Dim	Millimeters		Variations- D			Dim	Inches		Variations- D		
	Min.	Max.	Variations	Min.	Max.		Min.	Max.	Variations	Min.	Max.
A	1.350	1.75	SSOP-16	4.75	5.05	A	0.053	0.069	SSOP-16	0.187	0.199
A1	0.10	0.25				A1	0.004	0.010			
B	0.20	0.30				B	0.008	0.012			
D	See variations					D	See variations				
E	3.75	4.05				E	0.147	0.160			
e	0.625 TYP.					e	0.025 TYP.				
H	5.75	6.25				H	0.226	0.246			
L	0.4	1.27				L	0.016	0.050			
N	See variations					N	See variations				
φ 1	0°	8°				φ 1	0°	8°			

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

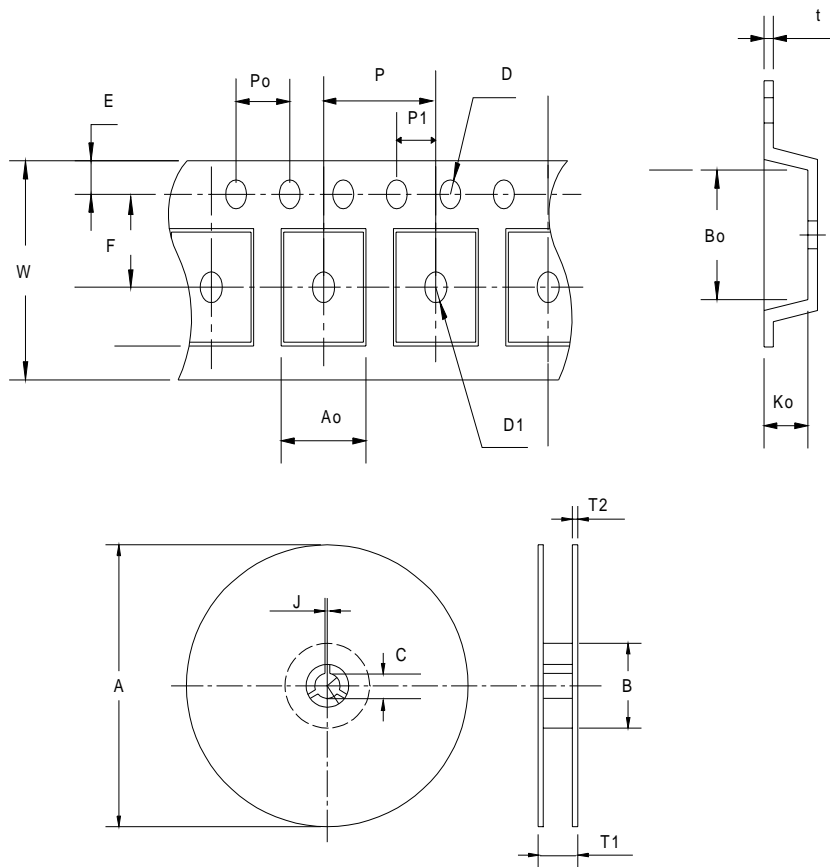
Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly	
	Large Body	Small Body	Large Body	Small Body
Average ramp-up rate (T_L to T_P)	3°C/second max.		3°C/second max.	
Preheat				
- Temperature Min (T_{smin})	100°C		150°C	
- Temperature Mix (T_{smax})	150°C		200°C	
- Time (min to max)(t_s)	60-120 seconds		60-180 seconds	
T_{smax} to T_L			3°C/second max	
- Ramp-up Rate				
T_{smax} to T_L				
- Temperature(T_L)	183°C		217°C	
- Time (t_L)	60-150 seconds		60-150 seconds	
Peak Temperature(T_p)	225 +0/-5°C	240 +0/-5°C	245 +0/-5°C	250 +0/-5°C
Time within 5°C of actual Peak Temperature(t_p)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.		6°C/second max.	
Time 25°C to Peak Temperature	6 minutes max.		8 minutes max.	

Note: All temperatures refer to topside of the package. Measured on the body surface.

Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I _{tr} > 100mA

Carrier Tape & Reel Dimensions



Application	A	B	D0	D1	E	F	P0	P1	P2
SSOP-16	6.95	5.4	1.55±0.05	1.55±0.1	1.75±0.1	5.5±0.05	4.0±0.1	8.0±0.1	2.0±0.05
	T	T2	W	W1	C1	C2	T1	T2	C
	0.3±0.05	2.2	12.0±0.3	9.5	13±0.3	21±0.8	13.5±0.5	2.0±0.2	80±1

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 16	24	21.3	1000

Customer Service**Anpec Electronics Corp.**

Head Office :

5F, No. 2 Li-Hsin Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :

7F, No. 137, Lane 235, Pac Chiao Rd.,
Hsin Tien City, Taipei Hsien, Taiwan, R. O. C.
Tel : 886-2-89191368
Fax : 886-2-89191369