



SANYO Semiconductors

DATA SHEET

LA8120T — Monolithic Linear IC

AGC Amplifier with Step Gain Control

Overview

The LA8120T bipolar monolithic IC is an AGC amplifier with driver amplifier for analog-to-digital converters. It is ideally suited for use with receiver systems that receive QPSK and/or QAM data transmissions.

Functions

- IF AGC control
- IF AGC amplifier
- IF Step Gain Controlled Amplifier
- Driver amplifier

Applications

- Digital CATV
- Cable modem receivers
- IP Telephony receivers

Specifications

Absolute Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum Supply voltage	V _{CC} max	Pin 1	7.0	V
Circuit Voltages	V max	Pin 4, Pin 5	V _{CC} op	V
Circuit Current	I ₆ I ₇	Pin 6 sink current Pin 7 sink current	2 2	mA
Allowable Power Dissipation	Pd max	Ta ≤ 85°C *	220	mW
Operating Temperature	Topr		-20 to +85	°C
Storage Temperature	Tstg		-55 to +150	°C

* Mounted on PCB : 20.0mm × 10.0mm × 0.8 mm, paper phenol.

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SANYO Semiconductor Co., Ltd.

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

LA8120T

Recommended Operating Conditions at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended Supply Voltage	V _{CC}	Pin 1	5.0	V
Operating Supply Voltage Range	V _{CC op}	Pin 1	4.5 to 5.5	V

Electrical Characteristics

AC Characteristics at Ta = 25 °C, V_{CC} = 5.0 V

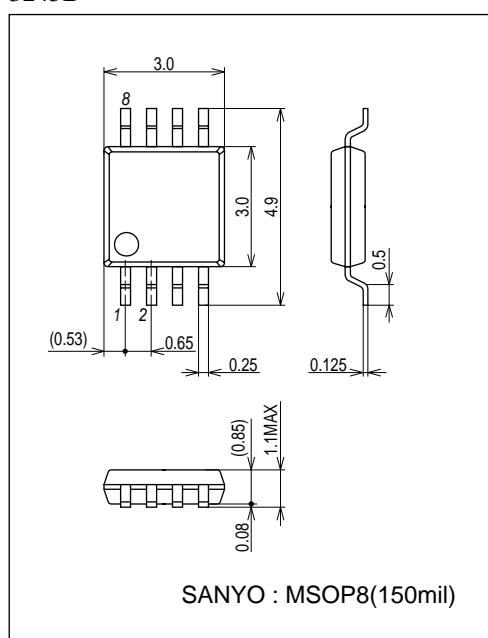
Parameter	Symbol	Pin No.	Conditions	Ratings			Unit	
				min	typ	max		
Circuit Current	I _{total}	1	No Signal	*1	25	30	35 mA	
IF Input Frequency Range	f(in)	2, 3	f _c : -3 dB	*1	30		100 MHz	
Noise Figure	NF	6, 7	V ₄ = 3.0 V, f = 45 MHz	Pin 5 : V _{CC}	*2		5 dB	
			V ₄ = 3.0 V, f = 45 MHz	Pin 5 : GND	*2		6 dB	
			V ₄ = 3.0 V, f = 45 MHz	Pin 5 : OPEN	*2		8 dB	
Intermodulation	IM3	6/2, 3 7/2, 3	f ₁ = 44 MHz, f ₂ = 45 MHz Input = 90 dB _μ /Tone, Output = 104 dB _μ /Tone	*1	50		dBc	
Total Amplifier Gain	G(AGC1)	6/2, 3 7/2, 3	V ₄ = 3.0 V, f = 45 MHz	Pin 5 : V _{CC}	*1	45.5	48	50.5 dB
	G(AGC2)	6/2, 3 7/2, 3	V ₄ = 3.0 V, f = 45 MHz	Pin 5 : GND	*1	41.5	44	46.5 dB
	G(AGC3)	6/2, 3 7/2, 3	V ₄ = 3.0 V, f = 45 MHz	Pin 5 : OPEN	*1	33.5	36	38.5 dB
AGC Range 1	GR1	6/2, 3 7/2, 3	IF Output Level < ±1 dB, f = 45 MHz	*1	40		dB	
IF Output Level	V _O (IF)	6, 7	Output Level, f = 45 MHz	*1		1.0	V _{p-p}	
AGC Control Max. Voltage	V _{4H}	4	Gain Max.	*1	2.5		3 V	
AGC Control Min. Voltage	V _{4L}	4	Gain Min.	*1	0		0.5 V	
Input impedance	Z _{in}	2, 3	V ₄ = 0 V, f = 45 MHz	*3		1 // 4.9	kΩ // pF	

*1 : Measurement circuit 1, *2 : Measurement circuit 2, *3 : Measurement circuit 3

Package Dimensions

unit : mm (typ)

3245B

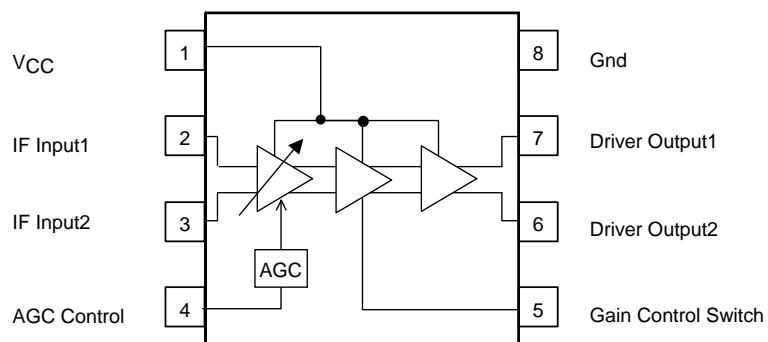


LA8120T

Pin Functions

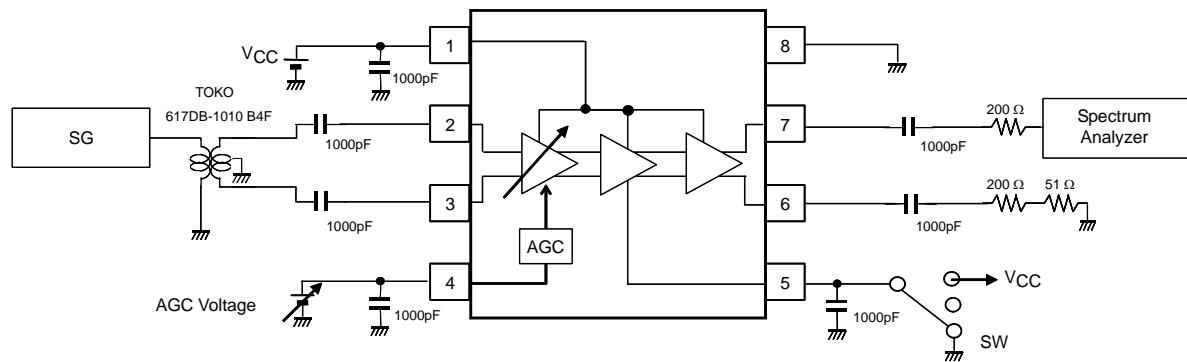
Pin Number	Pin Name	Equivalent Circuit
1	V _{CC}	
2 3	IF Input	<p>The circuit shows a bias network consisting of two 1kΩ resistors connected to ground. The non-inverting input (pin 2) is connected to the top node of the first resistor and to the base of a transistor. The inverting input (pin 3) is connected to the bottom node of the first resistor and to the base of another transistor. The emitters of these transistors are connected to ground. The outputs of the transistors are connected to a second stage, which includes a 1kΩ resistor and a feedback loop.</p>
4	AGC Control	<p>The circuit shows a voltage-controlled current source. Pin 4 is connected to V_{CC} through a 1kΩ resistor. The output of this stage is connected to the base of a transistor, which has its collector connected to ground.</p>
5	Gain Control Switch	<p>The circuit shows a switchable gain stage. Pin 5 is connected to V_{CC} through a 10kΩ resistor. The output of this stage is connected to the base of a transistor, which has its collector connected to ground. The base of this transistor is also connected to the collector of a second transistor, whose base is controlled by pin 4.</p>
6 7	Driver Output	<p>The circuit shows a push-pull driver stage. Pins 6 and 7 are connected to V_{CC} through 20Ω resistors. The outputs of these stages are connected to two 8.0mA current sources, which drive the collector of a pair of transistors. The bases of these transistors are connected to ground.</p>
8	GND	

Block Diagram

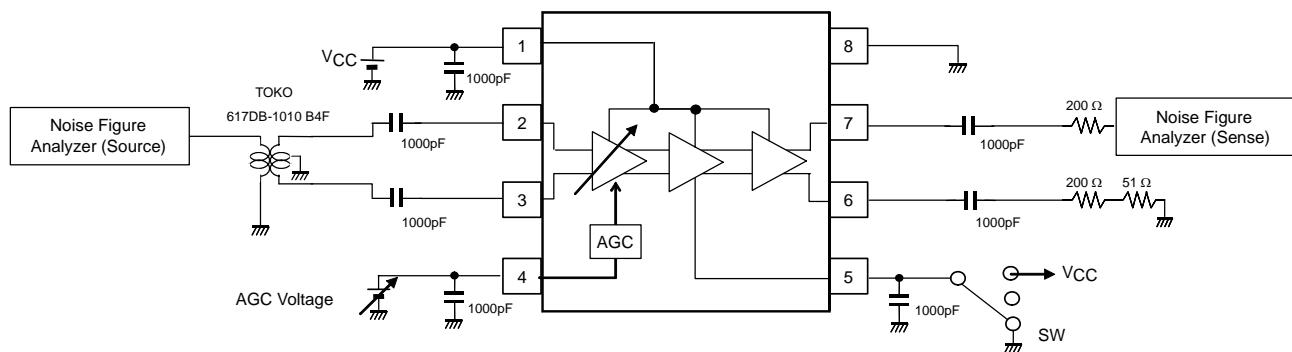


LA8120T

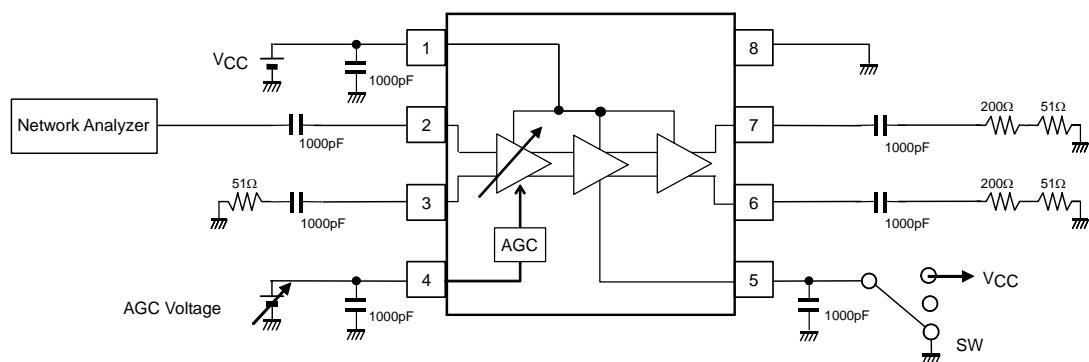
LA8120T Gain, Measurement Circuit 1



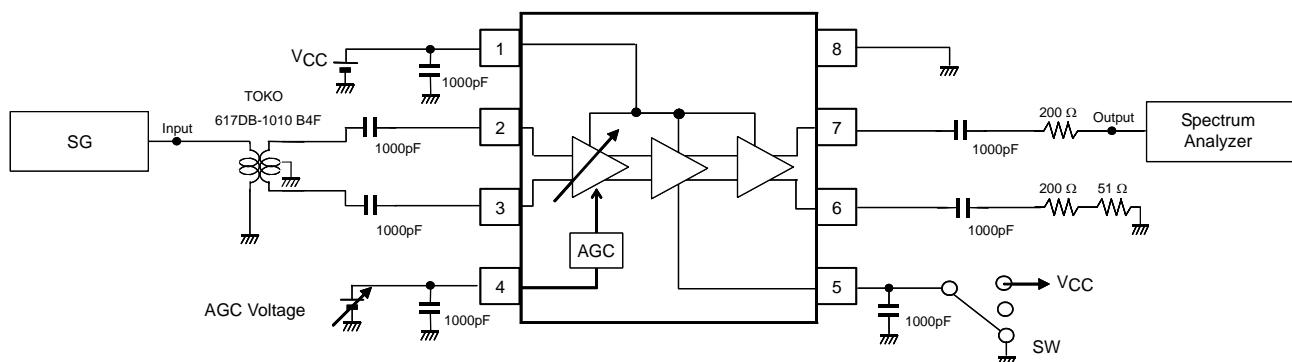
LA8120T Noise Figure Measurement Circuit 2



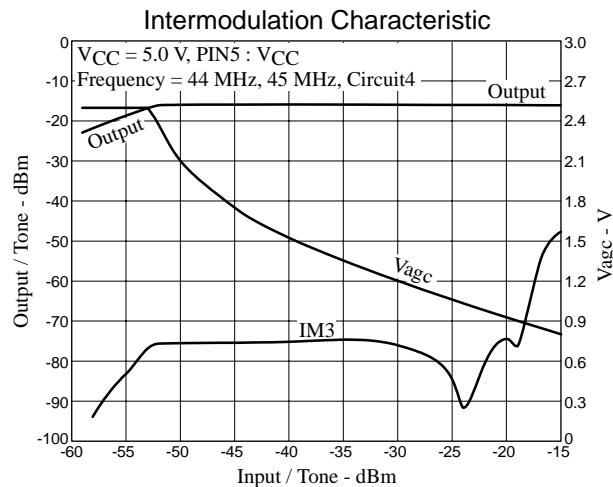
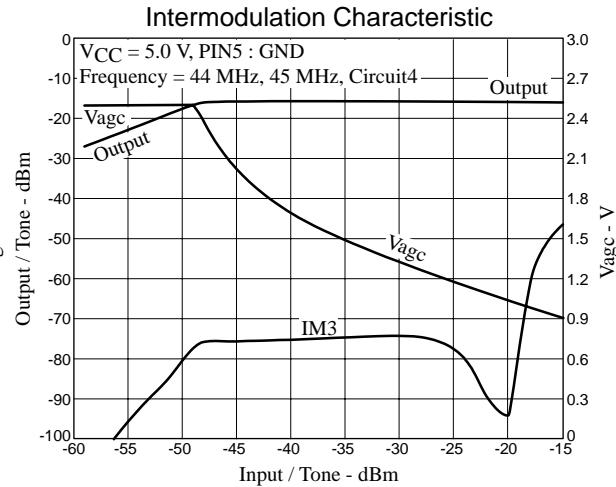
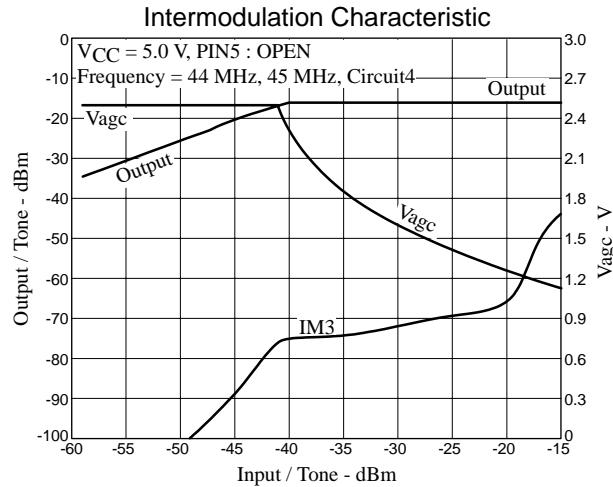
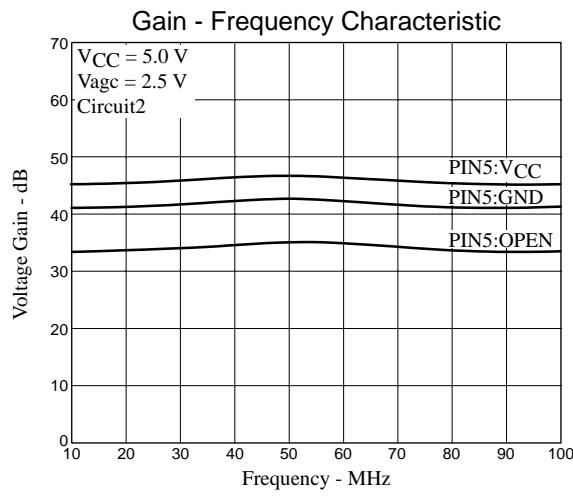
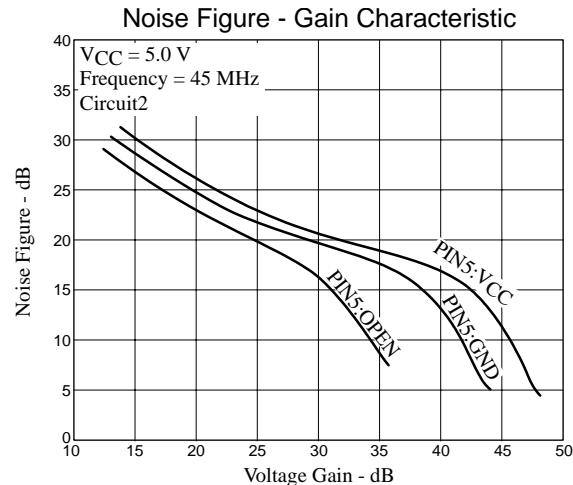
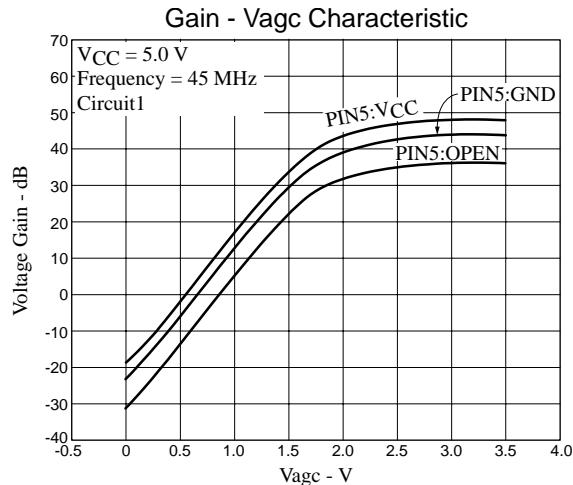
LA8120T Input Impedance Measurement Circuit 3



LA8120T Intermodulation Measurement Circuit 4



LA8120T



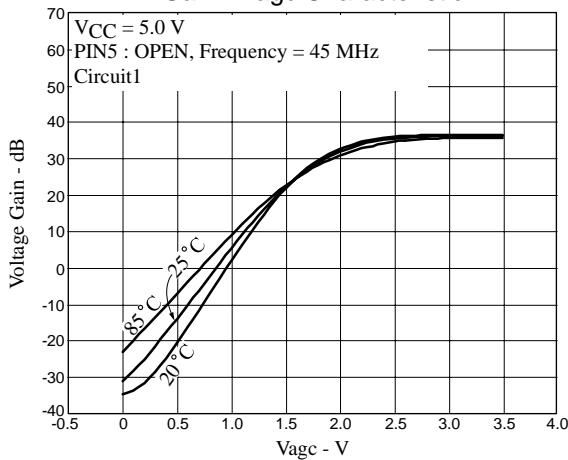
The vertical axis (Output/Tone) on this graph shows the values displayed by the spectrum analyzer for circuit 4.

The actual output power for the corresponding pins is given by the following formula.

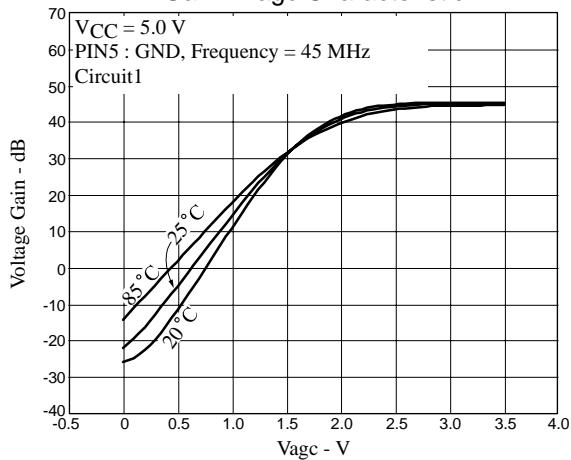
$$\{\text{output power [dBm]}\} = \{\text{displayed value [dBm]}\} + 10 \cdot \log (250 \Omega / 50 \Omega)$$

LA8120T

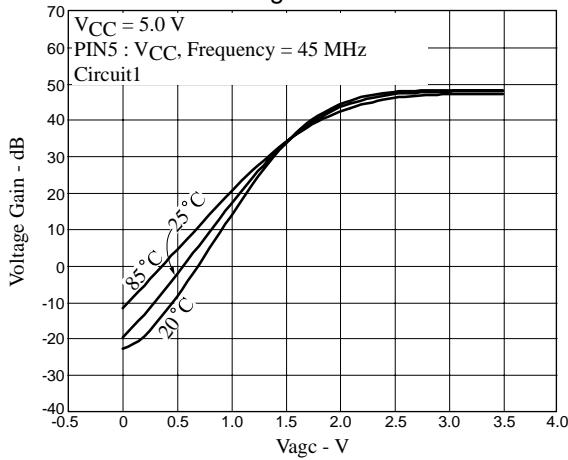
Gain - Vagc Characteristic



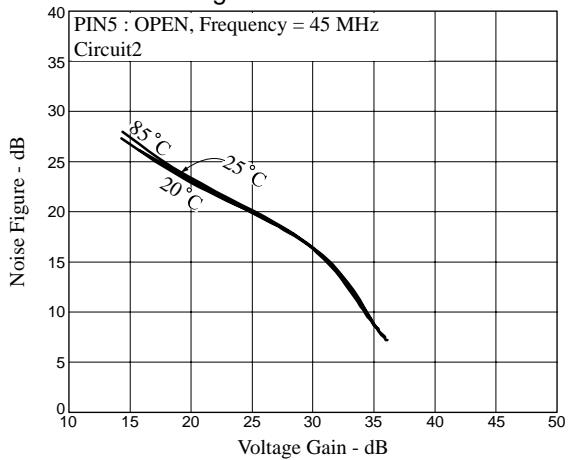
Gain - Vagc Characteristic



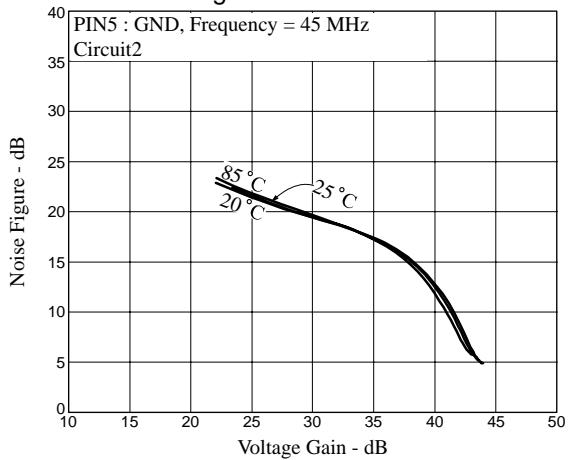
Gain - Vagc Characteristic



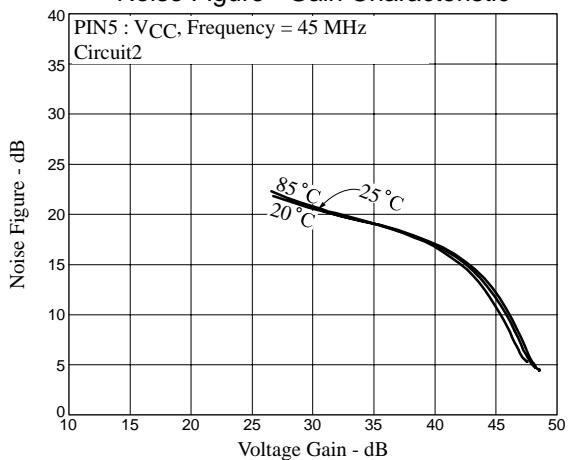
Noise Figure - Gain Characteristic



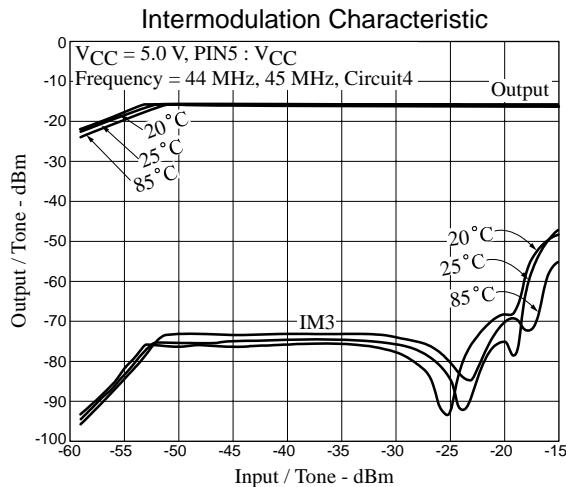
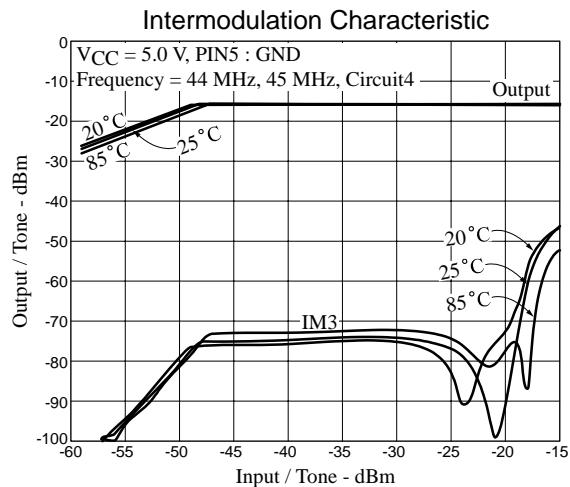
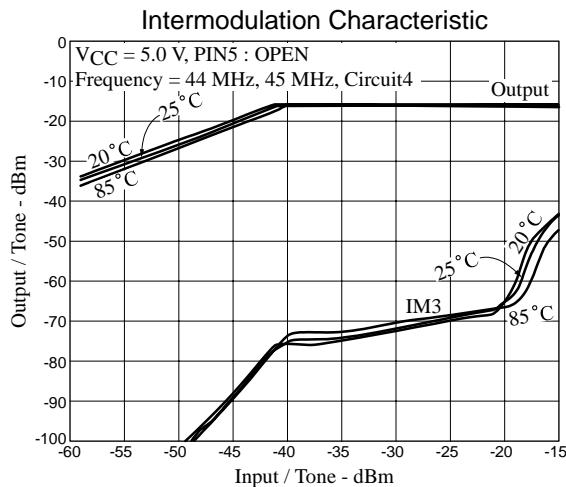
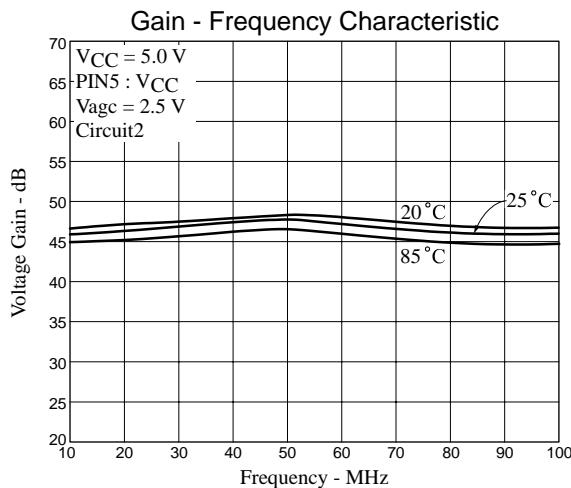
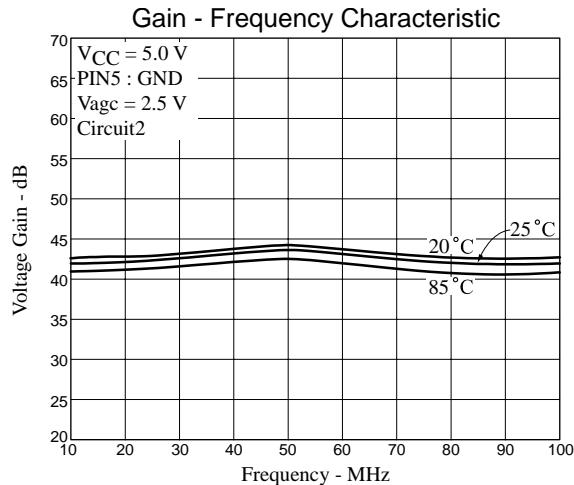
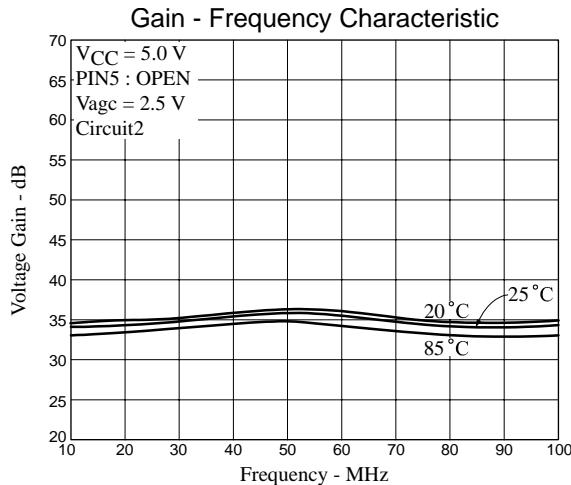
Noise Figure - Gain Characteristic



Noise Figure - Gain Characteristic



LA8120T



The vertical axis (Output/Tone) on this graph shows the values displayed by the spectrum analyzer for circuit 4.

The actual output power for the corresponding pins is given by the following formula.

$$\{\text{output power [dBm]}\} = \{\text{displayed value [dBm]}\} + 10 \cdot \log (250 \Omega / 50 \Omega)$$

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