

# Smart Four Channel Highside Power Switch

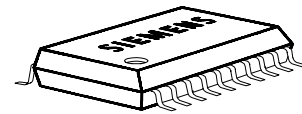
## Features

- Overload protection
- Current limitation
- Short-circuit protection
- Thermal shutdown
- Overvoltage protection (including load dump)
- Fast demagnetization of inductive loads
- Reverse battery protection<sup>1)</sup>
- Undervoltage and overvoltage shutdown with auto-restart and hysteresis
- Open drain diagnostic output
- Open load detection in ON-state
- CMOS compatible input
- Loss of ground and loss of  $V_{bb}$  protection
- **Electrostatic discharge (ESD)** protection

## Product Summary

|                                   |                  |            |              |               |    |
|-----------------------------------|------------------|------------|--------------|---------------|----|
| Overvoltage Protection            | $V_{bb(AZ)}$     | 43         | V            |               |    |
| Operating voltage                 | $V_{bb(on)}$     | 5.0 ... 34 | V            |               |    |
|                                   | active channels: | one        | two parallel | four parallel |    |
| On-state resistance $R_{ON}$      |                  | 100        | 50           | 25            | mΩ |
| Nominal load current $I_{L(NOM)}$ |                  | 2.9        | 4.3          | 6.3           | A  |
| Current limitation $I_{L(SCr)}$   |                  | 8          | 8            | 8             | A  |

P-DSO-20



## Application

- $\mu$ C compatible power switch with diagnostic feedback for 12 V and 24 V DC grounded loads
- All types of resistive, inductive and capacitive loads
- Replaces electromechanical relays and discrete circuits

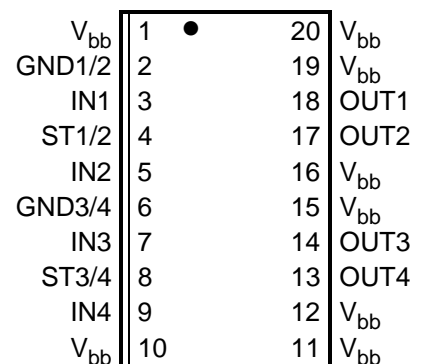
## General Description

N channel vertical power FET with charge pump, ground referenced CMOS compatible input and diagnostic feedback, monolithically integrated in Smart SIPMOS technology. Providing embedded protective functions.

### Pin Definitions and Functions

| Pin                                | Symbol   | Function   |
|------------------------------------|----------|--|
| 1,10,<br>11,12,<br>15,16,<br>19,20 | $V_{bb}$ | <b>Positive power supply voltage.</b> Design the wiring for the simultaneous max. short circuit currents from channel 1 to 4 and also for low thermal resistance |
| 3                                  | IN1      | <b>Input 1 .. 4</b> , activates channel 1 .. 4 in case of logic high signal  |
| 5                                  | IN2      |  |
| 7                                  | IN3      |  |
| 9                                  | IN4      |  |
| 18                                 | OUT1     | <b>Output 1 .. 4</b> , protected high-side power output of channel 1 .. 4. Design the wiring for the max. short circuit current                                  |
| 17                                 | OUT2     |  |
| 14                                 | OUT3     |  |
| 13                                 | OUT4     |  |
| 4                                  | ST1/2    | <b>Diagnostic feedback 1/2</b> of channel 1 and channel 2, open drain, low on failure  |
| 8                                  | ST3/4    | <b>Diagnostic feedback 3/4</b> of channel 3 and channel 4, open drain, low on failure  |
| 2                                  | GND1/2   | <b>Ground 1/2</b> of chip 1 (channel 1 and channel 2)  |
| 6                                  | GND3/4   | <b>Ground 3/4</b> of chip 2 (channel 3 and channel 4)  |

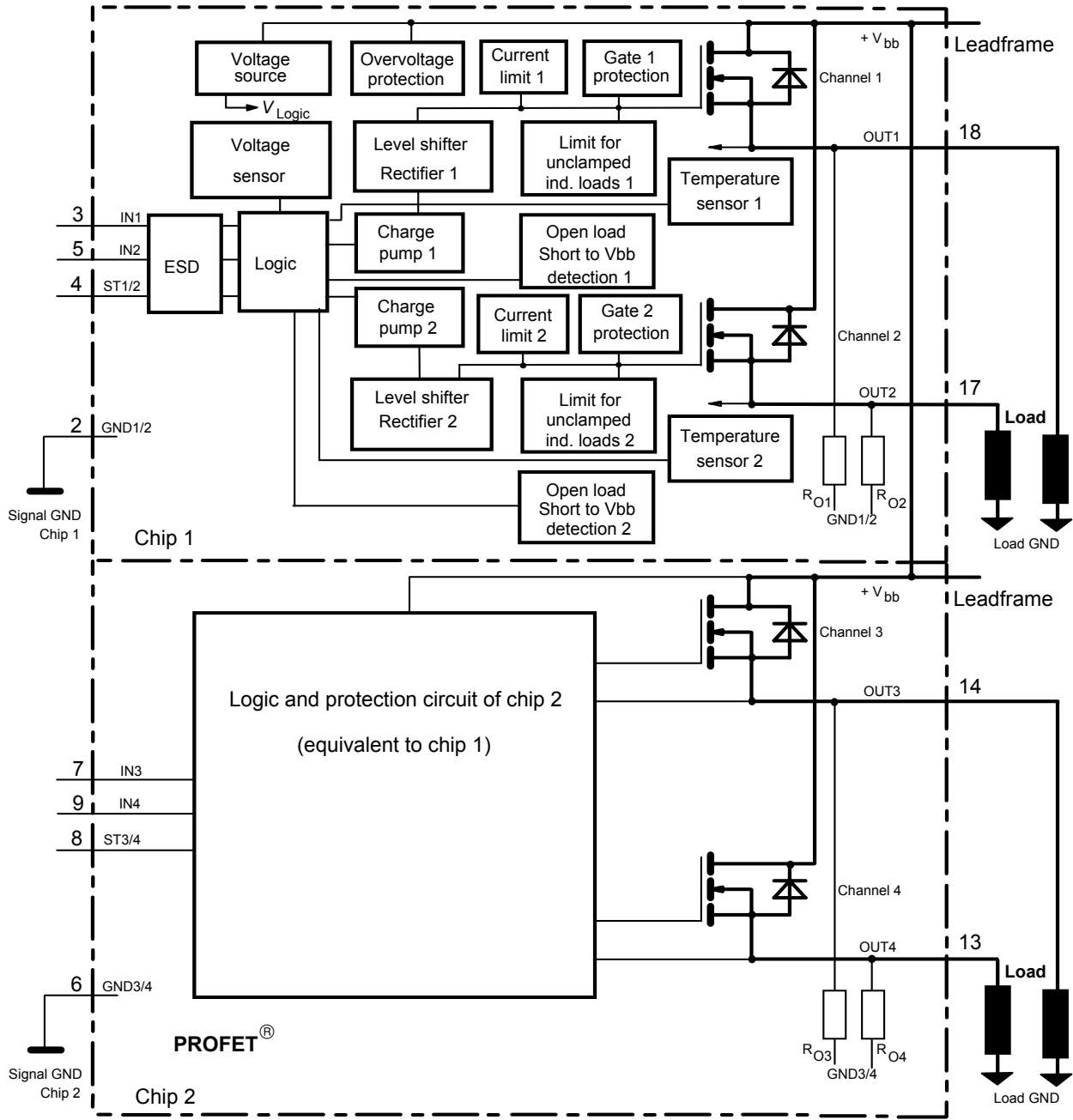
Pin configuration (top view)



<sup>1)</sup> With external current limit (e.g. resistor  $R_{GND}=150\ \Omega$ ) in GND connection, resistor in series with ST connection, reverse load current limited by connected load.

### Block diagram

Four Channels; Open Load detection in on state;



Leadframe connected to pin 1, 10, 11, 12, 15, 16, 19, 20

**Maximum Ratings** at  $T_j = 25^\circ\text{C}$  unless otherwise specified

| Parameter   | Symbol   | Values             | Unit             |
|---|--|--------------------|------------------|
| Supply voltage (overvoltage protection see page 4)  | $V_{bb}$   | 43                 | V                |
| Supply voltage for full short circuit protection<br>$T_{j,start} = -40 \dots +150^\circ\text{C}$  | $V_{bb}$   | 34                 | V                |
| Load current (Short-circuit current, see page 5)  | $I_L$  | self-limited       | A                |
| Load dump protection <sup>2)</sup> $V_{LoadDump} = U_A + V_S$ , $U_A = 13.5\text{ V}$<br>$R_l^3) = 2\ \Omega$ , $t_d = 200\text{ ms}$ ; IN = low or high,<br>each channel loaded with $R_L = 4.7\ \Omega$ ,   | $V_{Load\ dump}^{4)}$                                    | 60                 | V                |
| Operating temperature range   | $T_j$  | -40 ... +150       | $^\circ\text{C}$ |
| Storage temperature range   | $T_{stg}$  | -55 ... +150       |                  |
| Power dissipation (DC) <sup>5)</sup><br>(all channels active)   | $T_a = 25^\circ\text{C}$ :<br>$T_a = 85^\circ\text{C}$ : | $P_{tot}$          | 3.7<br>1.9<br>W  |
| Inductive load switch-off energy dissipation, single pulse<br>$V_{bb} = 12\text{V}$ , $T_{j,start} = 150^\circ\text{C}^{5)}$ ,<br>$I_L = 2.9\text{ A}$ , $Z_L = 58\text{ mH}$ , $0\ \Omega$ one channel:<br>$I_L = 4.3\text{ A}$ , $Z_L = 58\text{ mH}$ , $0\ \Omega$ two parallel channels:<br>$I_L = 6.3\text{ A}$ , $Z_L = 58\text{ mH}$ , $0\ \Omega$ four parallel channels:<br>see diagrams on page 9 and page 10 | $E_{AS}$   | 0.3<br>0.65<br>1.5 | J                |
| Electrostatic discharge capability (ESD)<br>(Human Body Model)  | $V_{ESD}$  | 1.0                | kV               |
| Input voltage (DC)  | $V_{IN}$   | -10 ... +16        | V                |
| Current through input pin (DC)  | $I_{IN}$   | $\pm 2.0$          | mA               |
| Current through status pin (DC)<br>see internal circuit diagram page 8  | $I_{ST}$   | $\pm 5.0$          |                  |
| Thermal resistance<br>junction - soldering point <sup>5),6)</sup> each channel:<br>junction - ambient <sup>5)</sup> one channel active:<br>all channels active:   | $R_{thjs}$<br>$R_{thja}$                                 | 15<br>41<br>34     | K/W              |

2) Supply voltages higher than  $V_{bb(AZ)}$  require an external current limit for the GND and status pins, e.g. with a  $150\ \Omega$  resistor in the GND connection and a  $15\text{ k}\Omega$  resistor in series with the status pin. A resistor for input protection is integrated.

3)  $R_l$  = internal resistance of the load dump test pulse generator

4)  $V_{Load\ dump}$  is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839

5) Device on  $50\text{mm} \times 50\text{mm} \times 1.5\text{mm}$  epoxy PCB FR4 with  $6\text{cm}^2$  (one layer,  $70\ \mu\text{m}$  thick) copper area for  $V_{bb}$  connection. PCB is vertical without blown air. See page 15

6) Soldering point: upper side of solder edge of device pin 15. See page 15

## Electrical Characteristics

| Parameter and Conditions, each of the four channels<br>at $T_j = 25^\circ\text{C}$ , $V_{bb} = 12\text{ V}$ unless otherwise specified | Symbol | Values |     |     | Unit |
|--|--------|--------|-----|-----|------|
|  |        | min    | typ | max |      |

### Load Switching Capabilities and Characteristics

|   |                       |                   |                   |            |                        |
|---|-----------------------|-------------------|-------------------|------------|------------------------|
| On-state resistance ( $V_{bb}$ to OUT)<br>$I_L = 2\text{ A}$ each channel, $T_j = 25^\circ\text{C}$ :<br>$T_j = 150^\circ\text{C}$ :<br><br>two parallel channels, $T_j = 25^\circ\text{C}$ :<br>four parallel channels, $T_j = 25^\circ\text{C}$ : | $R_{ON}$              | --                | 85<br>170         | 100<br>200 | $\text{m}\Omega$       |
| Nominal load current one channel active:<br>two parallel channels active:<br>four parallel channels active:<br>Device on PCB <sup>5)</sup> , $T_a = 85^\circ\text{C}$ , $T_j \leq 150^\circ\text{C}$  | $I_{L(NOM)}$          | 2.5<br>3.8<br>5.9 | 2.9<br>4.3<br>6.3 | --         | A                      |
| Output current while GND disconnected or pulled up; $V_{bb} = 30\text{ V}$ , $V_{IN} = 0$ , see diagram page 9  | $I_{L(GNDhigh)}$      | --                | --                | 10         | mA                     |
| Turn-on time to 90% $V_{OUT}$ :<br>Turn-off time to 10% $V_{OUT}$ :<br>$R_L = 12\ \Omega$ , $T_j = -40\dots+150^\circ\text{C}$  | $t_{on}$<br>$t_{off}$ | 80<br>80          | 200<br>200        | 400<br>400 | $\mu\text{s}$          |
| Slew rate on<br>10 to 30% $V_{OUT}$ , $R_L = 12\ \Omega$ , $T_j = -40\dots+150^\circ\text{C}$ :   | $dV/dt_{on}$          | 0.1               | --                | 1          | $\text{V}/\mu\text{s}$ |
| Slew rate off<br>70 to 40% $V_{OUT}$ , $R_L = 12\ \Omega$ , $T_j = -40\dots+150^\circ\text{C}$ :  | $-dV/dt_{off}$        | 0.1               | --                | 1          | $\text{V}/\mu\text{s}$ |

### Operating Parameters

|  |                        |     |          |            |               |
|--|------------------------|-----|----------|------------|---------------|
| Operating voltage <sup>7)</sup> $T_j = -40\dots+150^\circ\text{C}$ :                                     | $V_{bb(on)}$           | 5.0 | --       | 34         | V             |
| Undervoltage shutdown $T_j = -40\dots+150^\circ\text{C}$ :   | $V_{bb(under)}$        | 3.5 | --       | 5.0        | V             |
| Undervoltage restart $T_j = -40\dots+25^\circ\text{C}$ :<br>$T_j = +150^\circ\text{C}$ :                 | $V_{bb(u\ rst)}$       | --  | --       | 5.0<br>7.0 | V             |
| Undervoltage restart of charge pump<br>see diagram page 14 $T_j = -40\dots+150^\circ\text{C}$ :          | $V_{bb(ucp)}$          | --  | 5.6      | 7.0        | V             |
| Undervoltage hysteresis<br>$\Delta V_{bb(under)} = V_{bb(u\ rst)} - V_{bb(under)}$                       | $\Delta V_{bb(under)}$ | --  | 0.2      | --         | V             |
| Overvoltage shutdown $T_j = -40\dots+150^\circ\text{C}$ :  | $V_{bb(over)}$         | 34  | --       | 43         | V             |
| Overvoltage restart $T_j = -40\dots+150^\circ\text{C}$ :   | $V_{bb(o\ rst)}$       | 33  | --       | --         | V             |
| Overvoltage hysteresis $T_j = -40\dots+150^\circ\text{C}$ :  | $\Delta V_{bb(over)}$  | --  | 0.5      | --         | V             |
| Overvoltage protection <sup>8)</sup> $T_j = -40\dots+150^\circ\text{C}$ :<br>$I_{bb} = 40\text{ mA}$     | $V_{bb(AZ)}$           | 42  | 47       | --         | V             |
| Standby current, all channels off $T_j = 25^\circ\text{C}$ :<br>$V_{IN} = 0$ $T_j = 150^\circ\text{C}$ : | $I_{bb(off)}$          | --  | 28<br>44 | 60<br>70   | $\mu\text{A}$ |

7) At supply voltage increase up to  $V_{bb} = 5.6\text{ V}$  typ without charge pump,  $V_{OUT} \approx V_{bb} - 2\text{ V}$

8) see also  $V_{ON(CL)}$  in circuit diagram on page 8.

| Parameter and Conditions, each of the four channels<br>at $T_j = 25\text{ °C}$ , $V_{bb} = 12\text{ V}$ unless otherwise specified  | Symbol       | Values   |        |         | Unit          |
|---|--------------|----------|--------|---------|---------------|
|   |              | min      | typ    | max     |               |
| Leakage output current (included in $I_{bb(off)}$ )<br>$V_{IN} = 0$   | $I_{L(off)}$ | --       | --     | 12      | $\mu\text{A}$ |
| Operating current <sup>9)</sup> , $V_{IN} = 5\text{ V}$ , $T_j = -40\dots+150\text{ °C}$<br>$I_{GND} = I_{GND1/2} + I_{GND3/4}$ ,<br>one channel on:<br>four channels on: | $I_{GND}$    | --<br>-- | 2<br>8 | 3<br>12 | mA            |

### Protection Functions<sup>10)</sup>

|  |                 |                |                                       |                |             |
|--|-----------------|----------------|---------------------------------------|----------------|-------------|
| Initial peak short circuit current limit, (see timing diagrams, page 12)<br><br>each channel, $T_j = -40\text{ °C}$ :<br>$T_j = 25\text{ °C}$ :<br>$T_j = +150\text{ °C}$ :<br><br>two parallel channels<br>four parallel channels | $I_{L(SCp)}$    | 11<br>9<br>5   | 18<br>14<br>8                         | 25<br>22<br>14 | A           |
|  |                 |                | twice the current of one channel      |                |             |
|  |                 |                | four times the current of one channel |                |             |
| Repetitive short circuit current limit,<br>$T_j = T_{jt}$<br><br>each channel<br>two parallel channels<br>four parallel channels<br><br>(see timing diagrams, page 12)   | $I_{L(SCr)}$    | --<br>--<br>-- | 8<br>8<br>8                           | --<br>--<br>-- | A           |
| Initial short circuit shutdown time<br>$T_{j,start} = -40\text{ °C}$ :<br>$T_{j,start} = 25\text{ °C}$ :<br><br>(see page 12 and timing diagrams on page 12)   | $t_{off(SC)}$   | --<br>--       | 3.8<br>3                              | --<br>--       | ms          |
| Output clamp (inductive load switch off) <sup>11)</sup><br>at $V_{ON(CL)} = V_{bb} - V_{OUT}$  | $V_{ON(CL)}$    | --             | 47                                    | --             | V           |
| Thermal overload trip temperature  | $T_{jt}$        | 150            | --                                    | --             | $\text{°C}$ |
| Thermal hysteresis   | $\Delta T_{jt}$ | --             | 10                                    | --             | K           |

### Reverse Battery

|   |           |    |     |    |    |
|---|-----------|----|-----|----|----|
| Reverse battery voltage <sup>12)</sup>  | $-V_{bb}$ | -- | --  | 32 | V  |
| Drain-source diode voltage ( $V_{out} > V_{bb}$ )<br>$I_L = -2.9\text{ A}$ , $T_j = +150\text{ °C}$ | $-V_{ON}$ | -- | 610 | -- | mV |

9) Add  $I_{ST}$ , if  $I_{ST} > 0$

10) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

11) If channels are connected in parallel, output clamp is usually accomplished by the channel with the lowest  $V_{ON(CL)}$



12) Requires a 150  $\Omega$  resistor in GND connection. The reverse load current through the intrinsic drain-source diode has to be limited by the connected load. Note that the power dissipation is higher compared to normal operating conditions due to the voltage drop across the intrinsic drain-source diode. The temperature protection is not active during reverse current operation! Input and Status currents have to be limited (see max. ratings page 3 and circuit page 8).

| Parameter and Conditions, each of the four channels<br>at $T_j = 25^\circ\text{C}$ , $V_{bb} = 12\text{ V}$ unless otherwise specified | Symbol | Values |     |     | Unit |
|--|--------|--------|-----|-----|------|
|  |        | min    | typ | max |      |

**Diagnostic Characteristics**

|  |               |                |                |                   |            |
|--|---------------|----------------|----------------|-------------------|------------|
| Open load detection current, (on-condition)<br>each channel, $T_j = -40^\circ\text{C}$ :<br>$T_j = 25^\circ\text{C}$ :<br>$T_j = 150^\circ\text{C}$ :<br>two parallel channels<br>four parallel channels | $I_{L(OL)}$   | 20<br>20<br>20 | --<br>--<br>-- | 400<br>300<br>300 | mA         |
| Open load detection voltage <sup>13)</sup> $T_j = -40..+150^\circ\text{C}$ :   | $V_{OUT(OL)}$ | 2              | 3              | 4                 | V          |
| Internal output pull down<br>(OUT to GND), $V_{OUT} = 5\text{ V}$ $T_j = -40..+150^\circ\text{C}$ :  | $R_O$         | 4              | 10             | 30                | k $\Omega$ |

**Input and Status Feedback<sup>14)</sup>**

|  |                                 |                 |                 |                  |               |
|--|---------------------------------|-----------------|-----------------|------------------|---------------|
| Input resistance<br>(see circuit page 8) $T_j = -40..+150^\circ\text{C}$ :   | $R_I$                           | 2.5             | 3.5             | 6                | k $\Omega$    |
| Input turn-on threshold voltage  $T_j = -40..+150^\circ\text{C}$ :  | $V_{IN(T+)}$                    | 1.7             | --              | 3.5              | V             |
| Input turn-off threshold voltage  $T_j = -40..+150^\circ\text{C}$ :  | $V_{IN(T-)}$                    | 1.5             | --              | --               | V             |
| Input threshold hysteresis   | $\Delta V_{IN(T)}$              | --              | 0.5             | --               | V             |
| Off state input current $V_{IN} = 0.4\text{ V}$ :<br>$T_j = -40..+150^\circ\text{C}$ :   | $I_{IN(off)}$                   | 1               | --              | 50               | $\mu\text{A}$ |
| On state input current $V_{IN} = 5\text{ V}$ :<br>$T_j = -40..+150^\circ\text{C}$ :  | $I_{IN(on)}$                    | 20              | 50              | 90               | $\mu\text{A}$ |
| Delay time for status with open load after switch<br>off (other channel in off state)<br>(see timing diagrams, page 14), $T_j = -40..+150^\circ\text{C}$ :   | $t_{d(ST\ OL4)}$                | 100             | 320             | 800              | $\mu\text{s}$ |
| Delay time for status with open load after switch<br>off (other channel in on state)<br>(see timing diagrams, page 14), $T_j = -40..+150^\circ\text{C}$ :  | $t_{d(ST\ OL5)}$                | --              | 5               | 20               | $\mu\text{s}$ |
| Status invalid after positive input slope<br>(open load) $T_j = -40..+150^\circ\text{C}$ :   | $t_{d(ST)}$                     | --              | 200             | 600              | $\mu\text{s}$ |
| Status output (open drain)<br>Zener limit voltage $T_j = -40..+150^\circ\text{C}$ , $I_{ST} = +1.6\text{ mA}$ :<br>ST low voltage $T_j = -40..+25^\circ\text{C}$ , $I_{ST} = +1.6\text{ mA}$ :<br>$T_j = +150^\circ\text{C}$ , $I_{ST} = +1.6\text{ mA}$ : | $V_{ST(high)}$<br>$V_{ST(low)}$ | 5.4<br>--<br>-- | 6.1<br>--<br>-- | --<br>0.4<br>0.6 | V             |

<sup>13)</sup> External pull up resistor required for open load detection in off state.

<sup>14)</sup> If ground resistors  $R_{GND}$  are used, add the voltage drop across these resistors.

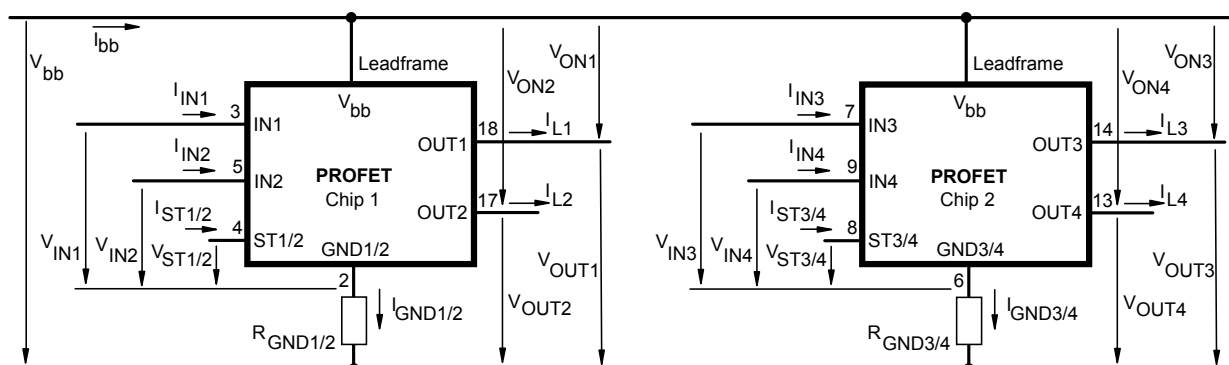
## Truth Table

| Channel 1 and 2                                    | Chip 1        | IN1 | IN2 | OUT1 | OUT2 | ST1/2               |
|--|---------------|-----|-----|------|------|---------------------|
| Channel 3 and 4<br>(equivalent to channel 1 and 2) | Chip 2        | IN3 | IN4 | OUT3 | OUT4 | ST3/4               |
| <b>BTS 721L1</b>                                   |               |     |     |      |      |                     |
| <b>Normal operation</b>                            |               | L   | L   | L    | L    | H                   |
|  |               | L   | H   | L    | H    | H                   |
|  |               | H   | L   | H    | L    | H                   |
|  |               | H   | H   | H    | H    | H                   |
| <b>Open load</b>                                   | Channel 1 (3) | L   | L   | Z    | L    | H(L <sup>15</sup> ) |
|  |               | L   | H   | Z    | H    | H                   |
|  |               | H   | X   | H    | X    | L                   |
|  | Channel 2 (4) | L   | L   | L    | Z    | H(L <sup>15</sup> ) |
|  |               | H   | L   | H    | Z    | H                   |
|  |               | X   | H   | X    | H    | L                   |
| <b>Short circuit to V<sub>bb</sub></b>             | Channel 1 (3) | L   | L   | H    | L    | L <sup>16</sup>     |
|  |               | L   | H   | H    | H    | H                   |
|  |               | H   | X   | H    | X    | H(L <sup>17</sup> ) |
|  | Channel 2 (4) | L   | L   | L    | H    | L <sup>16</sup>     |
|  |               | H   | L   | H    | H    | H                   |
|  |               | X   | H   | X    | H    | H(L <sup>17</sup> ) |
| <b>Overtemperature</b>                             | both channel  | L   | L   | L    | L    | H                   |
|  |               | X   | H   | L    | L    | L                   |
|  |               | H   | X   | L    | L    | L                   |
|  | Channel 1 (3) | L   | X   | L    | X    | H                   |
|  |               | H   | X   | L    | X    | L                   |
|  | Channel 2 (4) | X   | L   | X    | L    | H                   |
| X  |               | H   | X   | L    | L    |                     |
| <b>Undervoltage/ Overvoltage</b>                   |               | X   | X   | L    | L    | H                   |

L = "Low" Level      X = don't care      Z = high impedance, potential depends on external circuit  
H = "High" Level      Status signal valid after the time delay shown in the timing diagrams

Parallel switching of channel 1 and 2 (also channel 3 and 4) is easily possible by connecting the inputs and outputs in parallel (see truth table). If switching channel 1 to 4 in parallel, the status outputs ST1/2 and ST3/4 have to be configured as a 'Wired OR' function with a single pull-up resistor.

## Terms

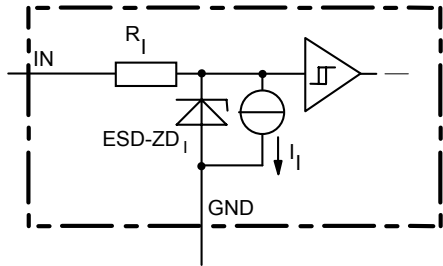


Leadframe ( $V_{bb}$ ) is connected to pin 1,10,11,12,15,16,19,20

External  $R_{GND}$  optional; two resistors  $R_{GND1/2}$ ,  $R_{GND3/4} = 150 \Omega$  or a single resistor  $R_{GND} = 75 \Omega$  for reverse battery protection up to the max. operating voltage.

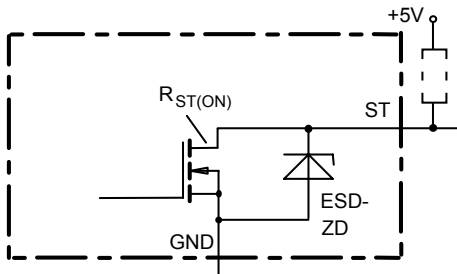
- 15) With additional external pull up resistor  
16) An external short of output to  $V_{bb}$  in the off state causes an internal current from output to ground. If  $R_{GND}$  is used, an offset voltage at the GND and ST pins will occur and the  $V_{ST\ low}$  signal may be erroneous.  
17) Low resistance to  $V_{bb}$  may be detected by no-load-detection

**Input circuit (ESD protection), IN1...4**



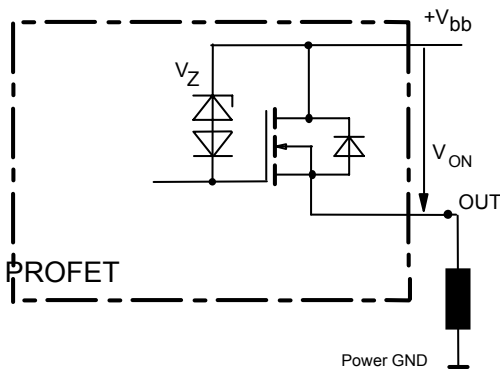
ESD zener diodes are not to be used as voltage clamp at DC conditions. Operation in this mode may result in a drift of the zener voltage (increase of up to 1 V).

**Status output, ST1/2 or ST3/4**



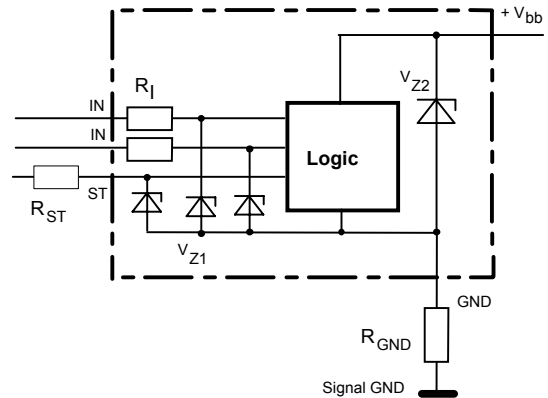
ESD-Zener diode: 6.1 V typ., max 5.0 mA;  $R_{ST(ON)} < 380 \Omega$  at 1.6 mA, ESD zener diodes are not to be used as voltage clamp at DC conditions. Operation in this mode may result in a drift of the zener voltage (increase of up to 1 V).

**Inductive and overvoltage output clamp, OUT1...4**



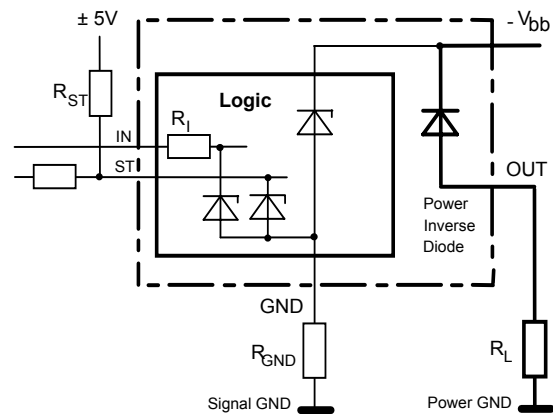
$V_{ON}$  clamped to  $V_{ON(CL)} = 47 \text{ V typ.}$

**Overvoltage protection of logic part  
GND1/2 or GND3/4**



$V_{Z1} = 6.1 \text{ V typ.}$ ,  $V_{Z2} = 47 \text{ V typ.}$ ,  $R_1 = 3.5 \text{ k}\Omega \text{ typ.}$ ,  $R_{GND} = 150 \Omega$

**Reverse battery protection**



$R_{GND} = 150 \Omega$ ,  $R_1 = 3.5 \text{ k}\Omega \text{ typ.}$

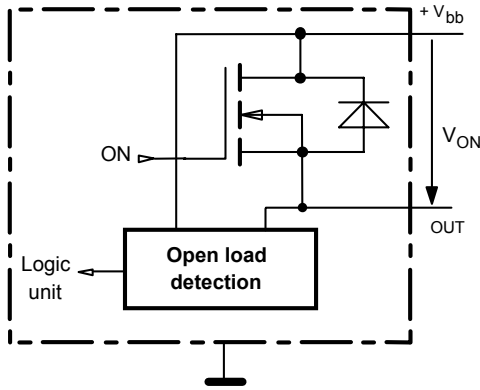
Temperature protection is not active during inverse current operation.



**Open-load detection, OUT1...4**

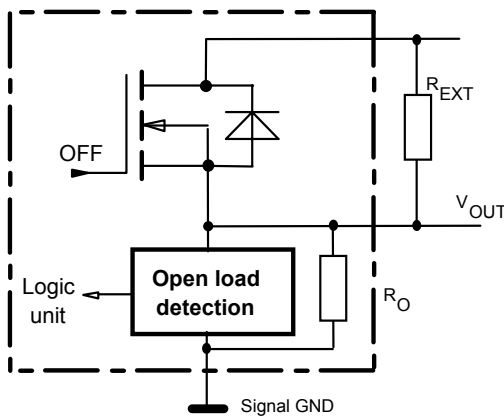
ON-state diagnostic condition:

$$V_{ON} < R_{ON} \cdot I_{L(OL)}; \text{IN high}$$



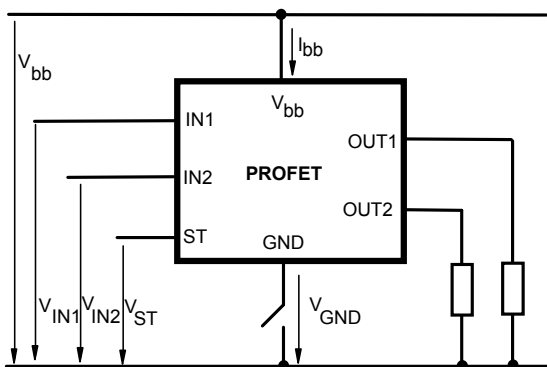
OFF-state diagnostic condition:

$$V_{OUT} > 3 \text{ V typ.}; \text{IN low}$$



**GND disconnect**

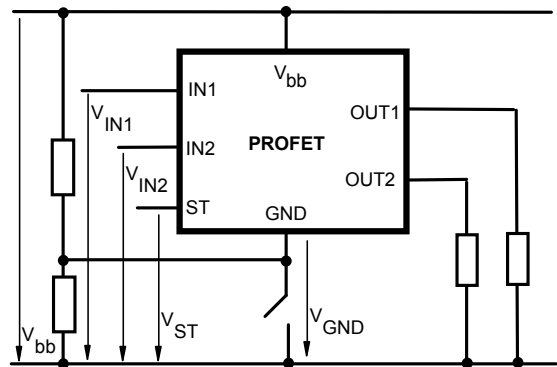
(channel 1/2 or 3/4)



Any kind of load. In case of IN=high is  $V_{OUT} \approx V_{IN} - V_{IN(T+)}$ .  
Due to  $V_{GND} > 0$ , no  $V_{ST} = \text{low}$  signal available.

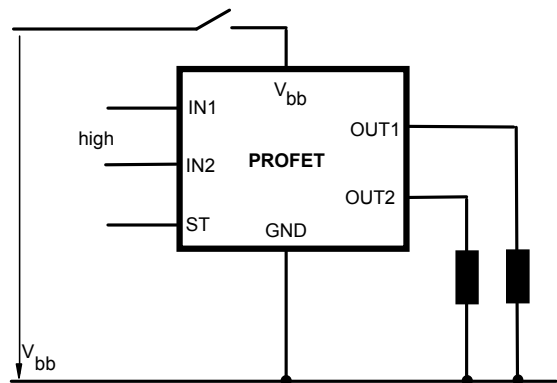
**GND disconnect with GND pull up**

(channel 1/2 or 3/4)



Any kind of load. If  $V_{GND} > V_{IN} - V_{IN(T+)}$  device stays off  
Due to  $V_{GND} > 0$ , no  $V_{ST} = \text{low}$  signal available.

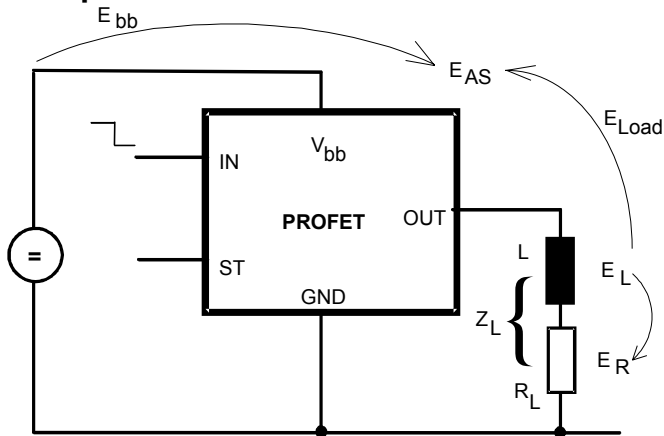
**V<sub>bb</sub> disconnect with energized inductive load**



For an inductive load current up to the limit defined by  $E_{AS}$  (max. ratings see page 3 and diagram on page 10) each switch is protected against loss of  $V_{bb}$ .

Consider at your PCB layout that in the case of  $V_{bb}$  disconnection with energized inductive load the whole load current flows through the GND connection.

**Inductive load switch-off energy dissipation**



Energy stored in load inductance:

$$E_L = 1/2 \cdot L \cdot I_L^2$$

While demagnetizing load inductance, the energy dissipated in PROFET is

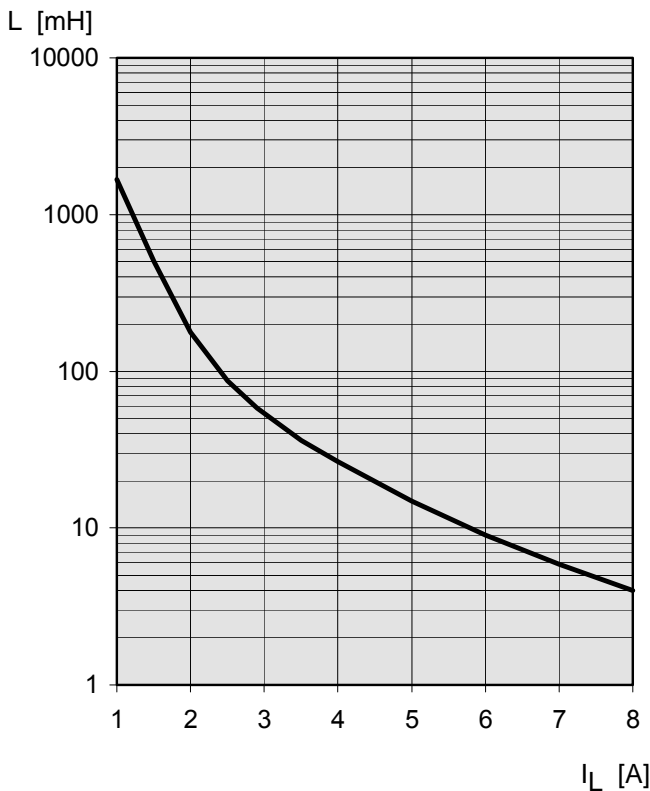
$$E_{AS} = E_{bb} + E_L - E_R = \int V_{ON(CL)} \cdot i_L(t) dt,$$

with an approximate solution for  $R_L > 0 \Omega$ :

$$E_{AS} = \frac{I_L \cdot L}{2 \cdot R_L} (V_{bb} + |V_{OUT(CL)}|) \ln \left( 1 + \frac{I_L \cdot R_L}{|V_{OUT(CL)}|} \right)$$

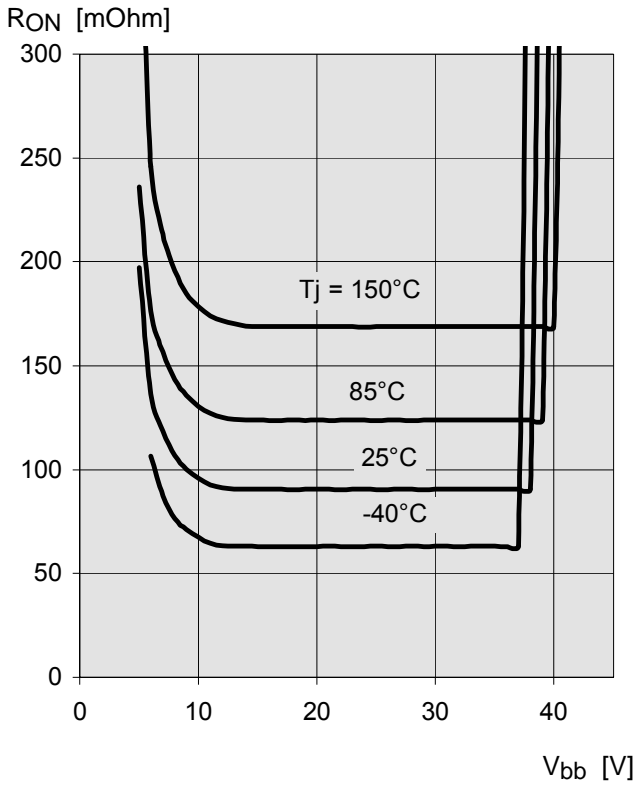
**Maximum allowable load inductance for a single switch off** (one channel)<sup>5)</sup>

$L = f(I_L)$ ;  $T_{j,start} = 150^\circ\text{C}$ ,  $V_{bb} = 12\text{ V}$ ,  $R_L = 0 \Omega$



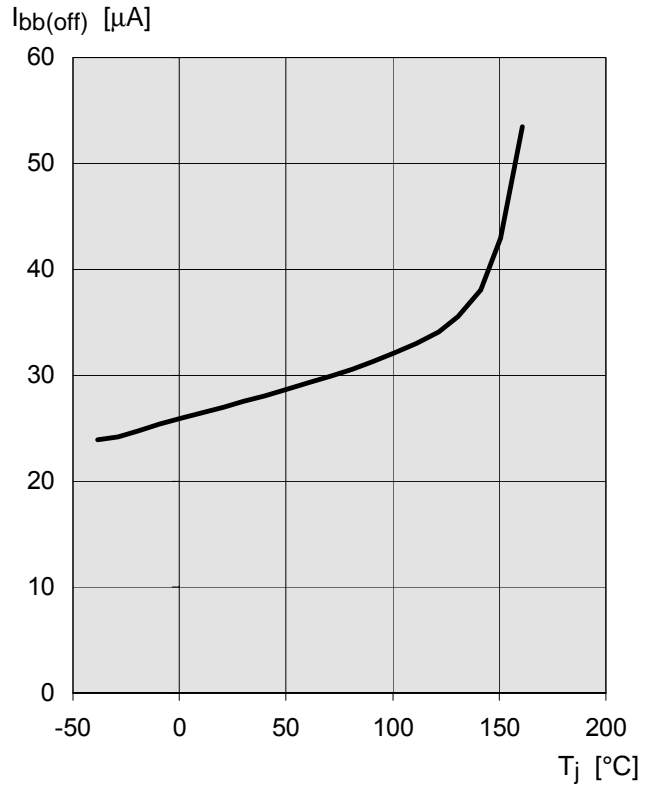
**Typ. on-state resistance**

$R_{ON} = f(V_{bb}, T_j)$ ;  $I_L = 2\text{ A}$ ,  $I_N = \text{high}$



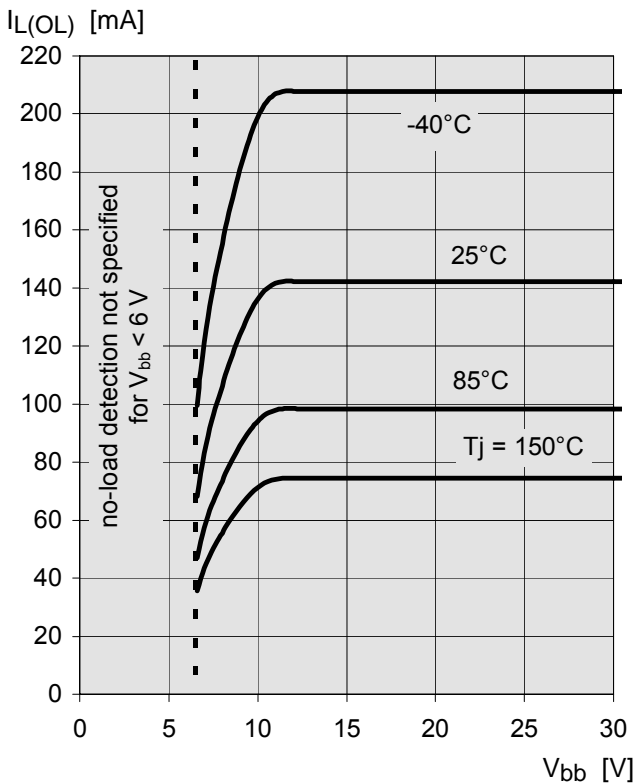
**Typ. standby current**

$I_{bb(off)} = f(T_j)$ ;  $V_{bb} = 9...34\text{ V}$ ,  $I_{N1...4} = \text{low}$



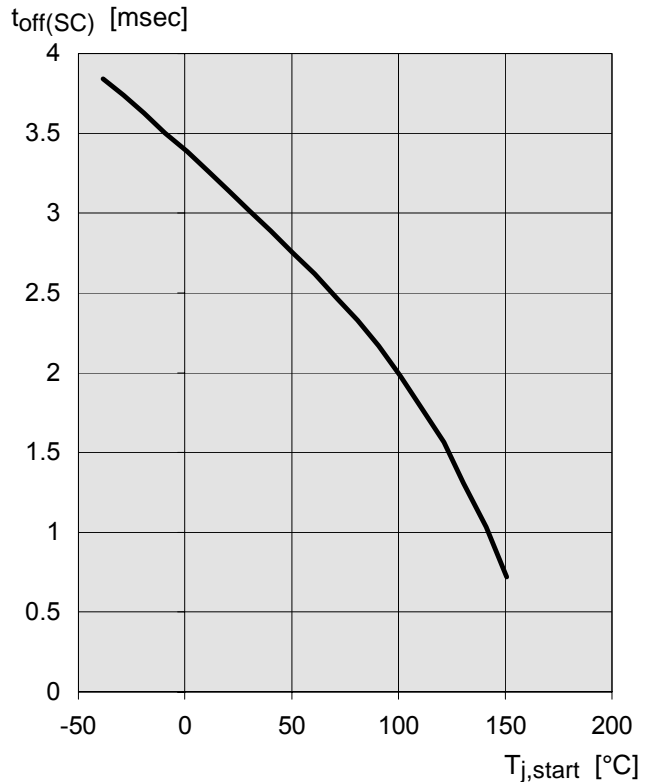
**Typ. open load detection current**

$I_{L(OL)} = f(V_{bb}, T_j)$ ;  $I_N = \text{high}$



**Typ. initial short circuit shutdown time**

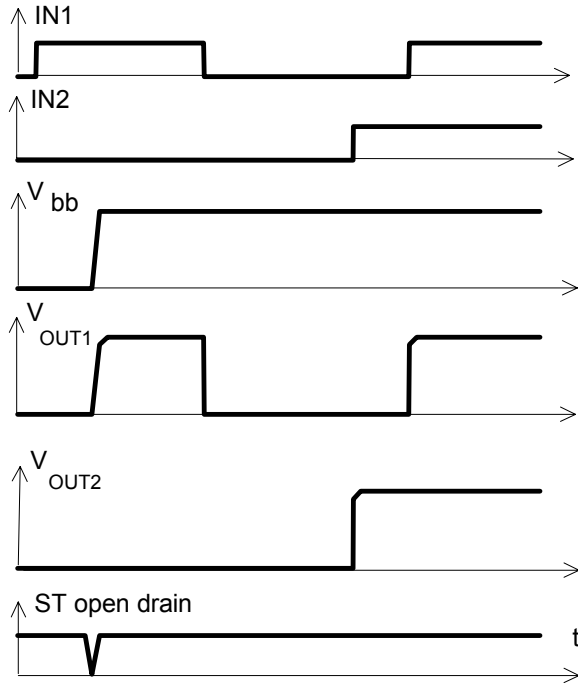
$t_{off(SC)} = f(T_{j,start})$ ;  $V_{bb} = 12\text{ V}$



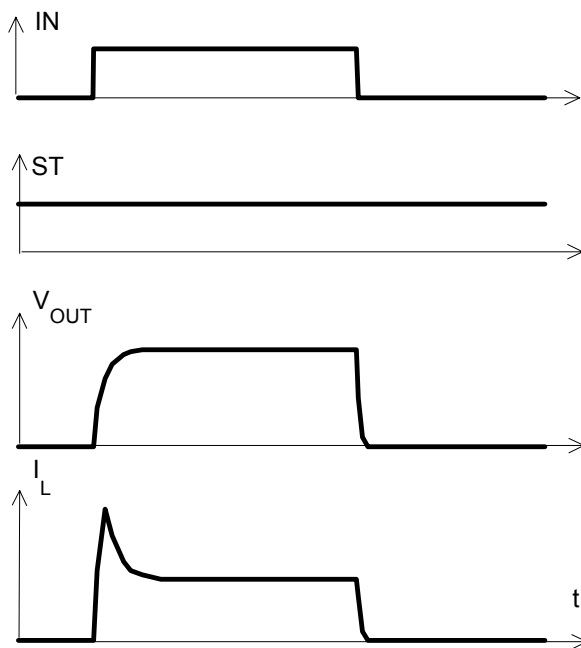
## Timing diagrams

Timing diagrams are shown for chip 1 (channel 1/2). For chip 2 (channel 3/4) the diagrams are valid too. The channels 1 and 2, respectively 3 and 4, are symmetric and consequently the diagrams are valid for each channel as well as for permuted channels

**Figure 1a:**  $V_{bb}$  turn on:

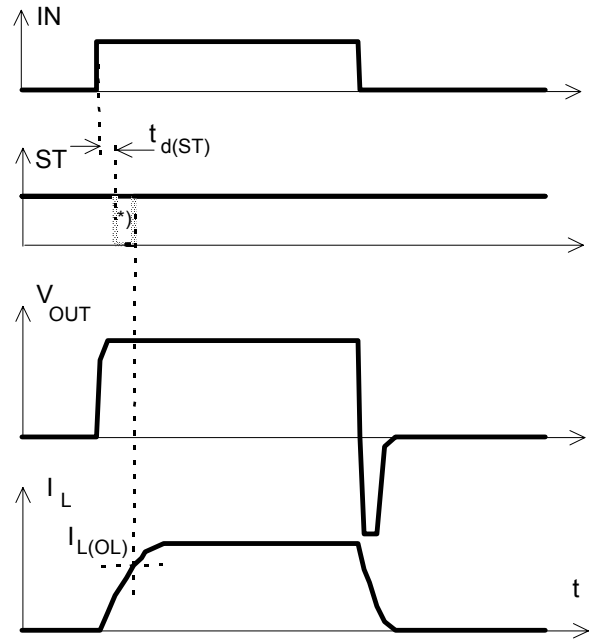


**Figure 2a:** Switching a lamp:



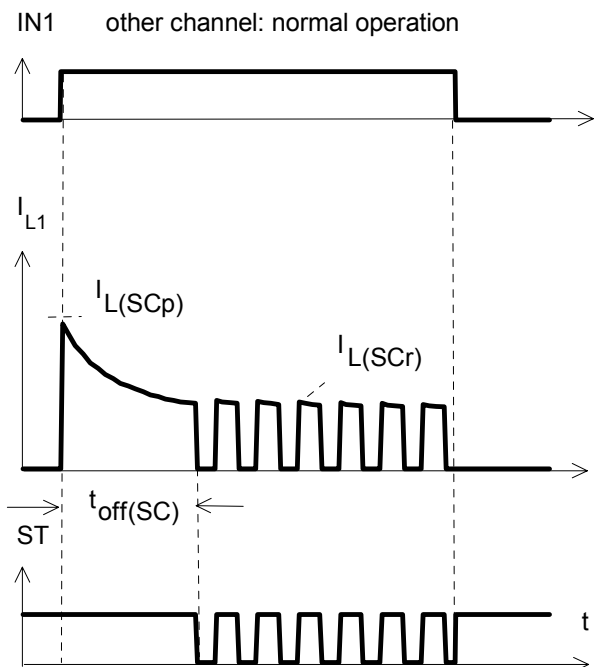
The initial peak current should be limited by the lamp and not by the initial short circuit current  $I_{L(SCp)} = 14 \text{ A}$  typ. of the device.

**Figure 2b:** Switching an inductive load



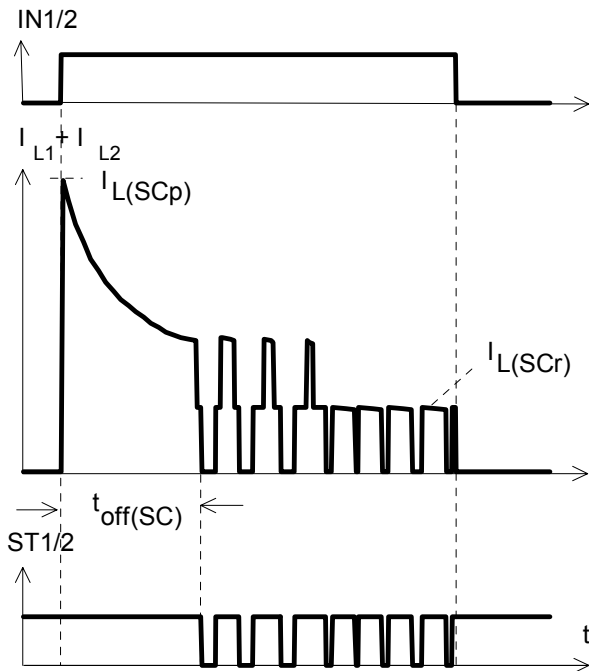
\*) if the time constant of load is too large, open-load-status may occur

**Figure 3a:** Turn on into short circuit: shut down by overtemperature, restart by cooling

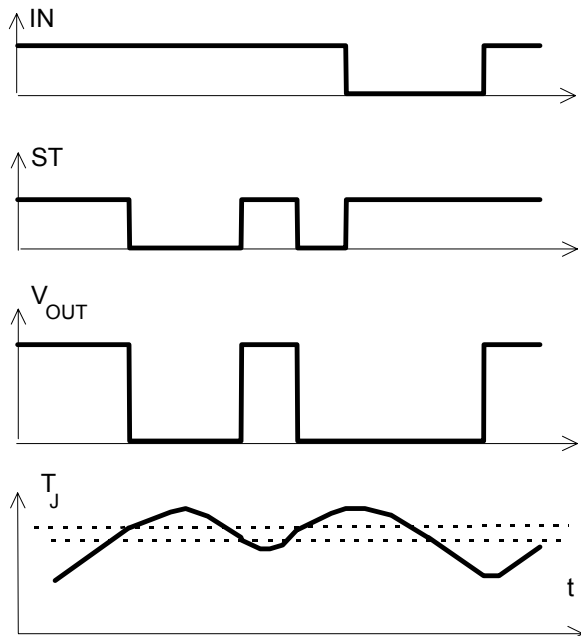


Heating up of the chip may require several milliseconds, depending on external conditions ( $t_{off(SC)}$  vs.  $T_{j,start}$  see page 12)

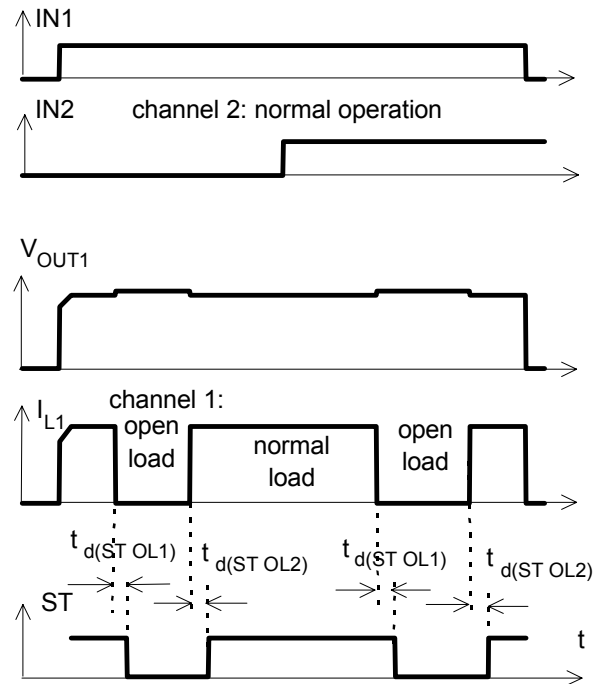
**Figure 3b:** Turn on into short circuit: shut down by overtemperature, restart by cooling (two parallel switched channels 1 and 2)



**Figure 4a:** Overtemperature: Reset if  $T_j < T_{jt}$

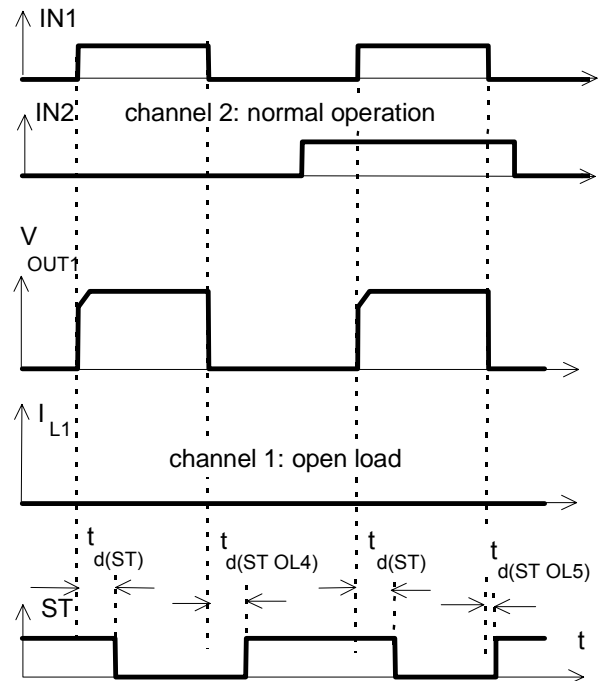


**Figure 5a:** Open load: detection in ON-state, open load occurs in on-state



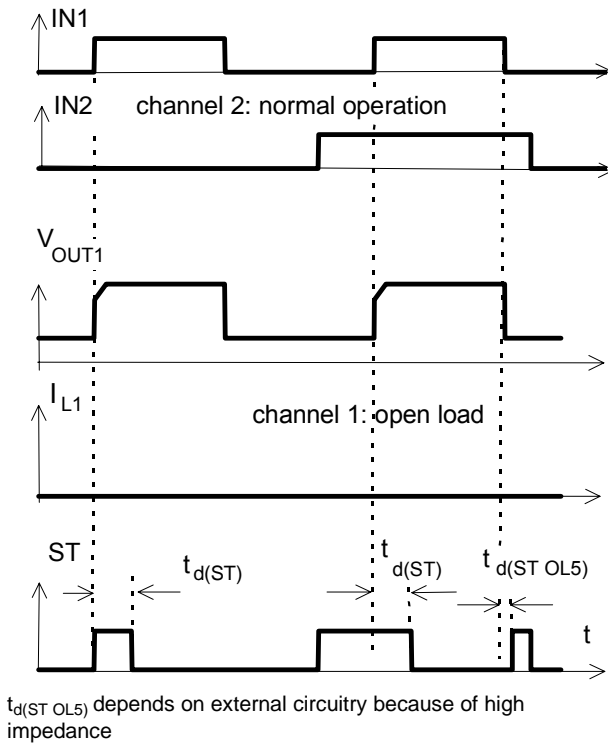
$t_{d(ST OL1)} = 30 \mu s$  typ.,  $t_{d(ST OL2)} = 20 \mu s$  typ

**Figure 5b:** Open load: detection in ON-state, turn on/off to open load

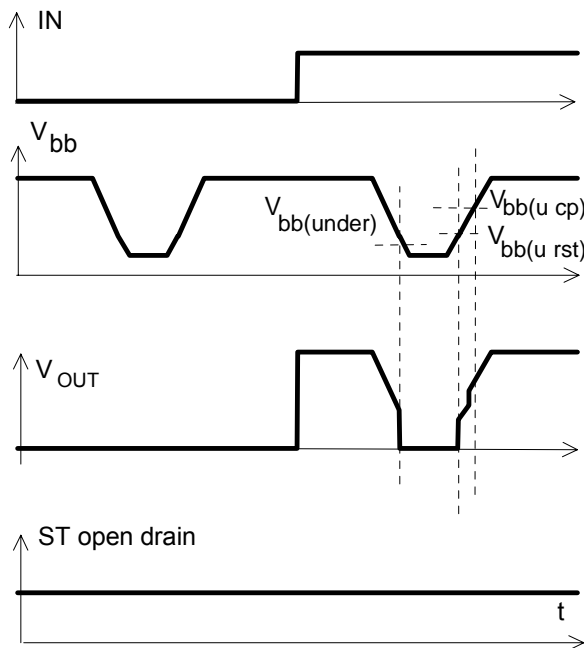


The status delay time  $t_{d(STOL4)}$  allows to distinguish between the failure modes "open load in ON-state" and "overtemperature".

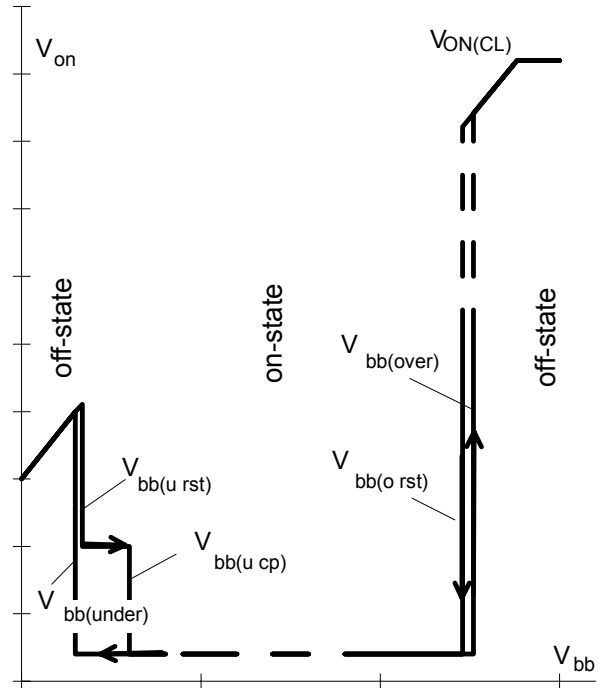
**Figure 5c:** Open load: detection in ON- and OFF-state (with R<sub>EXT</sub>), turn on/off to open load



**Figure 6a:** Undervoltage:

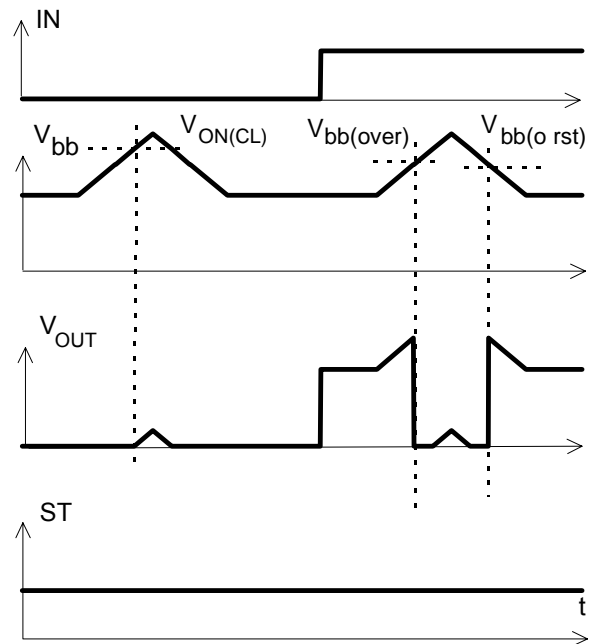


**Figure 6b:** Undervoltage restart of charge pump



IN = high, normal load conditions.  
Charge pump starts at  $V_{bb(ucp)} = 5.6 V$  typ.

**Figure 7a:** Overvoltage:

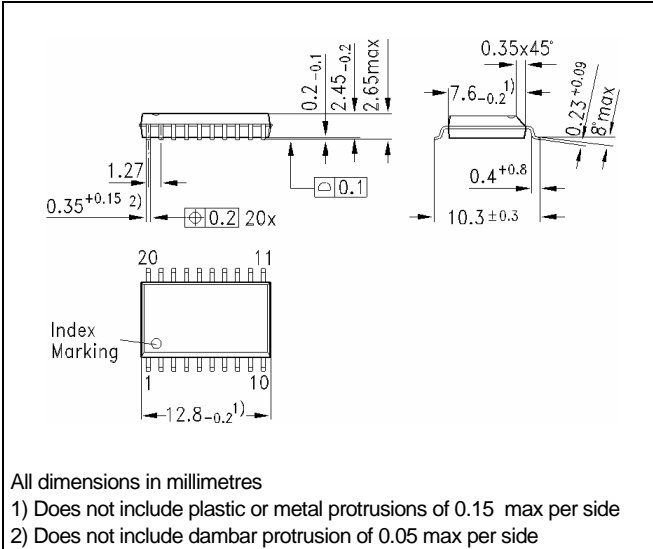


## Package and Ordering Code

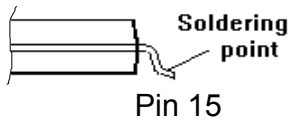
**Standard P-DSO-20-9**

Ordering Code

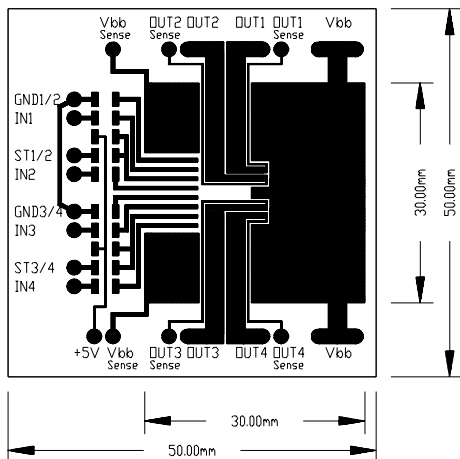
|          |                 |
|----------|-----------------|
| BTS721L1 | Q67060-S7002-A2 |
|----------|-----------------|



Definition of soldering point with temperature  $T_s$ :  
 upper side of solder edge of device pin 15.



Printed circuit board (FR4, 1.5mm thick, one layer 70µm, 6cm<sup>2</sup> active heatsink area) as a reference for max. power dissipation  $P_{tot}$ , nominal load current  $I_{L(NOM)}$  and thermal resistance  $R_{thja}$



**Published by**  
**Infineon Technologies AG,**  
**St.-Martin-Strasse 53,**  
**D-81669 München**  
**© Infineon Technologies AG 2001**  
**All Rights Reserved.**

**Attention please!**  
 The information herein is given to describe certain components and shall not be considered as a guarantee of characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

**Information**  
 For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

**Warnings**  
 Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.