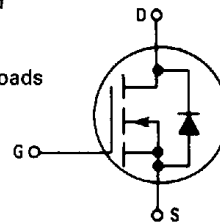


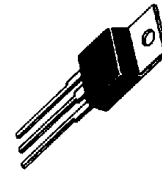
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA
Designer's Data Sheet
Power Field Effect Transistors
**N-Channel Enhancement-Mode
Silicon Gate**

This Logic Level TMOS Power FET is designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)} = 2$ Volts Max
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads


MTP15N08EL

Motorola Preferred Device

**TMOS POWER FET
LOGIC LEVEL
15 AMPERES
 $R_{DS(on)} = 0.135$ OHM
80 VOLTS**

 CASE 221A-06
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	80	Vdc
Drain-Gate Voltage ($R_{GS} = 1$ M Ω)	V_{DGR}	80	Vdc
Gate-Source Voltage — Continuous — Non-Repetitive ($t_p \leq 50$ μ s)	V_{GS}	± 15 ± 20	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	15 45	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Drain-Source Breakdown Voltage ($V_{GS} = 0, I_D = 250$ μ A)	$V_{(BR)DSS}$	80	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 80$ Volts, $V_{GS} = 0$) ($V_{DS} = 80$ Volts, $V_{GS} = 0, T_J = 125^\circ\text{C}$)	I_{DSS}	— —	1 50	μ Adc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design

Preferred device is a Motorola recommended choice for future use and best overall value.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS (continued)

Gate-Body Leakage Current, Forward ($V_{GSF} = 15\text{ Vdc}$, $V_{DS} = 0$)	I_{GSSF}	—	100	nAdc
Gate Body Leakage Current, Reverse ($V_{GSR} = 15\text{ Vdc}$, $V_{DS} = 0$)	I_{GSSR}	—	100	nAdc

ON CHARACTERISTICS

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 1\text{ mA}$) ($T_J = 100^\circ\text{C}$)	$V_{GS(th)}$	1 0.75	2 1.75	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 5\text{ Vdc}$, $I_D = 7.5\text{ Adc}$)	$R_{DS(on)}$	—	0.135	Ohm
Drain-Source On-Voltage ($V_{GS} = 5\text{ V}$) ($I_D = 15\text{ Adc}$) ($I_D = 7.5\text{ Adc}$, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	— —	2.5 1.5	Vdc
Forward Transconductance ($V_{DS} = 15\text{ V}$, $I_D = 7.5\text{ A}$)	g_{FS}	6	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1\text{ MHz}$	C_{iss}	750 (Typ)	—	pF
	$V_{GS} = 15\text{ V}$, $V_{DS} = 0$, $f = 1\text{ MHz}$ See Figure 8		2500 (Typ)	—	
Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1\text{ MHz}$	C_{rss}	65 (Typ)	—	pF
	$V_{GS} = 15\text{ V}$, $V_{DS} = 0$, $f = 1\text{ MHz}$ See Figure 8		1400 (Typ)	—	
Output Capacitance	$V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1\text{ MHz}$ See Figure 8	C_{oss}	240 (Typ)	—	pF

SWITCHING CHARACTERISTICS ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	$(V_{DD} = 25\text{ V}$, $I_D = 7.5\text{ A}$, $V_{GS} = 5\text{ V}$, $R_{gen} = 50\text{ ohms}$) See Figures 13 and 14	$t_{d(on)}$	16 (Typ)	—	ns
Rise Time		t_r	85 (Typ)	—	
Turn-Off Delay Time		$t_{d(off)}$	85 (Typ)	—	
Fall Time		t_f	75 (Typ)	—	
Total Gate Charge	$(V_{DD} = 60\text{ V}$, $I_D = 15\text{ A}$, $V_{GS} = 5\text{ Vdc}$) See Figures 9 and 10	Q_g	12.5 (Typ)	22	nC
Gate-Source Charge		Q_{gs}	2 (Typ)	—	
Gate-Drain Charge		Q_{gd}	6 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	$I_S = 15\text{ A}$, $V_{GS} = 0$	V_{SD}	1.06 (Typ)	1.2	Vdc
Forward Turn-On Time	$I_S = 15\text{ A}$, $dI_S/dt = 100\text{ A}/\mu\text{s}$, $V_R = 30\text{ V}$ See Figures 16 and 17	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	85 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_d	3.5 (Typ)	—	nH
		4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L_s	7.5 (Typ)	—	

Figure 1. On-Region Characteristics

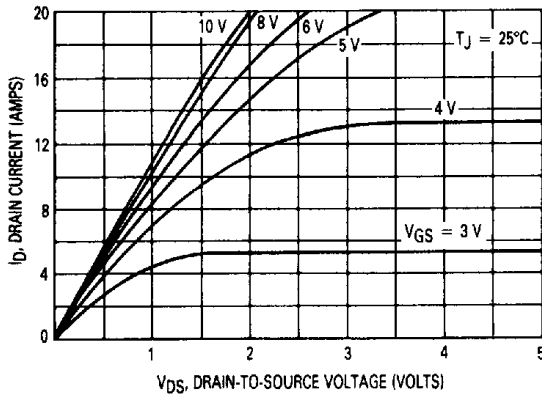


Figure 2. Gate-Threshold Voltage Variation With Temperature

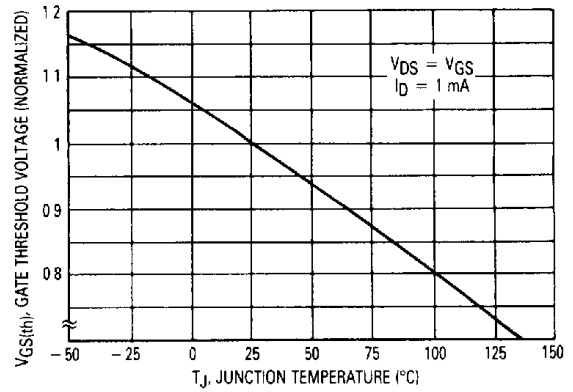


Figure 3. Transfer Characteristics

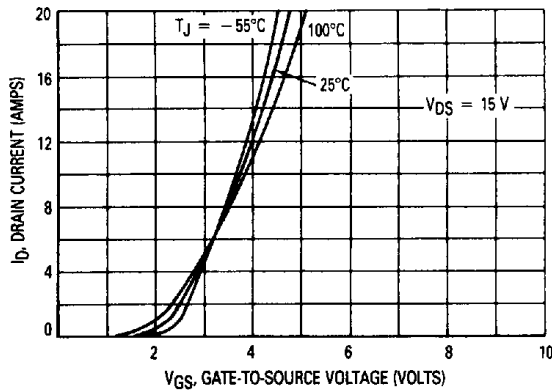


Figure 4. On-Resistance Variation With Drain Current

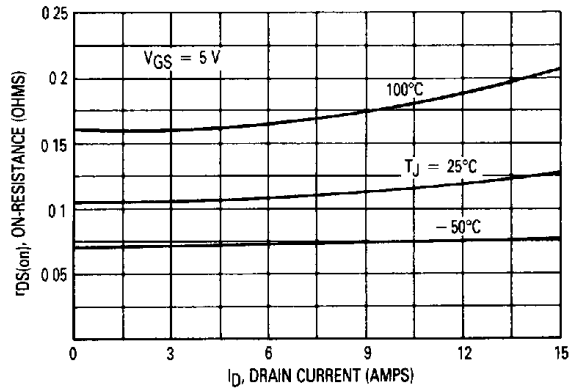


Figure 5. On-Resistance versus Gate-to-Source Voltage

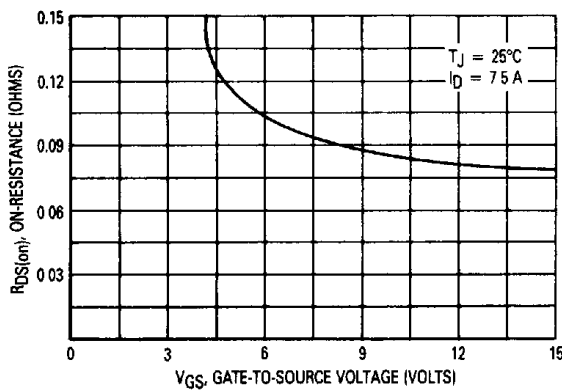


Figure 6. On-Resistance Variation With Temperature

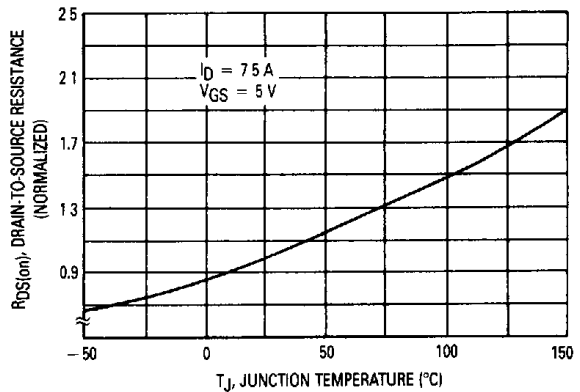


Figure 7. Drain-Source Breakdown Voltage Variation with Temperature

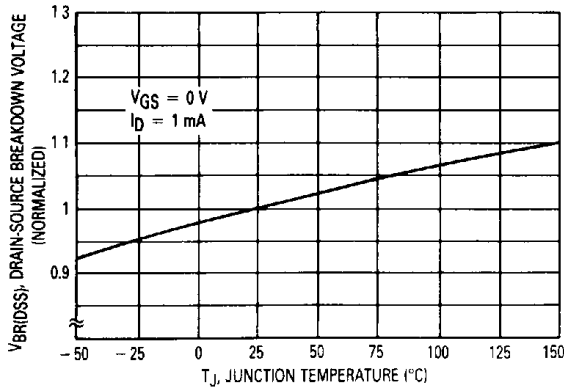


Figure 8. Capacitance Variation With Voltage

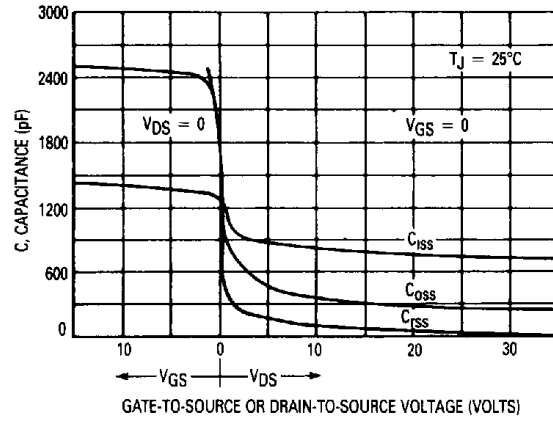


Figure 9. Gate Charge Test Circuit

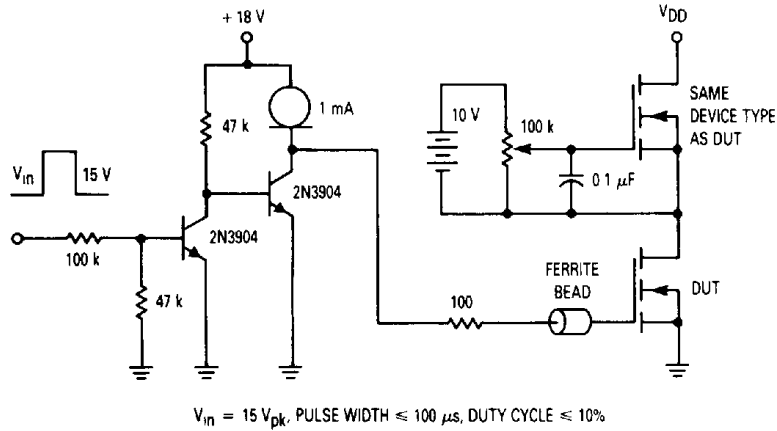


Figure 10. Gate Charge Variation

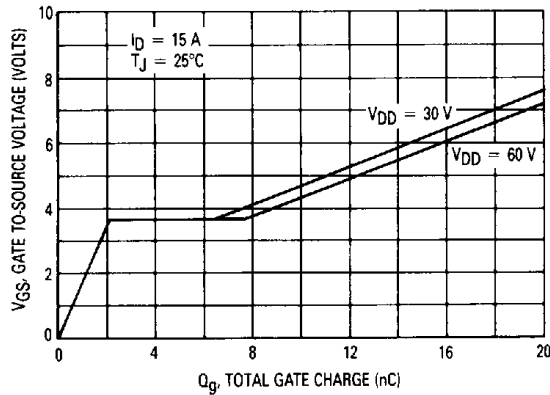
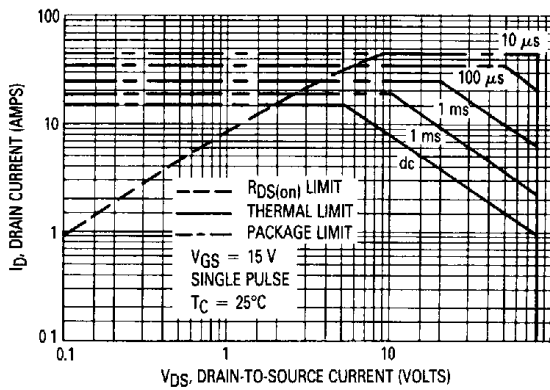


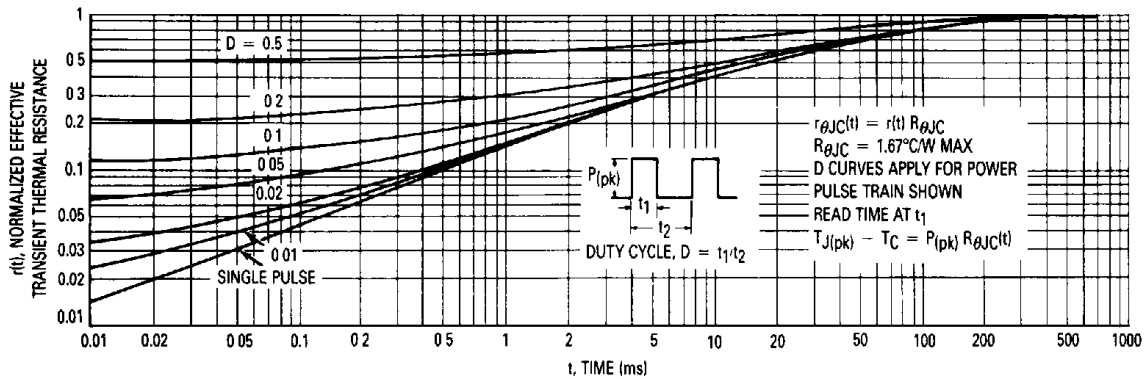
Figure 11. Maximum Rated Forward Biased Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

Figure 12. Thermal Response



RESISTIVE SWITCHING

Figure 13. Switching Test Circuit

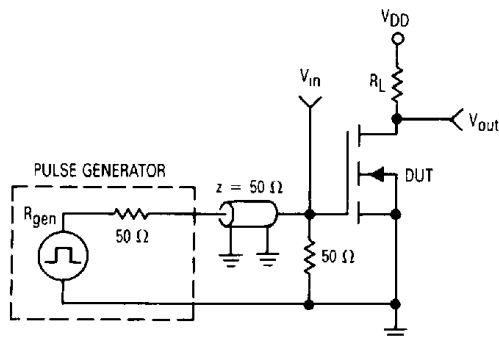


Figure 14. Switching Waveforms

