

64K x 1 Static RAM

Features

- **High speed**
— 15 ns
- **CMOS for optimum speed/power**
- **Low active power**
— 495 mW
- **Low standby power**
— 110 mW
- **TTL compatible inputs and outputs**
- **Automatic power-down when deselected**
- **Available in Pb-free and non Pb-free 22-pin (300-Mil) Molded DIP and 24-pin (300-Mil) Molded SOJ**

Functional Description

The CY7C187 is a high-performance CMOS static RAM organized as 65,536 words x 1 bit. Easy memory expansion is provided by an active LOW Chip Enable (CE) and tri-state drivers. The CY7C187 has an automatic power-down feature, reducing the power consumption by 56% when deselected.

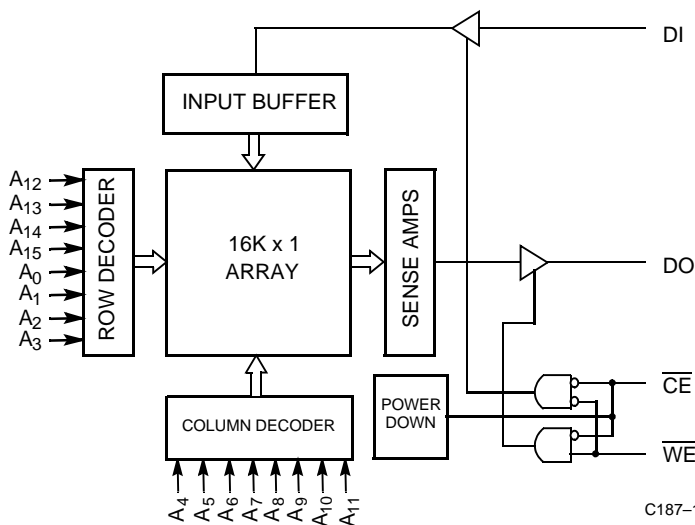
Writing to the device is accomplished when the Chip Enable (CE) and Write Enable (WE) inputs are both LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A₀ through A₁₅).

Reading the device is accomplished by taking the Chip Enable (CE) LOW, while Write Enable (WE) remains HIGH. Under these conditions, the contents of the memory location specified on the address pin will appear on the data output (D_{OUT}) pin.

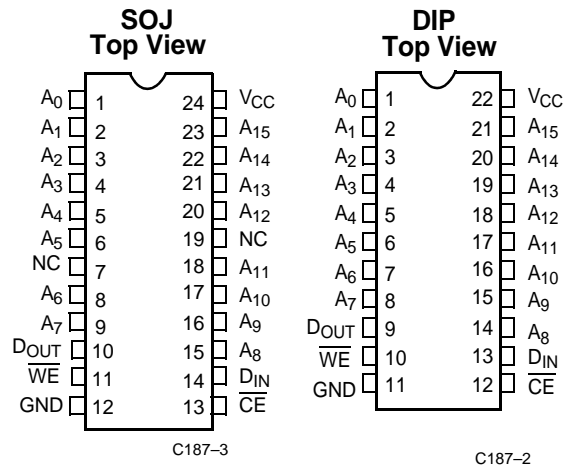
The output pin stays in high-impedance state when Chip Enable (CE) is HIGH or Write Enable (WE) is LOW.

The CY7C187 utilizes a die coat to insure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide

| | -15 | -25 | -35 |
|-----------------------------------|-----|-----|-----|
| Maximum Access Time (ns) | 15 | 25 | 35 |
| Maximum Operating Current (mA) | 90 | 70 | 70 |
| Maximum CMOS Standby Current (mA) | 20 | 20 | 20 |

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature-65°C to +150°C
- Ambient Temperature with Power Applied.....-55°C to +125°C
- Supply Voltage to Ground Potential (Pin 22 to Pin 11) -0.5V to +7.0V
- DC Voltage Applied to Outputs in High Z State^[1] -0.5V to +7.0V

- DC Input Voltage^[1]-0.5V to +7.0V
- Output Current into Outputs (LOW)..... 20 mA
- Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current..... >200 mA

Operating Range

| Range | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ± 10% |

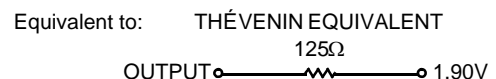
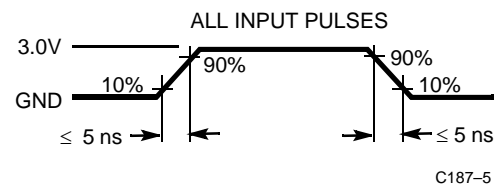
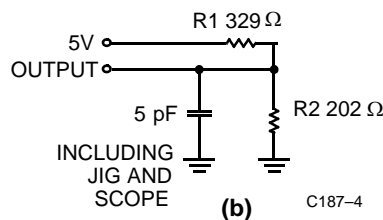
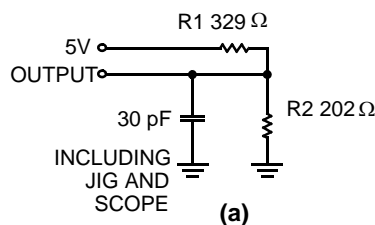
Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | -15 | | -25 and -35 | | Unit |
|------------------|---|--|------|-----------------|-------------|-----------------|------|
| | | | Min. | Max. | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -4.0mA | 2.4 | | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 12.0 mA | | 0.4 | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.2 | V _{CC} | 2.2 | V _{CC} | V |
| V _{IL} | Input LOW Voltage ^[1] | | -0.5 | 0.8 | -0.5 | 0.8 | V |
| I _{Ix} | Input Leakage Current | GND ≤ V _I ≤ V _{CC} | -5 | +5 | -5 | +5 | μA |
| I _{Oz} | Output Leakage Current | GND ≤ V _O ≤ V _{CC} , Output Disabled | -5 | +5 | -5 | +5 | μA |
| I _{CC} | V _{CC} Operating Supply Current | V _{CC} = Max., I _{OUT} = 0 mA | | 90 | | 70 | mA |
| I _{SB1} | Automatic \overline{CE} Power-Down Current ^[3] | Max. V _{CC} , $\overline{CE} \geq V_{IH}$ | | 40 | | 20 | mA |
| I _{SB2} | Automatic \overline{CE} Power-Down Current | Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V | | 20 | | 20 | mA |

Capacitance^[4]

| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|--|------|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V | 10 | pF |
| C _{OUT} | Output Capacitance | | 10 | pF |

AC Test Loads and Waveforms

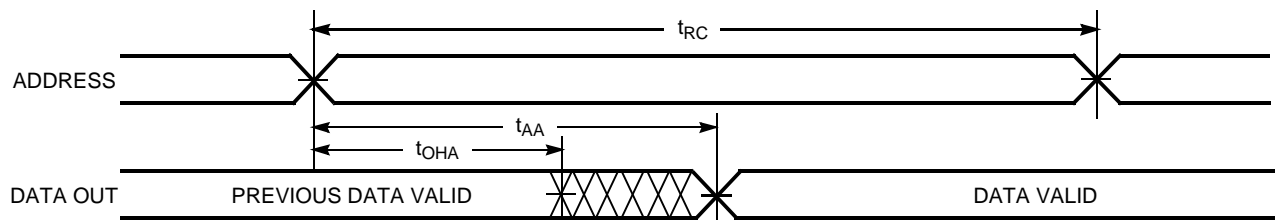


Notes:

1. V_{IL} (min.) = -3.0V for pulse durations less than 30 ns.
2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. A pull-up resistor to V_{CC} on the CE input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
4. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range^[5]

| Parameter | Description | -15 | | -25 | | -35 | | Unit |
|----------------------------------|--|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | |
| t_{RC} | Read Cycle Time | 15 | | 25 | | 35 | | ns |
| t_{AA} | Address to Data Valid | | 15 | | 25 | | 35 | ns |
| t_{OHA} | Output Hold from Address Change | 3 | | 5 | | 5 | | ns |
| t_{ACE} | \overline{CE} LOW to Data Valid | | 15 | | 25 | | 35 | ns |
| t_{LZCE} | \overline{CE} LOW to Low Z ^[6] | 3 | | 5 | | 5 | | ns |
| t_{HZCE} | \overline{CE} HIGH to High Z ^[6, 7] | | 8 | | 10 | | 15 | ns |
| t_{PU} | \overline{CE} LOW to Power Up | 0 | | 0 | | 0 | | ns |
| t_{PD} | \overline{CE} HIGH to Power Down | | 15 | | 20 | | 20 | ns |
| WRITE CYCLE^[8] | | | | | | | | |
| t_{WC} | Write Cycle Time | 15 | | 20 | | 25 | | ns |
| t_{SCE} | \overline{CE} LOW to Write End | 12 | | 20 | | 25 | | ns |
| t_{AW} | Address Set-Up to Write End | 12 | | 20 | | 25 | | ns |
| t_{HA} | Address Hold from Write End | 0 | | 0 | | 0 | | ns |
| t_{SA} | Address Set-Up to Write Start | 0 | | 0 | | 0 | | ns |
| t_{PWE} | \overline{WE} Pulse Width | 12 | | 15 | | 20 | | ns |
| t_{SD} | Data Set-Up to Write End | 10 | | 10 | | 15 | | ns |
| t_{HD} | Data Hold from Write End | 0 | | 0 | | 0 | | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z | 5 | | 5 | | 5 | | ns |
| t_{HZWE} | \overline{WE} LOW to High Z ^[7] | | 7 | | 7 | | 10 | ns |

Switching Waveforms
Read Cycle No. 1^[9, 10]


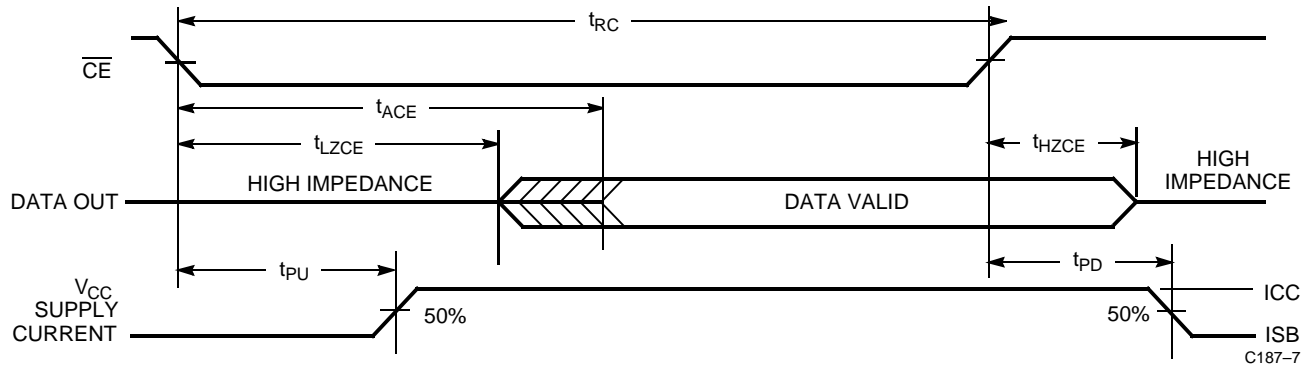
C187-6

Notes:

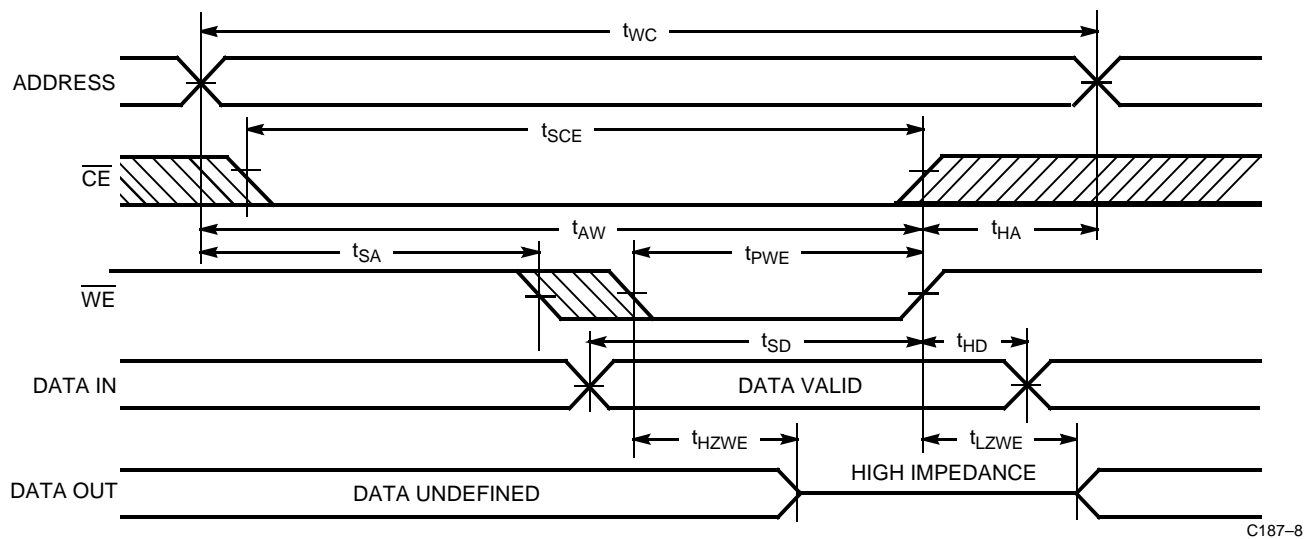
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
7. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. \overline{WE} is HIGH for read cycle.
10. Device is continuously selected, $\overline{CE} = V_{IL}$.

Switching Waveforms

Read Cycle No. 2^[9, 11]



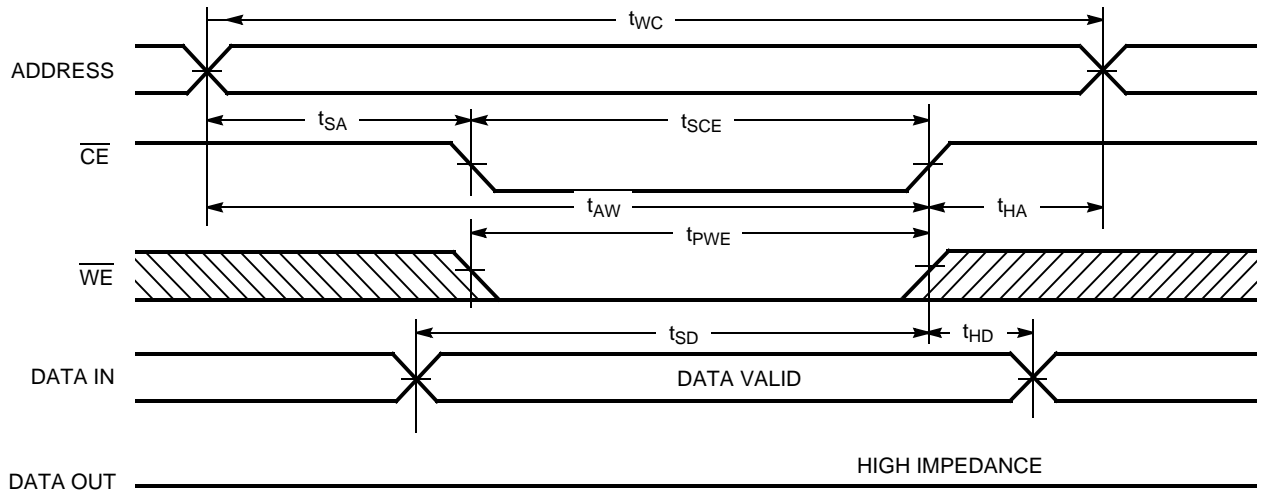
Write Cycle No. 1 (WE Controlled)^[11]



Note:
11. Address valid prior to or coincident with \overline{CE} transition LOW.

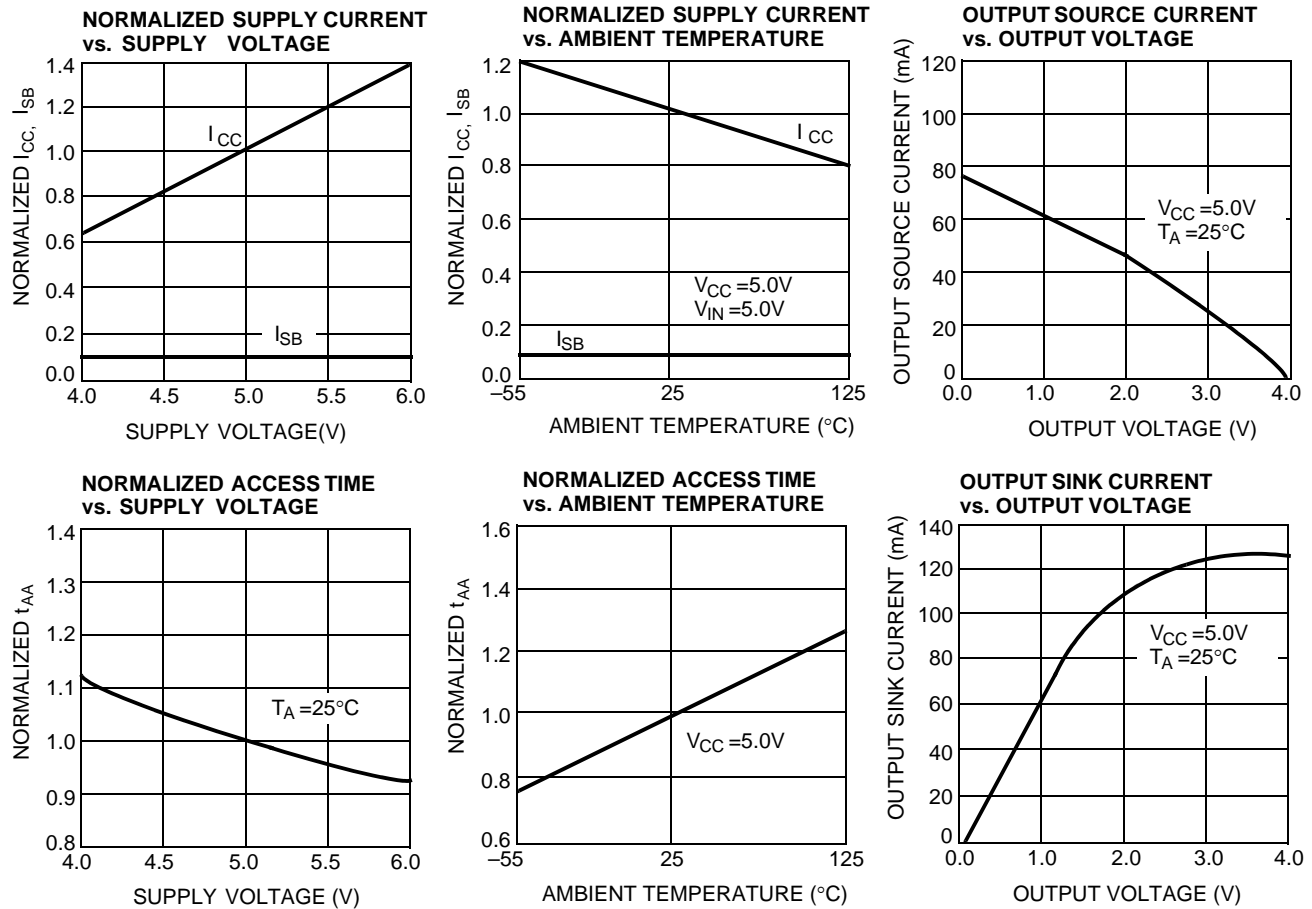
Switching Waveforms

Write Cycle No. 2(CE Controlled)^[11,13]



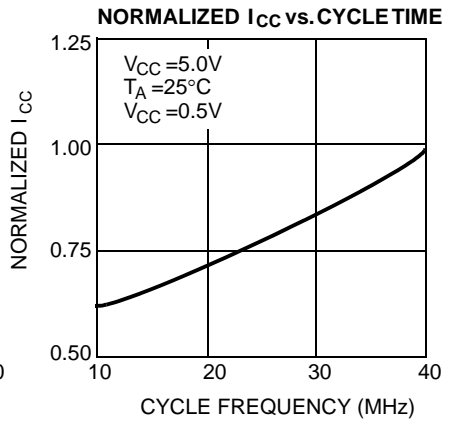
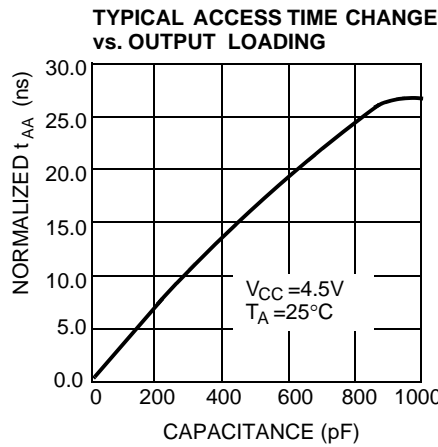
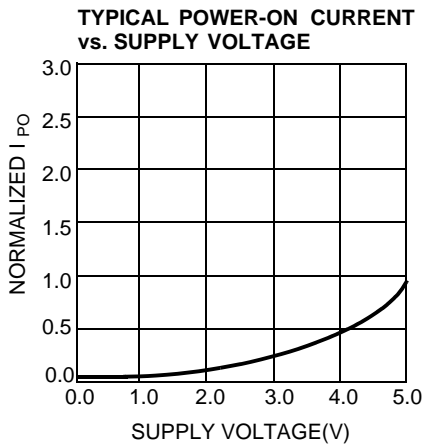
C187-9

Typical DC and AC Characteristics



Note:
12. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics (Continued)



Address Designators

| Address Name | Address Function | Pin Number |
|--------------|------------------|------------|
| A0 | X3 | 1 |
| A1 | X4 | 2 |
| A2 | X5 | 3 |
| A3 | X6 | 4 |
| A4 | X7 | 5 |
| A5 | Y7 | 6 |
| A6 | Y6 | 7 |
| A7 | Y2 | 8 |
| A8 | Y3 | 14 |
| A9 | Y1 | 15 |
| A10 | Y0 | 16 |
| A11 | Y4 | 17 |
| A12 | Y5 | 18 |
| A13 | X0 | 19 |
| A14 | X1 | 20 |
| A15 | X2 | 21 |

Truth Table

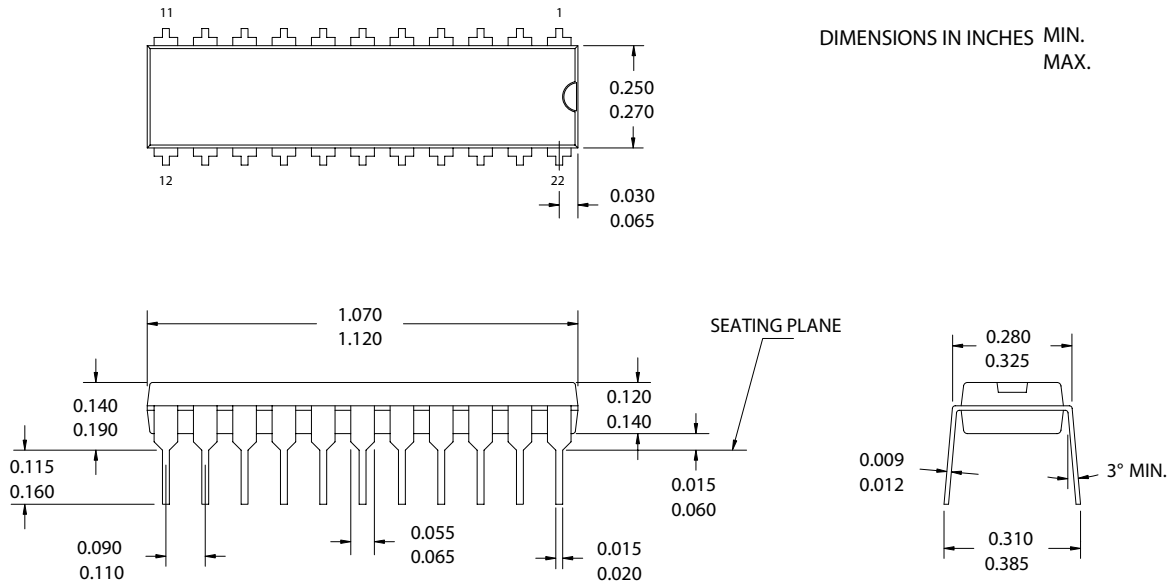
| CE | WE | Input/Output | Mode |
|----|----|--------------|---------------------|
| H | X | High Z | Deselect/Power-Down |
| L | H | Data Out | Read |
| L | L | Data In | Write |

Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|---------------|-----------------|---------------------------------------|-----------------|
| 15 | CY7C187-15PXC | 51-85012 | 22-pin (300-Mil) Molded DIP (Pb-free) | Commercial |
| 25 | CY7C187-25PC | 51-85012 | 22-pin (300-Mil) Molded DIP | Commercial |
| | CY7C187-25VC | 51-85030 | 24-pin (300-Mil) Molded SOJ | |
| | CY7C187-25VXC | | 24-pin (300-Mil) Molded SOJ (Pb-free) | |
| 35 | CY7C187-35VXC | 51-85030 | 24-pin (300-Mil) Molded SOJ (Pb-free) | Commercial |

Package Diagrams

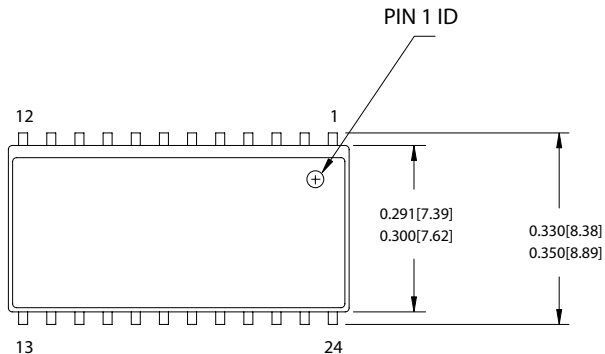
22-pin (300-Mil) PDIP (51-85012)



51-85012-*A

Package Diagrams (Continued)

24-pin (300-mil) SOJ (51-85030)



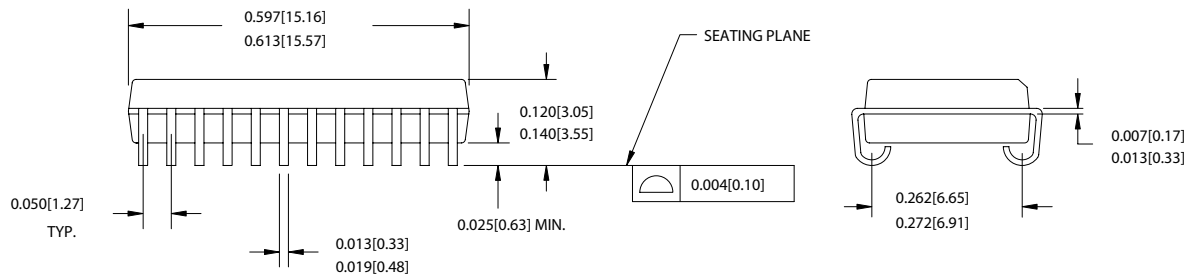
DIMENSIONS IN INCHES[MM]

MIN.
MAX.

REFERENCE JEDEC MO-088

PACKAGE WEIGHT 0.75gms

| PART # | |
|--------|----------------|
| V24.3 | STANDARD PKG. |
| VZ24.3 | LEAD FREE PKG. |



51-85030-B

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Document History Page

| Document Title: CY7C187 64K x 1 Static RAM Document Number: 38-05044 | | | | |
|---|---------|------------|-----------------|--|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 107146 | 09/10/01 | SZV | Change from Spec number: 38-00038 to 38-05044 |
| *A | 486744 | See ECN | NXR | Removed 20 ns speed bin Changed Low standby power from 220mW to 110mW Changed the description of I _{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the Ordering Information Table |