TOSHIBA Transistor Silicon PNP Epitaxial Type

TPC6602

High-Speed Switching Applications DC-DC Converter Applications Strobe Applications

- High DC current gain: $h_{FE} = 200$ to 500 ($I_{C} = -0.2$ A)
- Low collector-emitter saturation voltage: $V_{CE (sat)} = -0.19 \text{ V (max)}$
- High-speed switching: $t_f = 25$ ns (typ.)

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Collector-base voltage		V_{CBO}	-20	V	
Collector-emitter voltage	V_{CEO}	-10	V		
Emitter-base voltage		V _{EBO}	-7	V	
Collector current	DC	Ic	-2.0	Α	
	Pulse	I _{CP}	-3.5		
Base current		Ι _Β	-200	mA	
Collector power dissipation	t = 10 s	PC	1.6	W	
	DC	(Note)	0.8		
Junction temperature		Tj	150	°C	
Storage temperature range		T _{stg}	-55~150	°C	

Note: Mounted on FR4 board (glass epoxy, 1.6 mm thick, Cu area: 645 $\,$ mm $^2)$

Unit: mm 1. Collector (C) 4. Emitter (E) 2. Collector (C) 5. Collector (C) 3. Base (B) 6. Collector (C) JEDEC — JEITA — TOSHIBA 2-3T1

Weight: 0.011 g (typ.)

Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Collector cut-off current		I _{CBO}	$V_{CB} = -20 \text{ V}, I_E = 0$	_	_	-100	nA
Emitter cut-off curr	ent	I _{EBO}	$V_{EB} = -7 \text{ V}, I_{C} = 0$	_	_	-100	nA
Collector-emitter breakdown voltage		V (BR) CEO	$I_C = -10 \text{ mA}, I_B = 0$	-10	_	_	V
DC current gain		h _{FE} (1)	$V_{CE} = -2 \text{ V}, I_{C} = -0.2 \text{ A}$	200	_	500	
		h _{FE} (2)	$V_{CE} = -2 \text{ V}, I_{C} = -0.6 \text{ A}$	125	_	_	
Collector-emitter saturation voltage		V _{CE} (sat)	$I_C = -0.6 \text{ A}, I_B = -0.02 \text{ A}$	_	_	-0.19	V
Base-emitter saturation voltage		V _{BE (sat)}	$I_C = -0.6 \text{ A}, I_B = -0.02 \text{ A}$	_	_	-1.10	V
Collector output capacitance		C _{ob}	$V_{CB} = -10 \text{ V}, I_E = 0, f = 1 \text{ MHz}$	_	12	_	pF
Switching time	Rise time	t _r	See Figure 1 circuit diagram.	_	50	_	
	Storage time	t _{stg}	$V_{CC} \simeq -6 \text{ V}, R_L = 10 \Omega$	_	115	_	ns
	Fall time	t _f	$I_{B1} = -I_{B2} = -20 \text{ mA}$	_	25	_	

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Circuit Configuration Marking

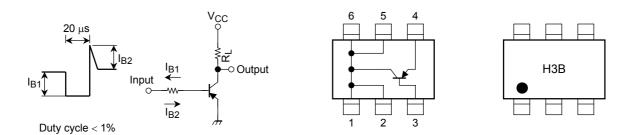
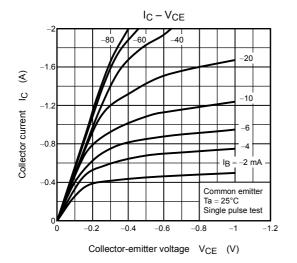
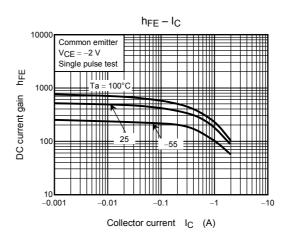
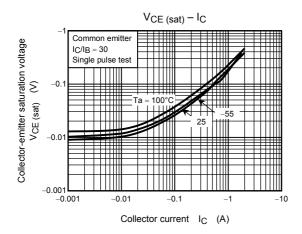
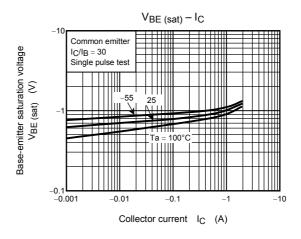


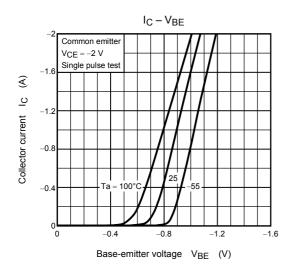
Figure 1 Switching Time Test Circuit & Timing Chart



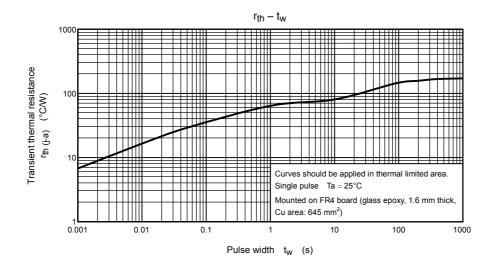


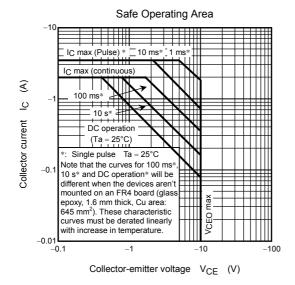






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