19-3045; Rev 0; 10/03

MAXIM

Parallelable Secondary-Side Synchronous Rectifier Driver and Feedback-Generator Controller ICs

General Description

The MAX5058/MAX5059 enable secondary-side synchronous rectification in isolated power supplies using widely available power MOSFETs. These devices facilitate the commutation of the secondary-side MOSFETs by providing a clean gate-drive signal that is synchronized to the power MOSFET switching in the primary side of the isolation transformer. The MAX5058/MAX5059 complement the MAX5051 and MAX5042/MAX5043 primary-side PWM ICs and enable the design of high-efficiency synchronously rectified isolated power supplies. Simultaneous conduction of the primary side and the freewheeling synchronous rectifier MOSFET is avoided by having a look-ahead signal (before the primary-side MOSFETs turn ON), thus eliminating large current spikes resulting from a shorted transformer secondary.

An on-board error amplifier with a versatile current reference output enables virtually unlimited possibilities in reference-voltage generation. Reference voltage for the error amplifier is generated by connecting an appropriate resistor to this output.

Low on-resistance margining MOSFETs integrated on-chip allow for implementation of a margining circuit without the use of external switches. The MAX5058 provides a 5V LDO output for logic-level MOSFETs while the MAX5059 provides a 10V LDO output for conventional 10V MOSFETs.

The MAX5058/MAX5059 are designed to enable paralleling of multiple power supplies for accurate current sharing using a simple 2-wire, differential, current-share bus. Parallelability enables expansion of the power capabilities and simplifies thermal management in high-output-current applications. When used in conjunction with the MAX5051, the primaries can also be synchronized and operated 180 degrees out of phase.

The MAX5058/MAX5059 are available in a 28-pin thermally enhanced TSSOP package and operate over a wide -40°C to +125°C temperature range.

Warning: The MAX5058/MAX5059 are designed to work in circuits that contain high voltages. Exercise caution.

Applications

Isolated Telecom Power Supplies

Isolated Networking Power Supplies

±48V Power-Supply Modules

Industrial Power Supplies

±48V/±12V Server Power Supplies

Features

- **Clean Drive Waveforms for Synchronous MOSFETs**
- **Utilization of a Look-Ahead Signal from the Primary for Proper Turn-On/Turn-Off Times**
- **Synchronous Rectifier Drivers Capable of Sourcing and Sinking Up to 2A Peak Current**
- **Internal Gate-Voltage Regulator for 5V (MAX5058) or 10V (MAX5059) Gate-Drive Voltage**
- **Internal Error Amplifier**
- **Accurate Differential Current-Share/Force Circuit Allows Paralleling of Several Power Supplies for High Output Current**
- **Internal Remote Voltage-Sense Amplifier**
- **Flexible Reference-Voltage Generation**
- **Output Voltage Regulation Down to 0.5V**
- **Low Quiescent Current Consumption of 2.5mA**
- **Integrated Digital Output Margining Circuit Saves External Parts and Board Space**
- **30ns Propagation Delay Time from Pulse Input to Output**
- **Automatic Detection of Discontinuous Current Conduction and Turn-Off of the Freewheeling MOSFET**
- **High Efficiency at Low Output Currents and Reverse-Current Protection**
- **Open-Drain Overtemperature Warning Flag**
- **28-Pin Thermally Enhanced TSSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	V_{REG} (V)
MAX5058AUI	-40°C to +125°C	28 TSSOP-EP*	5
MAX5058EUI	-40°C to +85°C	28 TSSOP-EP*	5
MAX5059AUI	-40°C to +125°C	28 TSSOP-EP*	10
MAX5059EUI	-40°C to +85°C	28 TSSOP-EP*	10

**EP = Exposed paddle.*

Pin Configuration appears at end of data sheet.

Parallelable Secondary-Side Synchronous Rectifier Driver and Feedback-Generator Controller ICs

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +30V
PGND to GND .....-0.3V to +0.3V
COMPV, V_{REG}, VDR, TSF to GND ..... -0.3V to +14V
All Other Pins to GND .....-0.3V to (VP + 0.3V)
V_{REG} Source Current 50mA
COMPV, RMGU, RMGD, TSF Sink Current 30mA
VP to GND .....-0.3V to +6V
VSO, CSO Source/Sink Current ..... ±5mA
SFP Source Current 5mA
QREC, QSYNC Continuous Current.....50mA
QREC, QSYNC Current < 500ns.....5A
Continuous Power Dissipation (T_A = +70°C)
28-Pin TSSOP (derate 23.8mW/°C above +70°C). 1905mW
Junction Temperature .....+150°C
Operating Temperature Ranges
MAX5058EUI, MAX5059EUI .....-40°C to +85°C
MAX5058AUI, MAX5059AUI.....-40°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +12V, GND = PGND = 0, VDR = V_{REG}, C_{QSYNC} = C_{QREC} = 0, ZCP = ZCN = BUFIN = CSP = CSN = SFN = VSN = GND, V_{IREF} = V_{VSP} = 1.785V, C_{VREG} = 2.2µF, C_{VP} = 1µF, C_{COMPS} = 0.1µF, C_{SFP} = 68nF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage Range	V+	MAX5058		4.5		28.0	V
		MAX5059		9.3		28.0	
Quiescent Supply Current	I_Q				2.5	5	mA
Switching Supply Current	I_{SW}	f_{SW} = 250kHz at BUFIN	MAX5058		4.5		mA
			MAX5059		6		
I_{REF}: REFERENCE CURRENT OUTPUT							
Reference Current	I_{IREF}	V_{IREF} = 1.785V		49.2	50	51.1	µA
Reference Current Variation	ΔI_{IREF}	V_{IREF} = 0.5V to 2.5V		-0.1		+0.1	%/V
Reference Voltage Compliance Range		Guaranteed by reference current variation test		0.5		2.5	V
V_{REG}: LOW-DROPOUT REGULATOR							
Regulator Output	V_{VREG}	I_{VREG} = 0 to 30mA	MAX5058	4.75	5	5.25	V
			MAX5059	9.4	10	10.6	
Line Regulation		MAX5058, V+ = 6V to 28V				25	mV
		MAX5059, V+ = 11V to 28V				25	
Dropout	V_{DROP}	MAX5058	V+ = 4.5V, I_{VREG} = 30mA		200	350	mV
		MAX5059	V+ = 9.3V, I_{VREG} = 30mA		200	350	
VP: INTERNAL REGULATOR							
Regulator Output Setpoint	V_{VP}	I_{VP} = 0 to 5mA		3.8		4.3	V
ZC: ZERO-CURRENT COMPARATOR							
Zero-Current Comparator Threshold	V_{ZCTH}	T_A = +25°C		+3.5	+5	+6.5	mV
Zero-Current Comparator Input Current	I_{ZC}			-2.5		+2.5	µA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +12V, GND = PGND = 0, VDR = V_{REG}, C_{QSYNC} = C_{QREC} = 0, ZCP = ZCN = BUFIN = CSP = CSN = SFN = VSN = GND, V_{IREF} = V_{VSP} = 1.785V, C_{VREG} = 2.2µF, C_{VP} = 1µF, C_{COMPS} = 0.1µF, C_{SFP} = 68nF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Zero-Current Comparator Input Range	V_{ZC}			-0.1		+1.5	V
Zero-Current Comparator Propagation Delay	t_{ZC}	10mV overdrive, from when V_{ZCP} - V_{ZCN} is greater than V_{ZCTH} to when QSYNC goes low			65		ns
BUFIN: SYNCHRONIZING PULSE INPUT							
BUFIN to Output Propagation Delay	t_{pd}	BUFIN rising to QREC rising or QSYNC falling			40		ns
BUFIN Input Current	I_{BUFIN}			-1		+1	µA
BUFIN Input Capacitance	C_{BUFIN}				10		pF
BUFIN Input-Logic High	V_{HBUFIN}			2.4			V
BUFIN Input-Logic Low	V_{LBUFIN}					0.8	V
MARGINING INPUTS							
RMGD Resistance	R_{RMGD}	Sinking 10mA			6.5	11	Ω
RMGU Resistance	R_{RMGU}	Sinking 10mA			6.5	11	Ω
MRGD Input-Logic High	V_{HMRGD}			2.4			V
MRGD Input-Logic Low	V_{LMRGD}					0.8	V
MRGU Input-Logic High	V_{HMRGU}			2.4			V
MRGU Input-Logic Low	V_{LMRGU}					0.8	V
MRGU, MRGD Input Resistance	R_{MRGD}, R_{MRGU}			40			kΩ
RMGU, RMGD Leakage Current	I_{RMGU}, I_{RMGD}			-100		+100	nA
DRIVER OUTPUTS							
QREC, QSYNC Peak Source Current	I_{QREC_SO}, I_{QSYNC_SO}				2		A
QREC, QSYNC Output-Voltage High	V_{QREC_H}, V_{QSYNC_H}	Measured with respect to V_{VDR}, sourcing 50mA	MAX5058		75	150	mV
			MAX5059		75	150	
QREC, QSYNC Low-to-High Delay Time	t_{PDLH}	C_{QREC} = C_{QSYNC} = 0			30		ns
		C_{QREC} = C_{QSYNC} = 5nF			70		
QREC, QSYNC Peak Sink Current	I_{QREC_SI}, I_{QSYNC_SI}				2		A
QREC, QSYNC Output-Voltage Low	V_{QREC_L}, V_{QSYNC_L}	Sinking 50mA	MAX5058		50	100	mV
			MAX5059		50	100	
QREC, QSYNC High-to-Low Delay Time	t_{PDHL}	C_{QREC} = C_{QSYNC} = 0			40		ns
		C_{QREC} = C_{QSYNC} = 5nF			70		

Parallelable Secondary-Side Synchronous Rectifier Driver and Feedback-Generator Controller ICs

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +12V, GND = PGND = 0, VDR = V_{REG}, C_{QSYNC} = C_{QREC} = 0, ZCP = ZCN = BUFIN = CSP = CSN = SFN = VSN = GND, V_{IREF} = V_{VSP} = 1.785V, C_{VREG} = 2.2µF, C_{VP} = 1µF, C_{COMPS} = 0.1µF, C_{SFP} = 68nF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER						
Inverting Input Current	I_{INV}		-50		+50	nA
Error-Amplifier Input Range	V_{INV}		0		2.5	V
Error-Amplifier Input Offset	V_{OS}	I_{COMPV} = 100µA to 5mA	-5		+5	mV
Error-Amplifier Output-Voltage Low	V_{COMPV}	I_{COMPV} = 5mA			200	mV
Error-Amplifier Unity-Gain BW	GBW	R_{COMP} = 220Ω, I_{COMP} = 5mA		1.3		MHz
Error-Amplifier Voltage Gain	A_{VOL}	R_{COMPV} = 220Ω, I_{COMP} = 5mA		80		dB
Error-Amplifier PSRR	PSRR			60		dB
COMPV Output Resistance to Ground		(Note 1)		1		MΩ
REMOTE-SENSE AMPLIFIER (RSA)						
VSN Input Current	I_{VSN}		-100		+100	µA
VSP Input Current	I_{VSP}		-20		+100	µA
Input Common-Mode Range			-0.3		+3.8	V
Input Offset Voltage	V_{OSRSA}	I_{VSO} = -0.5mA to +0.5mA		-4		mV
Output Impedance				8		Ω
Amplifier -3dB Frequency		I_{VSO} = -0.5mA to +0.5mA		1		MHz
Remote-Sense Amplifier Gain	G_{RS}	I_{VSO} = -0.5mA to +0.5mA	0.9925	1	1.0075	V/V
CURRENT-SENSE AMPLIFIER (CSA)						
CSN Input Current	I_{CSN}	-0.3V ≤ V_{CSN} ≤ +3.8V, -0.3V ≤ V_{CSP} ≤ +3.8V	-150		+150	µA
CSP Input Current	I_{CSP}	-0.3V ≤ V_{CSP} ≤ +3.8V	-40		+150	µA
Input Offset Voltage		I_{CSO} = -500µA to +500µA (Note 2)	+20	+25	+30	mV
Current-Sense Amplifier Gain	G_{CSA}	I_{CSO} = -500µA to +500µA	19.8	20	20.2	V/V
Input Differential-Mode Range					100	mV
Input Common-Mode Range			-0.3		+3.8	V
Output-Voltage Level Shift	V_{LS}	(Note 2)	0.415		0.570	V
Output Voltage Range	$V_{CSO(MIN)}$	I_{CSO} = -500µA to +500µA	0.1		3.0	V
Amplifier -3dB Frequency	f_{-3dB}	I_{CSO} = -500µA to +500µA		50		kHz
SHARE-FORCE AMPLIFIER (SFA)						
Sink Current					60	µA
Source Current			500			µA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +12V, GND = PGND = 0, VDR = V_{REG}, C_{QSYNC} = C_{QREC} = 0, ZCP = ZCN = BUFIN = CSP = CSN = SFN = VSN = GND, V_{IREF} = V_{VSP} = 1.785V, C_{VREG} = 2.2µF, C_{VP} = 1µF, C_{COMPS} = 0.1µF, C_{SFP} = 68nF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT-ADJUST AMPLIFIER (CAA)						
Transconductance				500		µA/V
Common-Mode Input Voltage Range			0.45		2.55	V
Output Voltage Range			0.85		2.75	V
Offset Voltage		T_A = +25°C	20	42	65	mV
Open-Loop Gain				72		dB
CURRENT-ADJUST VOLTAGE-TO-CURRENT CONVERTER						
Input Voltage Range			0.75		2.75	V
Input Voltage Offset				1.25		V
Output Voltage Range			0.5		2.5	V
Transconductance				1.15		µA/V
Maximum Current Adjustment Value			1.38	1.5	1.66	µA
THERMAL SHUTDOWN						
Thermal Warning Flag Level		When TSF pulls low		+125		°C
Thermal Warning Flag Hysteresis				15		°C
Internal Thermal-Shutdown Level				+160		°C
Internal Thermal-Shutdown Hysteresis				15		°C
TSF Maximum Output Voltage		I_{TSF} = 5mA			120	mV
TSF Output Leakage Current					0.1	µA

Note 1: Output resistance to ground used for unity-gain stability.
Note 2: $V_{CSO} = G_{CSA}(V_{CSP} - V_{CSN}) + V_{LS}$.

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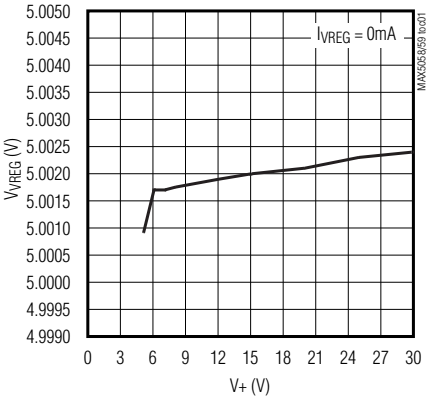
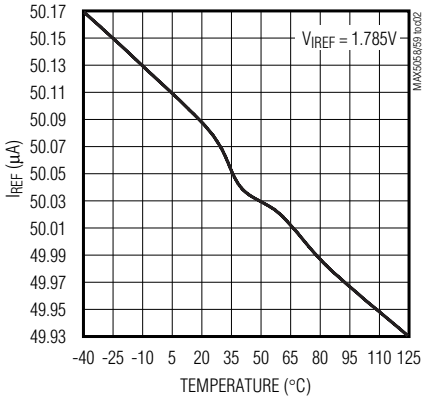
Typical Operating Characteristics

(V+ = +12V, GND = PGND = 0, VDR = V_{REG}, C_{QSYNC} = C_{QREC} = 0, ZCP = ZCN = BUFIN = CSP = CSN = SFN = VSN = GND, V_{IREF} = V_{VSP} = 1.785V, V_{COMPS} = 0.5V, C_{VREG} = 2.2µF, C_{VP} = 1µF, C_{COMPS} = 0.1µF, C_{SFP} = 68nF, T_A = +25°C, unless otherwise noted.)

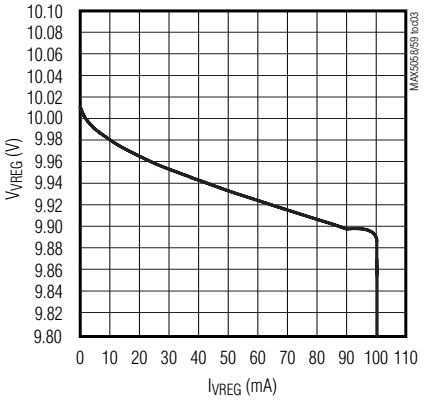
LDO OUTPUT VOLTAGE (V_{VREG}) vs. INPUT VOLTAGE (MAX5058)



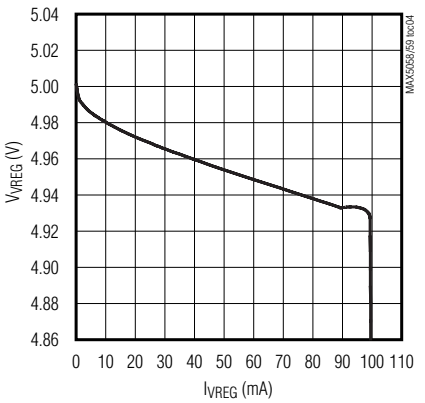
I_{REF} OUTPUT CURRENT vs. TEMPERATURE



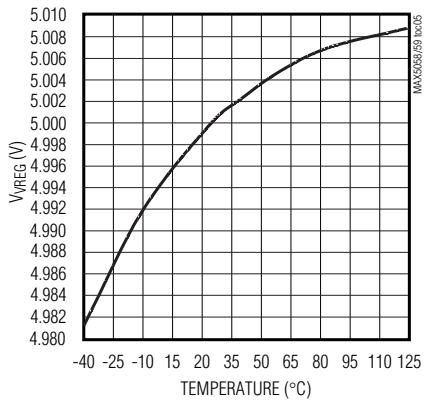
LDO OUTPUT VOLTAGE (V_{VREG}) vs. LOAD CURRENT (MAX5059)



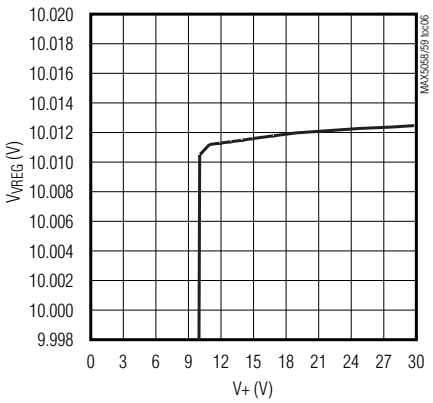
LDO OUTPUT VOLTAGE (V_{VREG}) vs. LOAD CURRENT (MAX5058)



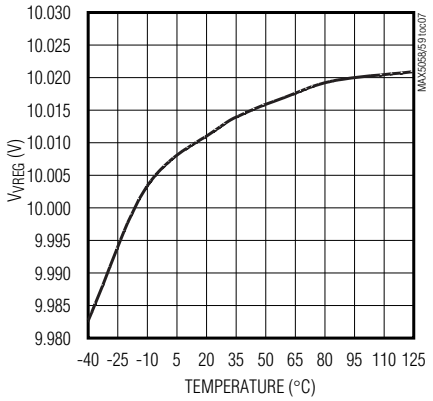
LDO OUTPUT VOLTAGE (V_{REG}) vs. TEMPERATURE (MAX5058)



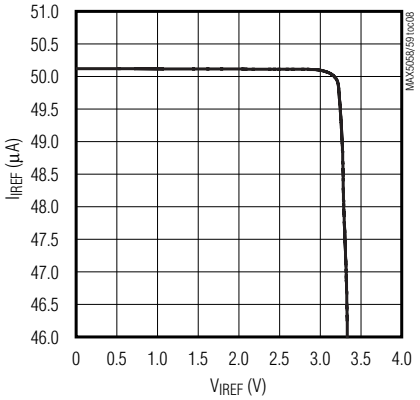
LDO OUTPUT VOLTAGE (V_{VREG}) vs. INPUT VOLTAGE (MAX5059)



LDO OUTPUT VOLTAGE (V_{VREG}) vs. TEMPERATURE (MAX5059)



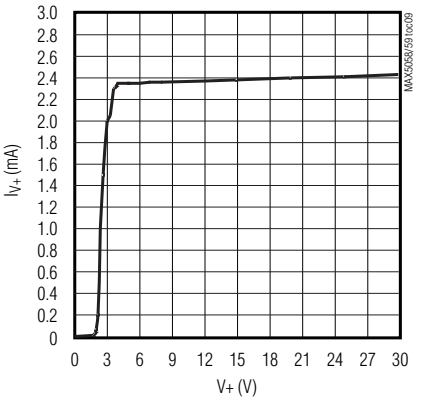
I_{REF} OUTPUT CURRENT vs. I_{REF} OUTPUT VOLTAGE



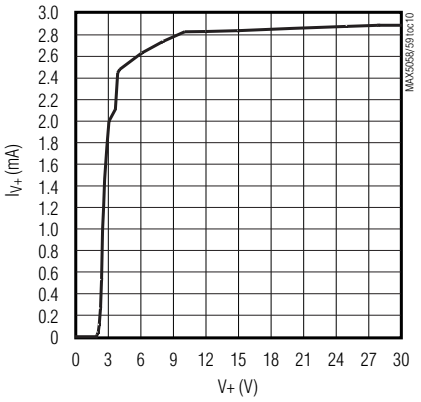
Typical Operating Characteristics (continued)

(V+ = +12V, GND = PGND = 0, VDR = V_{REG}, C_{QSYNC} = C_{QREC} = 0, ZCP = ZCN = BUFIN = CSP = CSN = SFN = VSN = GND, V_{IREF} = V_{VSP} = 1.785V, V_{COMPS} = 0.5V, C_{VREG} = 2.2µF, C_{VP} = 1µF, C_{COMPS} = 0.1µF, C_{SFP} = 68nF, T_A = +25°C, unless otherwise noted.)

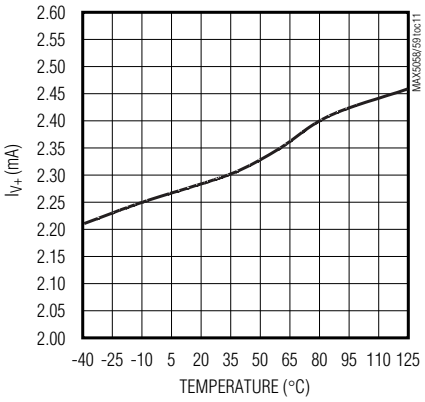
QUIESCENT SUPPLY CURRENT vs. INPUT VOLTAGE (MAX5058)



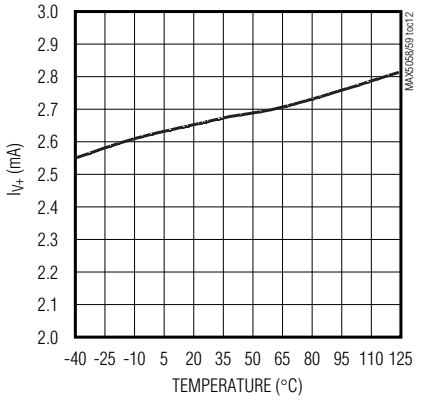
QUIESCENT SUPPLY CURRENT vs. INPUT VOLTAGE (MAX5059)



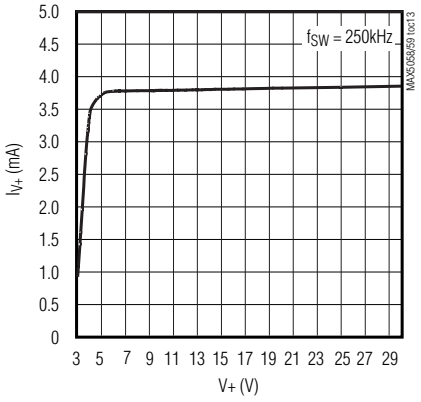
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE (MAX5058)



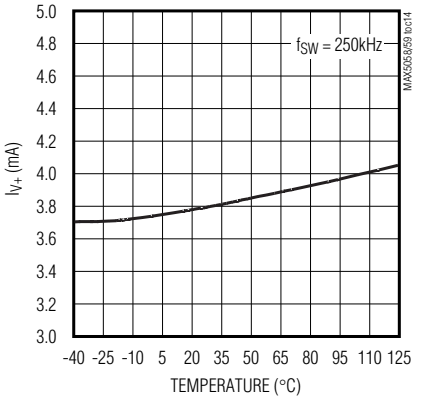
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE (MAX5059)



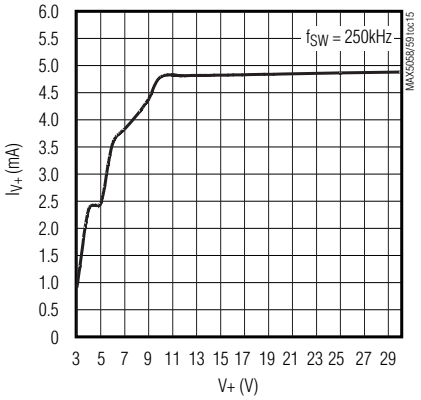
SWITCHING SUPPLY CURRENT vs. INPUT VOLTAGE (MAX5058)



SWITCHING SUPPLY CURRENT vs. TEMPERATURE (MAX5058)



SWITCHING SUPPLY CURRENT vs. INPUT VOLTAGE (MAX5059)

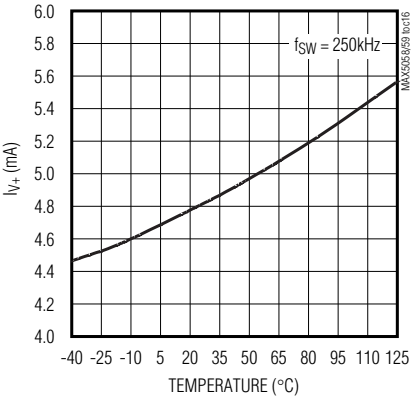


Parallelable Secondary-Side Synchronous Rectifier Driver and Feedback-Generator Controller ICs

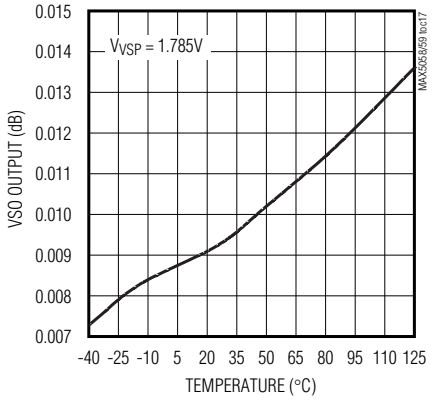
Typical Operating Characteristics (continued)

(V+ = +12V, GND = PGND = 0, VDR = V_{REG}, C_{QSYNC} = C_{QREC} = 0, ZCP = ZCN = BUFIN = CSP = CSN = SFN = VSN = GND, V_{IREF} = V_{VSP} = 1.785V, V_{COMPS} = 0.5V, C_{VREG} = 2.2µF, C_{VP} = 1µF, C_{COMPS} = 0.1µF, C_{SFP} = 68nF, T_A = +25°C, unless otherwise noted.)

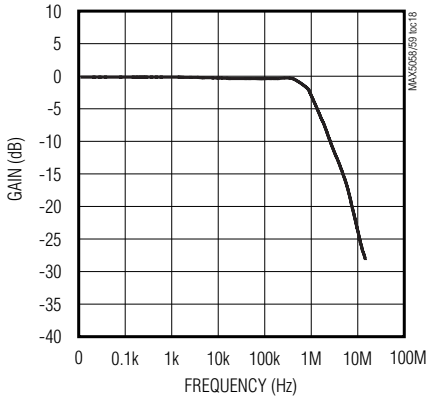
SWITCHING SUPPLY CURRENT vs. TEMPERATURE (MAX5059)



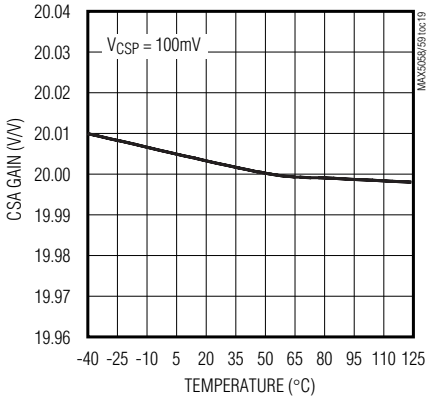
REMOTE-SENSE AMPLIFIER (RSA) GAIN vs. TEMPERATURE



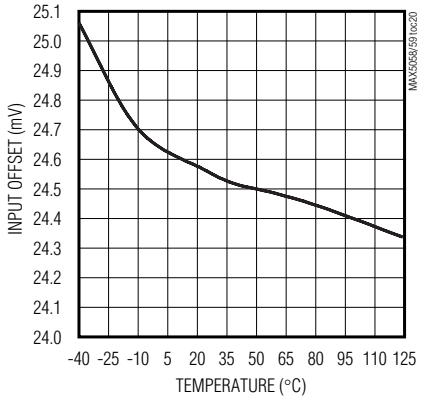
RSA GAIN vs. FREQUENCY



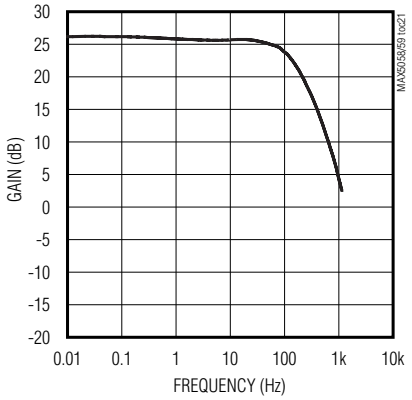
CURRENT-SENSE AMPLIFIER (CSA) GAIN vs. TEMPERATURE



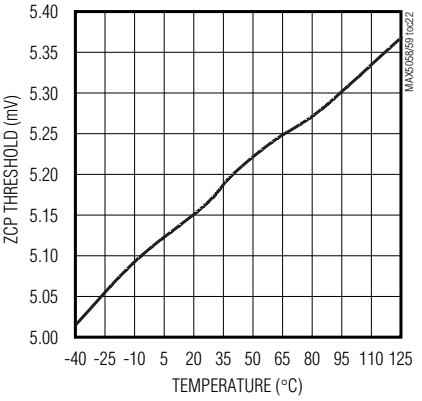
CSA INPUT OFFSET vs. TEMPERATURE



CSA GAIN vs. FREQUENCY



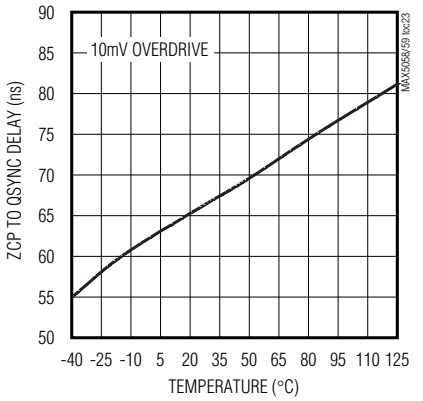
ZERO-CURRENT COMPARATOR THRESHOLD vs. TEMPERATURE



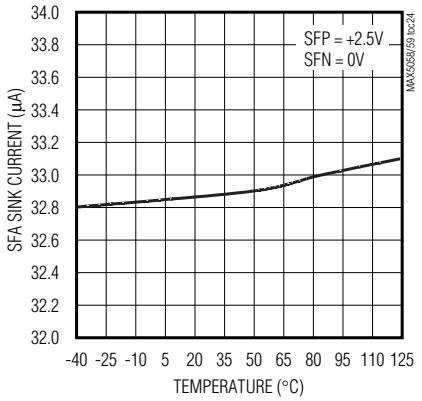
Typical Operating Characteristics (continued)

(V+ = +12V, GND = PGND = 0, VDR = V_{REG}, C_{QSYNC} = C_{QREC} = 0, ZCP = ZCN = BUFIN = CSP = CSN = SFN = VSN = GND, V_{IREF} = V_{VSP} = 1.785V, V_{COMPS} = 0.5V, C_{VREG} = 2.2µF, C_{VP} = 1µF, C_{COMPS} = 0.1µF, C_{SFP} = 68nF, T_A = +25°C, unless otherwise noted.)

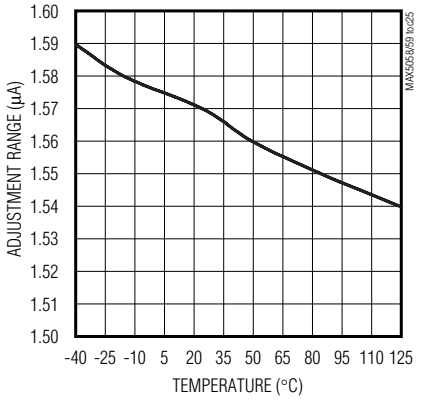
ZERO-CURRENT PROPAGATION DELAY vs. TEMPERATURE



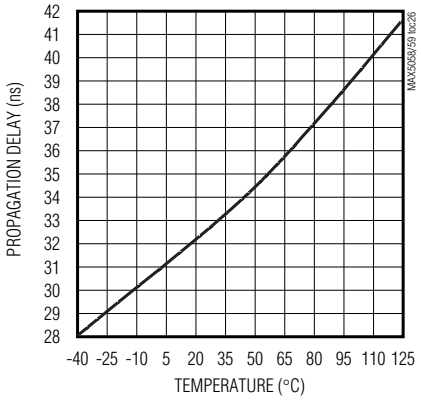
SFA AMPLIFIER MAXIMUM SINK CURRENT vs. TEMPERATURE



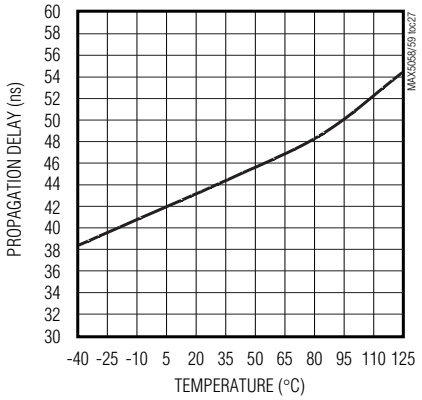
CURRENT-ADJUST VOLTAGE TO CURRENT-CONVERTER ADJUSTMENT RANGE vs. TEMPERATURE



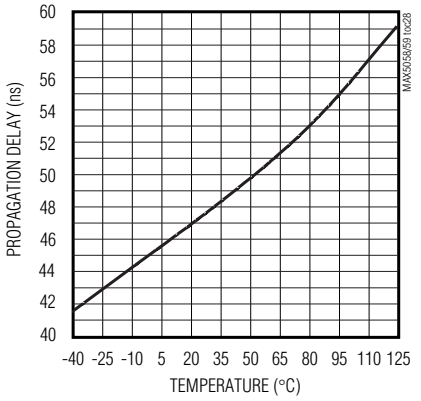
BUFIN TO QREC LOW-TO-HIGH PROPAGATION DELAY vs. TEMPERATURE



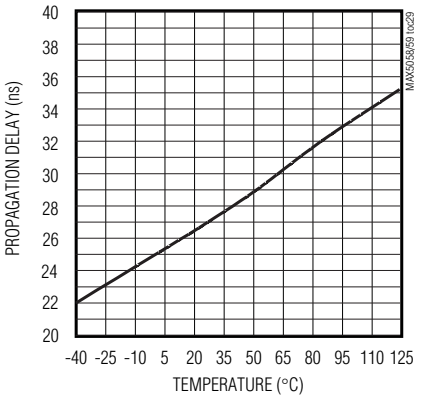
BUFIN TO QREC HIGH-TO-LOW PROPAGATION DELAY vs. TEMPERATURE



BUFIN TO QSYNC LOW-TO-HIGH PROPAGATION DELAY vs. TEMPERATURE



BUFIN TO QSYNC HIGH-TO-LOW PROPAGATION DELAY vs. TEMPERATURE



Parallelable Secondary-Side Synchronous Rectifier Driver and Feedback-Generator Controller ICs

Pin Description

PIN	NAME	FUNCTION
1	ZCP	Zero-Inductor Current-Sense Comparator Input. The source voltage of the freewheeling FET (N4 in the *Typical Application Circuit*) is sensed. The gate drive is terminated when this voltage becomes positive during a primary power-OFF cycle.
2	ZCN	Zero-Inductor Current-Sense Comparator Negative Input
3	GND	Ground Connection
4	SFN	Negative Input of the Share-Force Amplifier. Connect the SFN inputs together from all the power-supply secondaries, then connect to the load return terminal (isolated GND). Connect to GND when current sharing is not used.
5	SFP	Positive Input of the Share-Force Amplifier. Connect the SFP pins together from all the power-supply secondaries. Leave this pin unconnected when current sharing is not used.
6	COMPS	Compensation Output of the Load-Share Transconductance Amplifier
7	TSF	Thermal Warning Flag Output
8	MRGU	Margin-Up Logic Input. When toggled high, the power-supply output voltage is set to the high margin.
9	MRGD	Margin-Down Logic Input. When toggled high, the power-supply output voltage is set to the low margin.
10	RMGD	Resistor Connection for Margin-Down
11	RMGU	Resistor Connection for Margin-Up
12	I_{REF}	Reference Current Output. A resistor from this current source output to GND sets the reference voltage used by the error amplifier.
13	COMPV	Compensation Connection for the Error Amplifier. The feedback optocoupler LED is also connected to this point. This open-drain output is capable of sinking at least 5mA.
14	INV	Inverting Input of the Error Amplifier. A voltage-divider connected to this input scales the power-supply output voltage for regulation.
15	VSO	Output of the Remote-Sense Amplifier
16	VSN	Negative Input of the Remote-Sense Amplifier. Connect this to the negative terminal of the load.
17	VSP	Positive Input of the Remote-Sense Amplifier. Connect this to the positive terminal of the load.
18	CSO	Output of the Current-Sense Amplifier. It can be used to monitor the output current.
19	CSN	Connect this input to the negative terminal of the output current-sense resistor. Connect to GND when not used.
20	CSP	Connect this input to the positive terminal of the output current-sense resistor. Connect to GND when not used.
21	VP	Compensation Pin for Internal +4V Preregulator. A minimum 1µF low-ESR capacitor must be connected to this pin for bypassing.
22	V+	Supply Connection for the IC and Input to the Internal 5V (MAX5058) or 10V (MAX5059) Regulator. Maximum voltage on this input is 28V.
23	V_{REG}	Regulated +5V (MAX5058) or +10V(MAX5059) Output Used by the Internal Circuitry and the Output Drivers. A minimum 1µF capacitor must be connected to this pin for bypassing.
24	BUFIN	Input for the Synchronizing Pulse. This pulse is provided by the primary-side power IC.
25	VDR	Supply Connection for the Output Drivers. Can be connected to V_{REG} for 5V (MAX5058) or 10V (MAX5059) operation.
26	QREC	Driver Output for the Rectifying MOSFET
27	PGND	Power-Ground Connection. Return ground connection for the gate-driver pulse currents.
28	QSYNC	Driver Output for the Recirculating MOSFET
—	EP	Exposed Pad. This is the exposed pad on the underside of the IC. Connect the exposed paddle to GND and to a large copper ground plane to aid in heat dissipation.

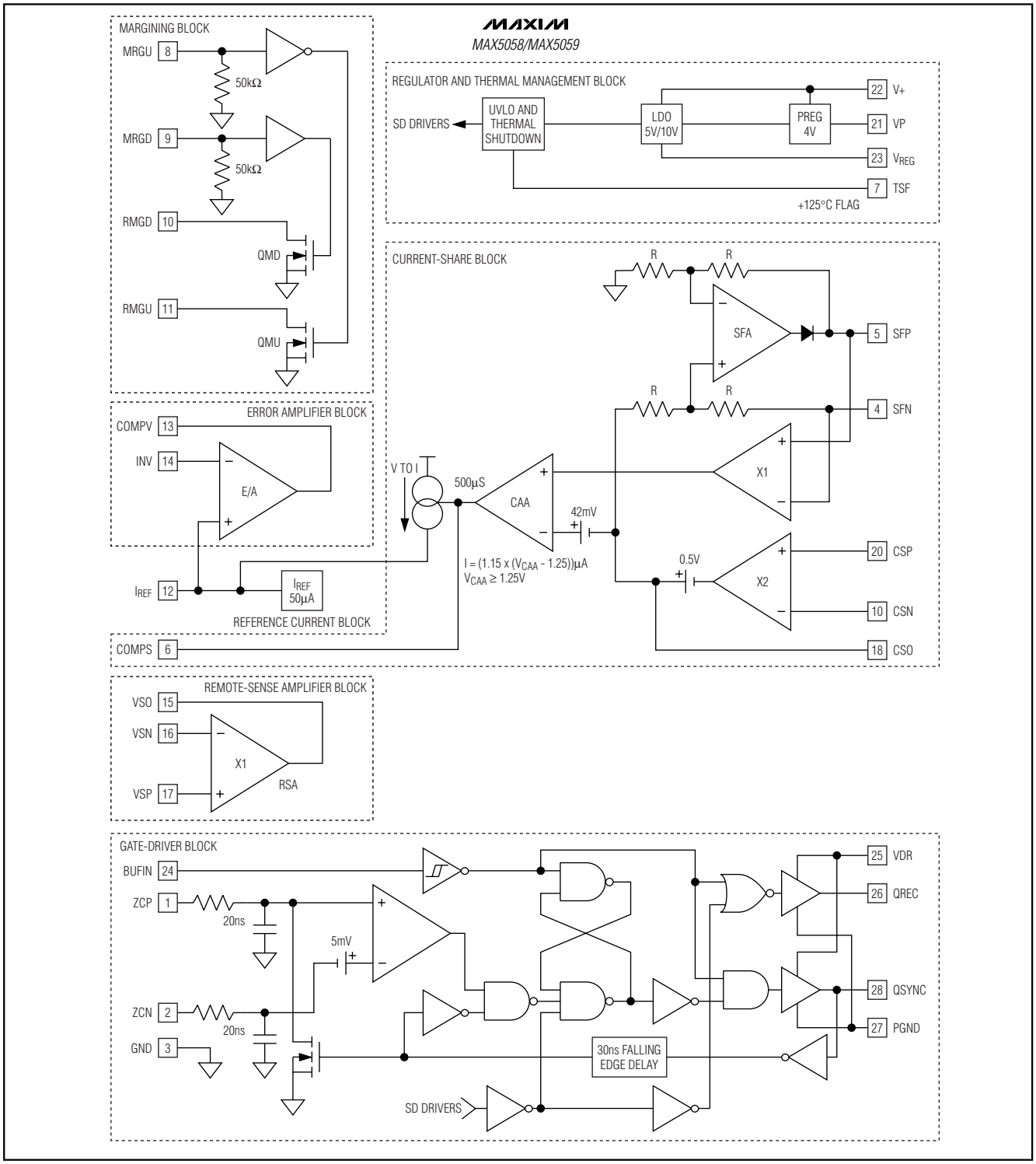


Figure 1. MAX5058/MAX5059 Functional Diagram

Parallelable Secondary-Side Synchronous Rectifier Driver and Feedback-Generator Controller ICs

Detailed Description

The MAX5058/MAX5059 enable the design of high-efficiency, isolated power supplies using synchronous rectification on the secondary side. These devices commutate the secondary-side MOSFETs by providing a clean gate-drive signal that is synchronized to the power MOSFET switching in the primary side of the isolation transformer. Once fully enhanced, the secondary-side MOSFETs have very low on-resistance, producing a voltage drop much lower than Schottky diodes, resulting in much higher efficiencies. Simultaneous conduction of the synchronous rectifier MOSFETs is avoided by having a look-ahead signal before the primary MOSFETs turn on. This eliminates large current spikes from a shorted transformer secondary.

The MAX5058 has a 5V internal gate-drive voltage regulator that can be used with logic-level MOSFETs. The MAX5059 has a 10V internal gate-drive voltage regulator that can be used with high-gate-voltage MOSFETs.

In addition to the gate drivers, there are blocks that make the MAX5058/MAX5059 complete secondary-side solutions. These blocks are as follows:

- Regulator and thermal-management block
- Buffer input and gate-driver block
- Reference-current block
- Error-amplifier block
- Margining block
- Remote-sense amplifier block
- Current-share block

Regulators and Thermal Management

The linear regulators in the MAX5058/MAX5059 provide power for the internal circuitry, as well as power for running the external synchronous MOSFETs. Design is simplified by deriving the power from the secondary winding before the output-filter inductor. The peak voltage at the secondary is at least twice the output voltage, yielding more than 7V peak even for output voltages down to 3.3V. Use a diode and a capacitor to rectify and filter the voltage before applying it to V+ (see D6 and C32 in the *Typical Application Circuit*). The input for the regulator is V+ and the output is V_{REG}. Connect VDR to V_{REG} to provide the supply for the gate driver's QREC and QSYNC. For logic-level MOSFETs, use the MAX5058. For conventional MOSFETs that require 10V to be fully enhanced, use the MAX5059. The V+ input voltage range is from +4.5V to +28V. Supply enough current to this input to satisfy the quiescent supply current of the MAX5058/MAX5059, as well as the current for the MOSFET drivers. Estimate the total required supply current by using the following formula:

$$I_{V+} = I_{SW} + f_{SW} \times (Q_{N3} + Q_{N4})$$

where I_{V+} is the current that must be supplied into V+ and Q_{N3}, Q_{N4} are the total gate charges of MOSFETs N3 and N4 in the *Typical Application Circuit*. f_{SW} is the switching frequency and I_{SW} is the switching current of the part. Use high-quality ceramic capacitors to bypass V+ and V_{REG}. Use additional capacitance as required for bypassing switching currents generated by the drivers when driving the chosen MOSFETs. Connect at least a 1µF ceramic capacitor at the output of the regulator V_{REG} for stability.

The MAX5058/MAX5059 have an exposed pad at the back of the package to enable heatsinking directly to a ground plane. When soldered to a $1in^2$ copper island, these devices are able to dissipate approximately 1.9W at +70°C ambient temperature. Connect the exposed pad to the GND.

In addition to the regulators, this block contains a thermal-shutdown circuit that shuts down the gate drivers if the die temperature exceeds +160°C. This is a last resort shutdown mechanism. The trigger of this shutdown mechanism must be avoided. Turning off the secondary synchronous rectifier drivers in this manner while the output carries the full load current causes the current to be diverted to the lossy external diodes or body diodes of the MOSFETs. This, in most cases, leads to rectifier failure due to power dissipation. To prevent this, make use of the TSF output (temperature warning flag). TSF is an open-drain output that gets asserted when the die temperature exceeds +125°C, well before the actual thermal shutdown at +160°C. An optocoupler connected from V_{REG} to the TSF pin can provide a means for shutting down the switching at the primary side, thus avoiding catastrophic failure.

Buffer Input (BUFIN) and MOSFET Drivers

The MAX5058/MAX5059 drive external N-channel MOSFETs at QSYNC and QREC. The QSYNC output drives the gate of the freewheeling MOSFET N4 in the *Typical Application Circuit*. The QREC output drives the gate of the rectifying MOSFET N3 in the *Typical Application Circuit*. Each gate-driver output is capable of sinking and sourcing up to 2A peak current, enabling the MAX5058/MAX5059 to drive high-gate-charge MOSFETs.

The MOSFET drivers are synchronized to the primary-side switching by using the BUFIN input. BUFIN accepts the PWM information from the primary through a high-speed optocoupler or through a small isolation pulse transformer. Figures 2 through 6 show the interface details using an optocoupler or a pulse transformer with two different kinds of primary-side PWM controllers.

For proper operation, the MAX5051, MAX5042, and MAX5043 devices generate a look-ahead signal that precedes the actual switching of the primary MOSFETs by a small amount of time, typically less than 100ns. Additional circuitry may be required when the MAX5058/MAX5059 are used with other primary-side controllers not capable of providing a look-ahead signal.

When BUFIN goes high, QREC goes high and QSYNC goes low. When BUFIN goes low, QREC goes low and QSYNC goes high.

The MAX5058/MAX5059 provide improved efficiency at light loads by allowing discontinuous conduction operation. A zero-crossing comparator with inputs ZCP and ZCN monitors the current through the freewheeling MOSFET using a sense resistor at its source. The freewheeling MOSFET is turned off when the inductor current is near zero. The actual threshold can be externally adjusted. The *Typical Application Circuit* shows one method for trip-point adjustment using components R31 and R34.

BUFIN is internally clamped to 4V. Use a voltage-divider, if necessary, to reduce any external voltage applied to this pin to less than 4V.

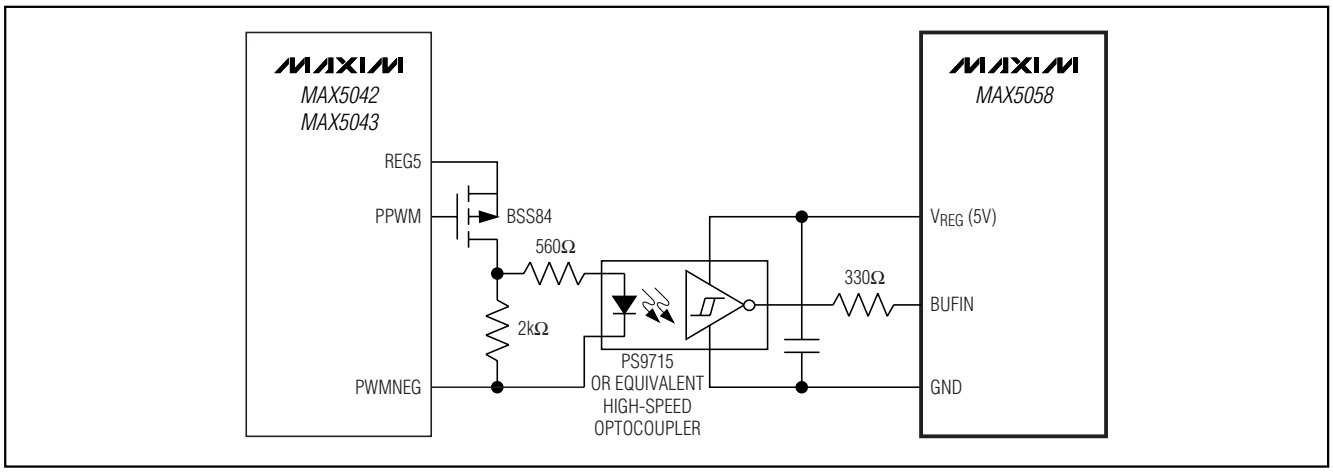


Figure 2. Interface of MAX5058 to MAX5042/MAX5043 Using a High-Speed Optocoupler

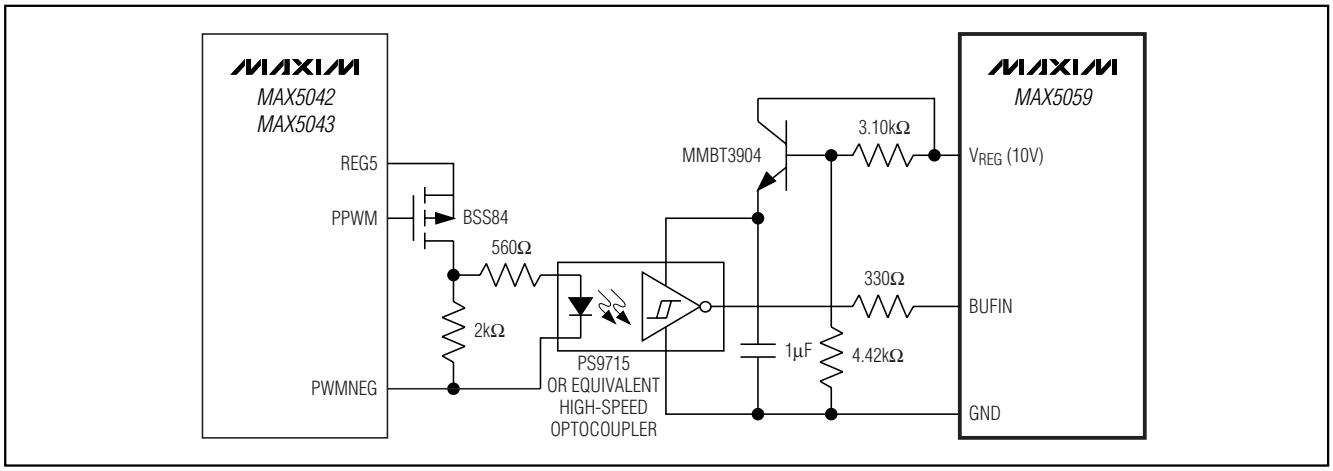


Figure 3. Interface of MAX5059 to MAX5042/MAX5043 Using a High-Speed Optocoupler

Parallelable Secondary-Side Synchronous Rectifier Driver and Feedback-Generator Controller ICs

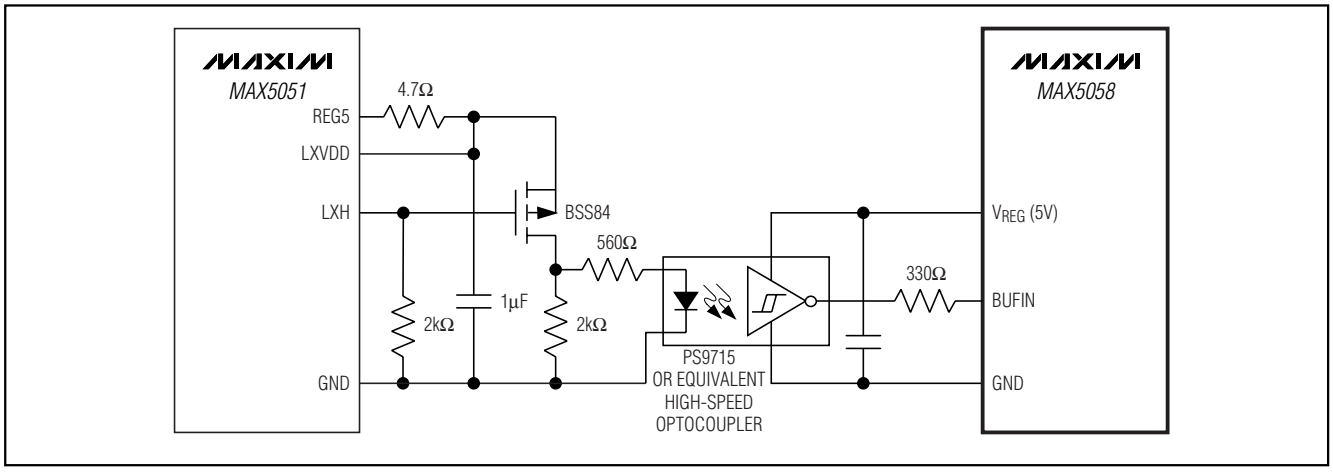


Figure 4. Interface of MAX5058 to MAX5051 Using a High-Speed Optocoupler

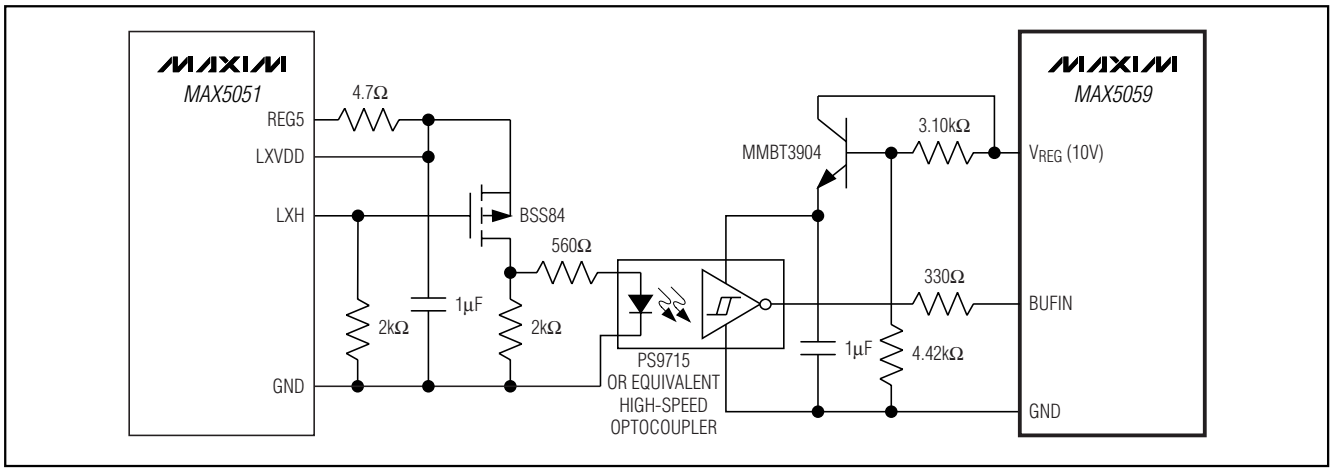


Figure 5. Interface of MAX5059 to MAX5051 Using a High-Speed Optocoupler

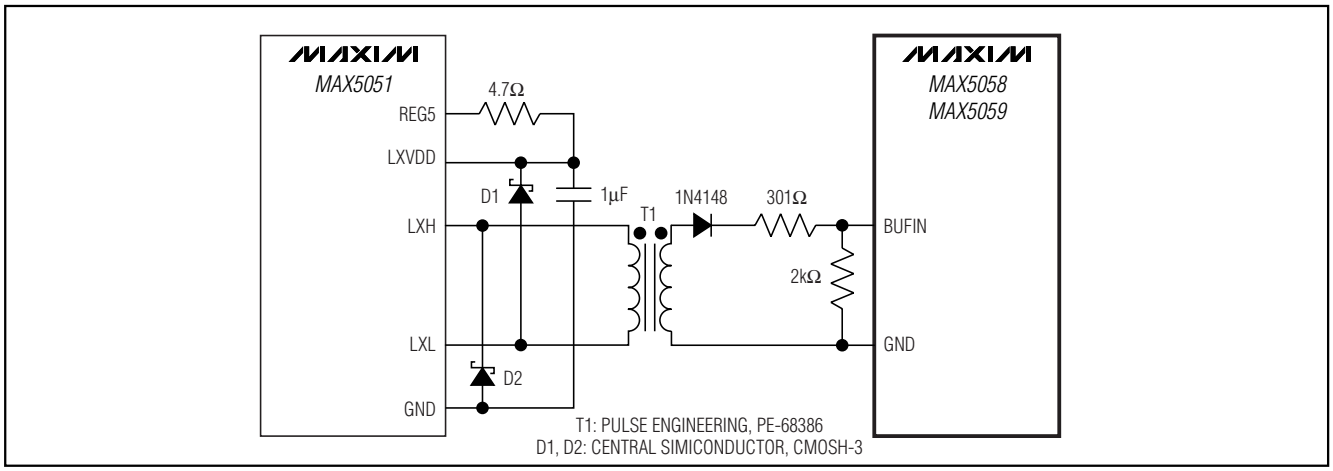


Figure 6. Interface Circuit to MAX5051 Using a Pulse Transformer

Reverse-Current Prevention in Synchronous Rectifiers

One benefit of secondary-side synchronous rectification is increased efficiency. Another benefit is that it allows the inductor current to remain continuous throughout the operating load range. This results in constant loop dynamics that are easy to compensate.

In some cases, it may be necessary to turn off the freewheeling MOSFET when the current through this device attempts to flow from drain to source. Turning off this MOSFET can be done to enhance efficiency at low output current. When multiple power supplies are paralleled, the power supply with the highest output voltage has a tendency to source current into the power-supply outputs with lower output voltage. Turning off the freewheeling MOSFET also prevents this current back-flow.

When the inductor current is allowed to become discontinuous, the loop dynamics change and the circuit must be compensated accordingly to accommodate stable continuous and discontinuous mode operation.

Turning off the freewheeling MOSFET is accomplished by using the zero-current comparator (pins ZCP and ZCN). Use this comparator to sense reverse current in the freewheeling MOSFET and turn off the device by pulling QSYNC low. An internal latch prevents the freewheeling MOSFET from turning on until the off-time of the next cycle.

Reference Current

The MAX5058/MAX5059 do not have an explicit reference voltage generator. Instead, they contain a 1%-accurate trimmed 50µA current source. This allows significant flexibility in setting the reference voltage. In some cases, the output-voltage resistive divider, consisting of R1 and R2 in the *Typical Application Circuit*, can be eliminated by selecting a suitable resistor value at the I_{REF} pin. This reduces the error that the output voltage-divider may add. Use a low-value bypass capacitance at this pin to eliminate noise. Typical values for this capacitance are calculated by considering the pole that it presents with R12. This pole must be placed well beyond the frequency range of interest of the current-share loop. Use values less than 2.2nF.

Error Amplifier

The MAX5058/MAX5059 incorporate a 1.3MHz unity gain-bandwidth error amplifier with inputs INV, I_{REF}, and output COMPV. I_{REF} is the noninverting input and also serves as the reference voltage generator with the internal 50µA current source and the external resistor connected from I_{REF} to GND. INV is the inverting input and connects to the center of a resistive divider from OUT to INV to GND. The output of the error amplifier, COMPV, connects to the cathode of the LED in the optocoupler to control the diode current that transmits the error signal back to the primary-side controller. An open-drain-output error amplifier simplifies interfacing with the feedback optocoupler. Use this error amplifier the same way as the industry-standard TL431 shunt reference. The open-drain output provides flexibility that may be necessary when additional functionality such as secondary current-limit regulation is required. Unlike the TL431, the output of the internal error amplifier of the MAX5058/MAX5059 is guaranteed to be a maximum of 200mV with a 5mA drain current, compared to 2.5V for the TL431 and 1.24V for the TLV431.

In some cases, it is possible to avoid the use of the output voltage-divider (R1 and R2) by connecting INV to the output through just R1. This eliminates the voltage tolerance errors caused by R1 and R2. Output voltage in this configuration is set directly by using a suitable resistor at I_{REF}. Figure 7 shows this configuration.

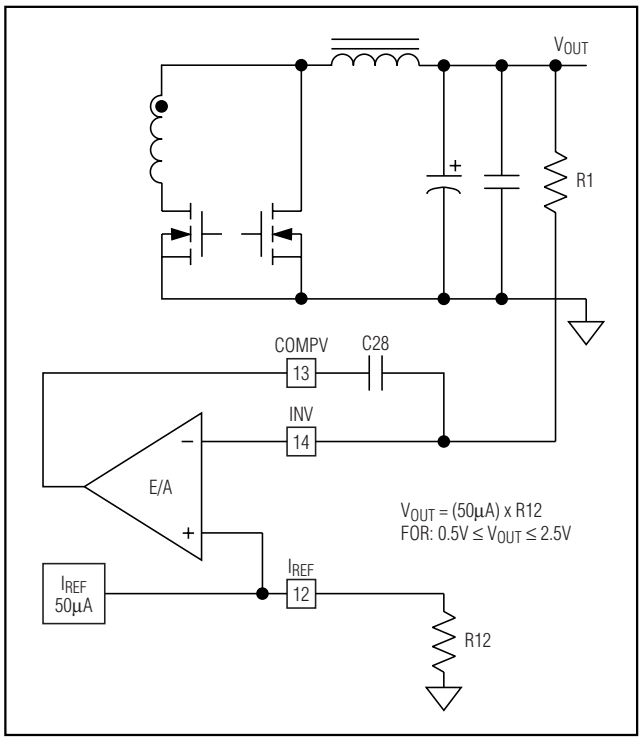


Figure 7. Output Voltage Regulation for 0.5V ≤ V_{OUT} ≤ 2.5V

Parallelable Secondary-Side Synchronous Rectifier Driver and Feedback-Generator Controller ICs

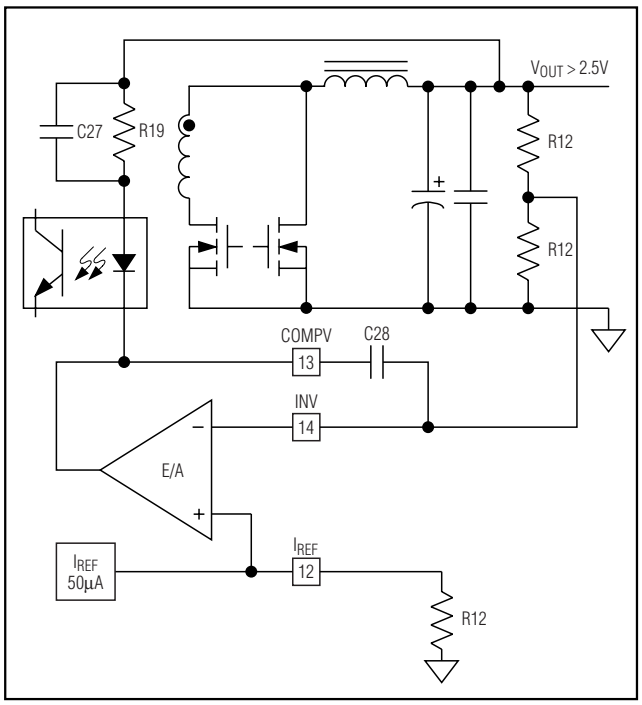


Figure 8. Optocoupler Connection for V_{OUT} > 2.5V

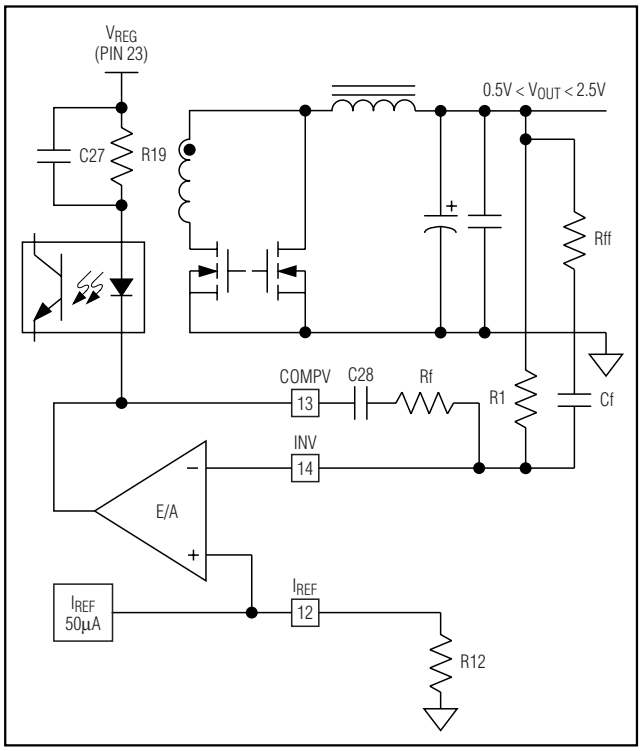


Figure 9. Optocoupler Connection for V_{OUT} < 2.5V

Figure 8 shows a typical configuration with output voltages high enough (V_{OUT} > 2.5V) to allow a typical optocoupler to be fully biased. In this case, there are two feedback paths—one though the error amplifier and one through the output-connected optocoupler. This second feedback path must be considered when compensating the overall feedback loop.

Figure 9 shows a typical configuration with an optocoupler for output voltages lower than 2.5V. In this case, the direct connection of the optocoupler to the output is not possible. There is only one feedback path and the error-amplifier feedback network must be designed accordingly.

Figure 10 shows the simplified block diagram for the error amplifier.

Voltage Margining

The margining inputs MRGU (margin up) and MRGD (margin down) control two internal MOSFETs with open-drain outputs at RMGU and RMGD, respectively. When margining is used, connect two pullup resistors from RMGU and RMGD to I_{REF}. A logic-high voltage at MRGU causes QMU (see Figure 1) to open, increasing the equivalent resistance at I_{REF} and the reference voltage (V_{IREF}). The error-amplifier inverting input, INV, tracks I_{REF} and forces the primary-side controller to increase the output voltage. MRGD has the opposite effect. When a logic high is applied to MRGD, QMD turns on, decreasing the equivalent resistance at I_{REF} and effectively reducing V_{IREF}. This causes INV to track and force the primary-side controller to reduce the output voltage.

The margining inputs MRGU and MRGD are internally pulled to GND with 40kΩ resistors. When margining is not used, the inputs can be left floating or connected to GND to make V_{IREF} = 50µA × R12.

Calculation Procedure for Output-Voltage Setting Resistors and Margining

Use the following step-by-step procedure to calculate the output-voltage setting and margining resistors (see the *Typical Application Circuit*):

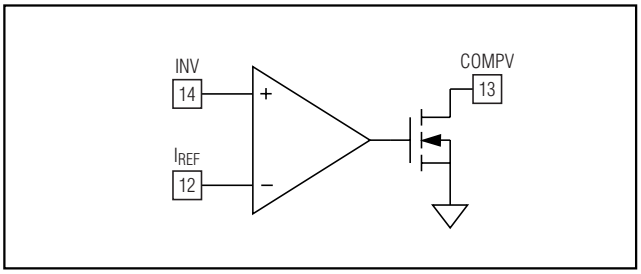


Figure 10. Simplified Error-Amplifier Diagram

1) Select a parallel equivalent resistance R_{eq} value to produce the nominal reference voltage. For example, R_{eq} = 35.4kΩ gives you V_{IREF} = 1.77V.
2) Select the margin-up percentage value:

$$\Delta U = 5\%$$

3) Calculate R_{32}:

$$R_{32} = R_{eq} \times \frac{100\% + \Delta U}{\Delta U}$$

R_{32} = 743.4kΩ. Calculated

Select the nearest 0.1% value.

R_{32} = 741kΩ. Selected

4) Calculate R_{12}:

$$R_{12} = \frac{R_{32} \times \Delta U}{100\%}$$

R_{12} = 37.05kΩ. Calculated

Select the nearest 0.1% value.

R_{12} = 37kΩ. Selected

5) Select the margin-down percentage value:

$$\Delta D = 5\%$$

6) Recalculate R_{eq} with the selected values:

$$R_{eq} = \frac{R_{12}R_{32}}{R_{12} + R_{32}}$$

R_{eq} = 35.24kΩ.

7) Calculate R_{33}:

$$R_{33} = \frac{100\% \times R_{eq} \times R_{12}}{R_{12} \times (100\% + \Delta D) - 100\% \times R_{eq}}$$

R_{33} = 361.186kΩ. Calculated

Select the nearest 0.1% value:

R_{33} = 361kΩ. Selected

8) Calculate the reference voltage with the selected chosen values:

V_{IREF} = 50µA × R_{eq}. R_{eq} from step 6.

V_{IREF} = 1.762V.

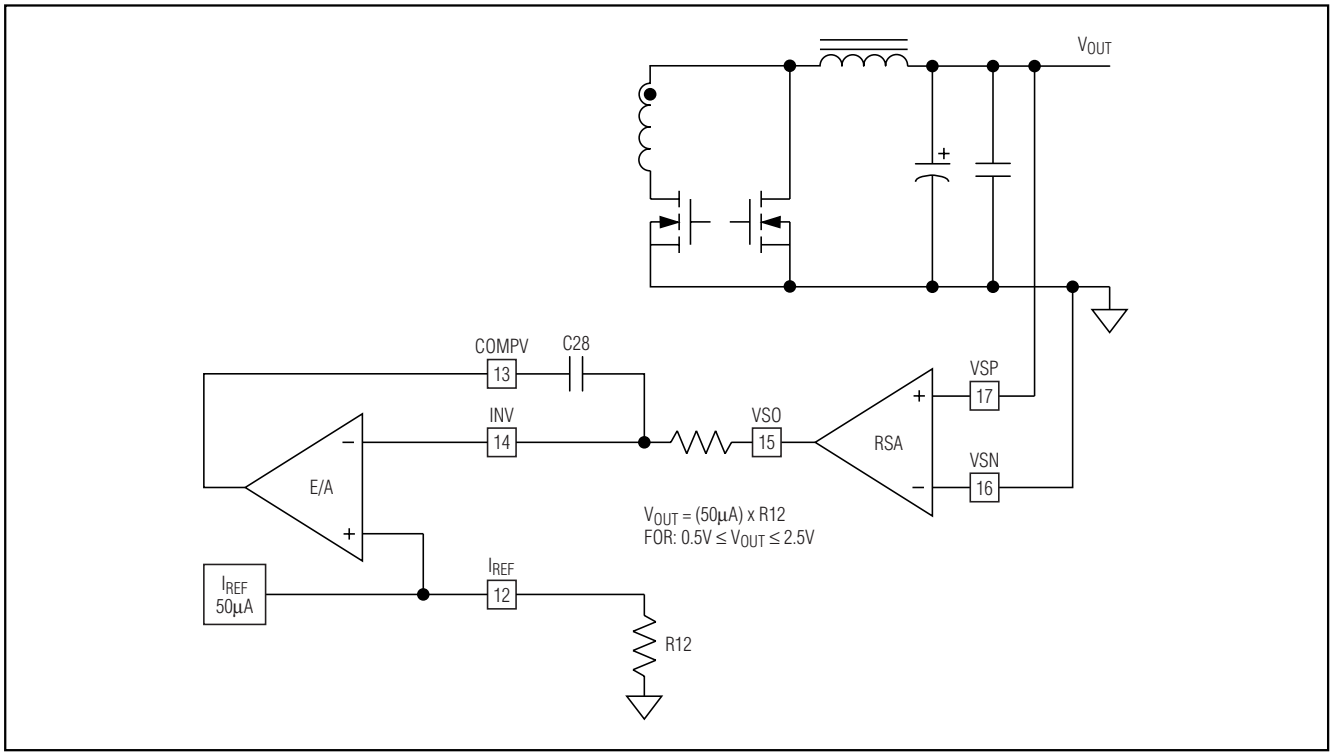


Figure 11. Remote-Sense Amplifier Connection for 0.5V ≤ V_{OUT} ≤ 2.5V

Parallelable Secondary-Side Synchronous Rectifier Driver and Feedback-Generator Controller ICs

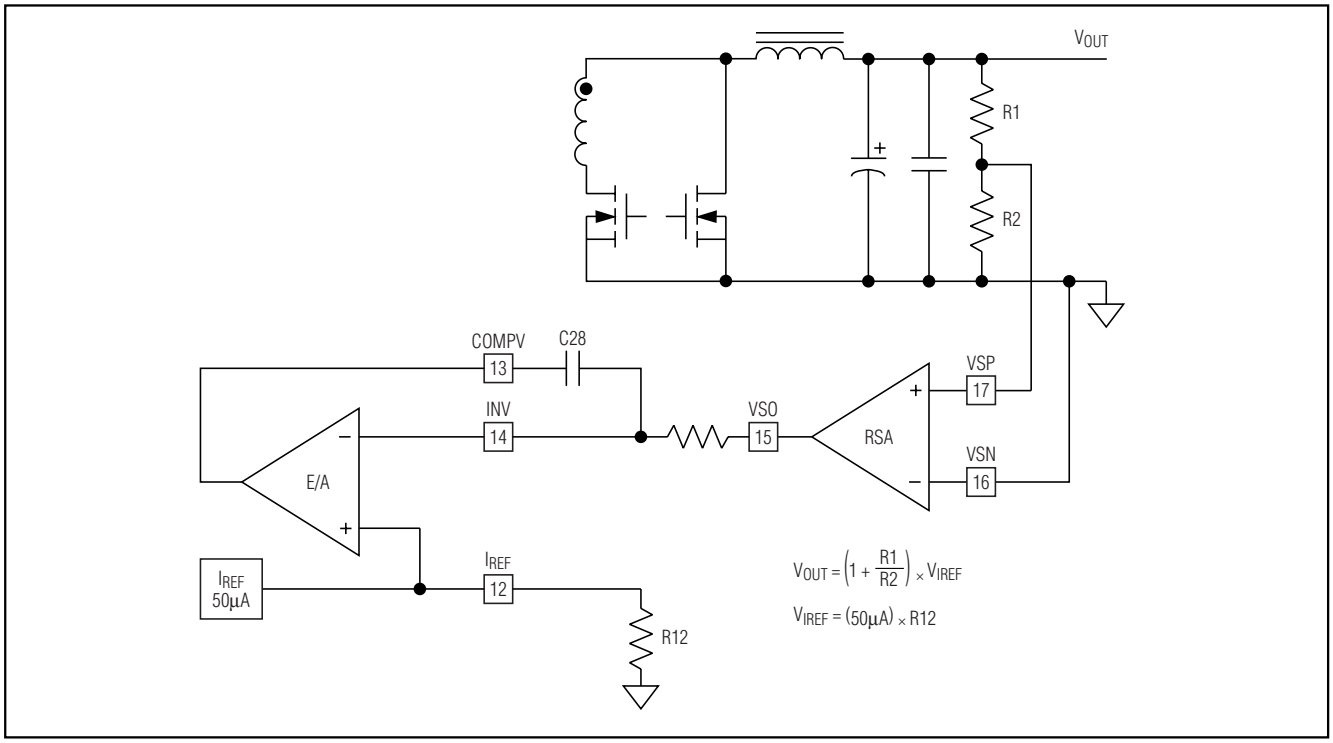


Figure 12. Remote-Sense Amplifier Connection for V_{OUT} > 2.5V (or any Other Arbitrary Voltage)

9) Select a value for R_1 and calculate R_2 for V_{OUT} = 3.3V:

$$R_1 = 19.1k\Omega$$

$$R_2 = \frac{V_{IREF}}{V_{OUT} - V_{IREF}} R1$$

R_2 = 21.882kΩ.

Select the nearest 1% value.

R_2 = 21.8kΩ.

When margining is not used, substitute R_{12} for R_{eq} in step 8 and go to step 9.

Remote-Sense Amplifier

Use the remote-sense amplifier (RSA in Figure 1) to directly sense the voltage across the load, compensating for voltage drops in PC board tracks or load connection wires. The remote-sense amplifier is a unity-gain amplifier with sufficient bandwidth to not interfere with the normal operation of the voltage-control loop. Direct sensing of the output voltage is possible if the output voltage is between 0.5V to 2.5V. Figure 11 shows this configuration. Figure 12 shows the use of the remote-sense amplifier with a voltage-divider. The remote-sense amplifier has an input bias current of 100µA. The impedance of R1 and R2 must be kept low in this configuration to avoid excessive errors in the output-voltage set point.

Current Sharing

When multiple power modules are providing power to the same load, the load current must be shared equally to provide the best reliability and thermal distribution. The MAX5058/MAX5059 contain circuitry that enable current sharing among paralleled power supplies without requiring an explicit controlling master circuit. Current sharing is accomplished by connecting together the current-share bus pins (SFP and SFN) of all paralleled power supplies (see Figure 13), thus creating a current-force/share bus. The voltage level on this differential bus is proportional to the output current of the power supply that has the highest current compared to the other supplies. The number of power supplies that can be paralleled with this method is limited only by practical considerations.

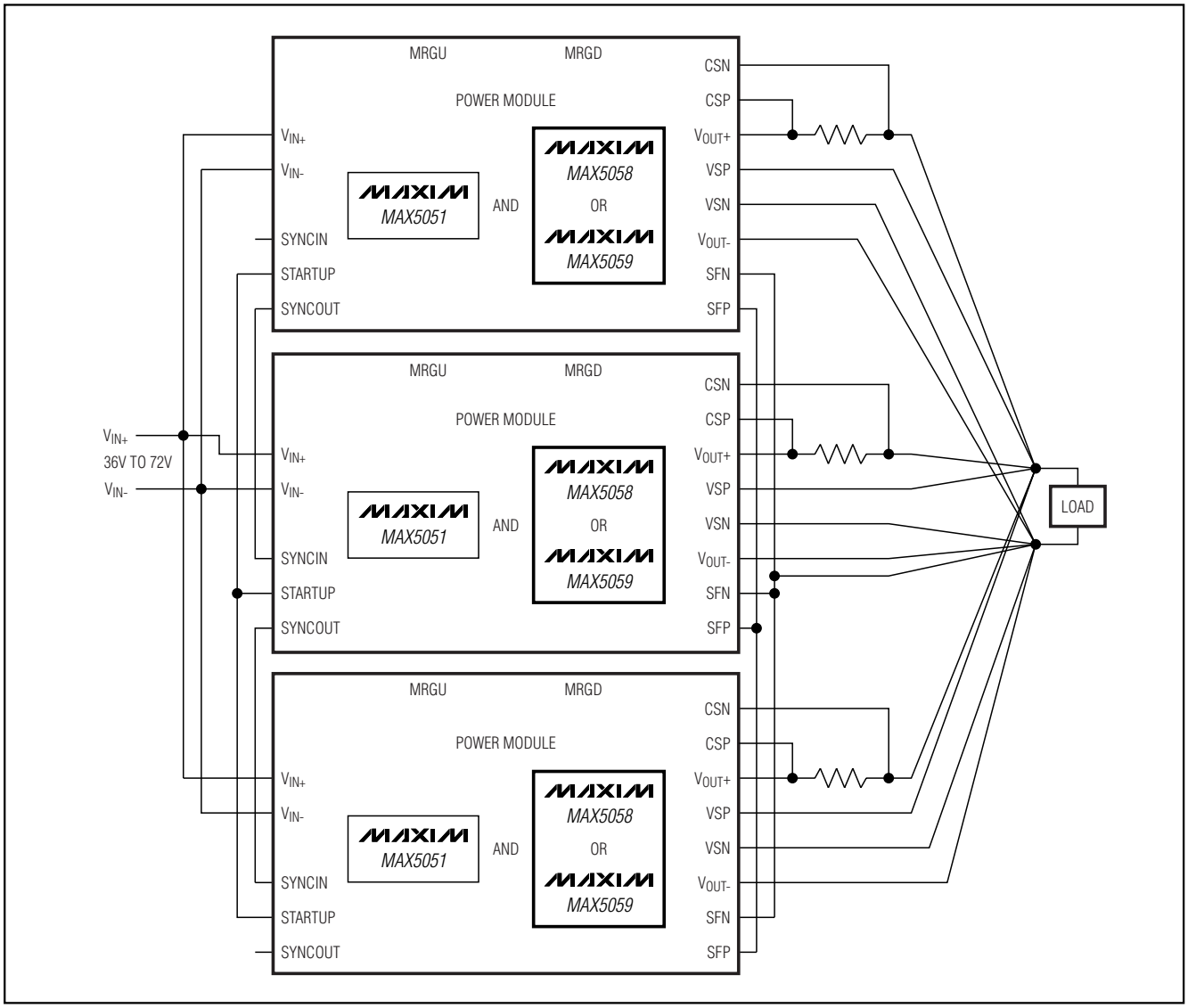


Figure 13. Paralleling Multiple Power-Supply Modules for Current Sharing

When the MAX5051 is used as the primary-side controller, additional benefits are also realized with its special paralleling pins. The MAX5051 allows simultaneous shutdown and wake-up, as well as frequency synchronization and 180 degree out-of-phase operation of each connected primary.

The current-share loop consists of the following functional blocks:

- A diode ORed force amplifier that connects with the other modules and forces the bus to carry a voltage proportional to the highest current among the modules.
- A sense amplifier that senses this share-bus voltage and applies it to internal circuitry.
- A fixed gain of 20, current-sense amplifier that senses the output current through a sense resistor.
- A current-adjust amplifier that functions as an error-amplifier block in the current-share loop.
- A voltage-to-current (Vtol) block that adds a small amount of current to the reference current, increasing the reference voltage and enabling the module to share more current.

Parallelable Secondary-Side Synchronous Rectifier Driver and Feedback-Generator Controller ICs

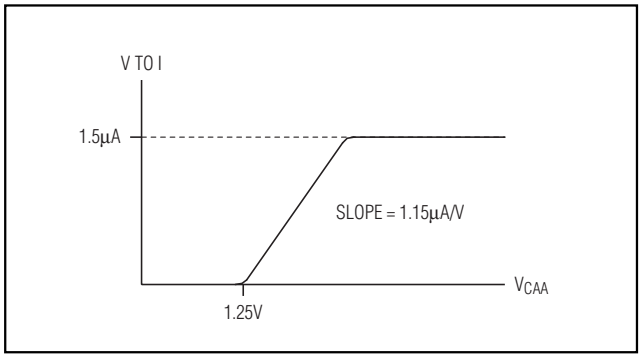


Figure 14. Transfer Function Curve of the V to I Block

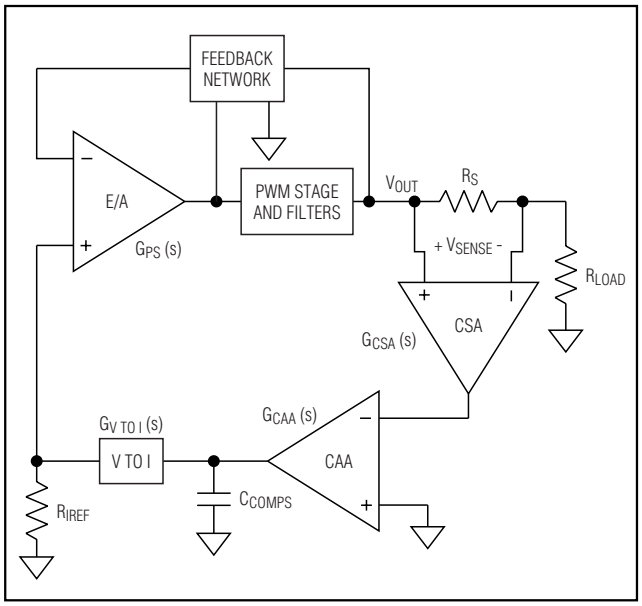


Figure 15. Small-Signal Equivalent Current-Share Control Loop

The adjustment range and thus the sharing capability of the modules is limited by the amount of additional output voltage boost possible through the VtoI block. The typical voltage boost is +3% (i.e., 1.5µA/50µA). Figure 14 shows the transfer function of the VtoI block. This adjustment range also sets a limit on the amount of voltage drop allowed for current sharing. For effective current sharing, the sum of all voltage drops must be kept below 3% and the output-to-load connection drop of each power module must be kept equal.

Current-sharing functions follow:

The voltage across the current-sense resistor for each module is sensed and compared to the voltage on the current-share bus. The voltage on the current-share bus represents the current from the module that has the highest output current compared to the other modules. Each module compares its current to this maximum current. If its current is less than the maximum, then the module increases its reference current with the VtoI block. This raises the reference voltage presented at the noninverting input of the error amplifier. With a higher reference voltage, the output voltage of the module rises in an attempt to increase its output current. This process continues until the currents balance between the modules.

The current-adjust amplifier (see Figure 1) has an offset at its inverting input that requires the share-bus voltage to reach 40mV before the current-share control loop attempts to regulate the output-load-current balance. Thus, the current-share regulation does not begin until the current-sense signals have exceeded 2mV (i.e., 42mV/20).

Figure 15 shows the simplified equivalent small-signal circuit of the current-share control loop. The current-adjust amplifier represents the error amplifier in this loop. The command signal, which is the voltage across the SFP and SFN pins, is applied to the noninverting input of this amplifier. For small-signal analysis, the noninverting pin is shown grounded in Figure 15. This is a low-bandwidth loop.

Assuming a much smaller unity-gain crossover bandwidth (f_{CS}) for the current-share loop compared to the main output-voltage-regulation loop (i.e., $f_{CS} << f_C$), the open-loop gain of the current-share loop can be written as:

$$G_T(s) = G_{SFA}(s) \times \left(\frac{G_{CAA}(s)}{s \times C_{COMPS}} \right) \times \left(G_{VtoI}(s) \times R_{IREF} \right) \times G_{PS}(s) \times \frac{R_S}{R_S + R_{LOAD}}$$

where f_{CS} is the unity-gain crossover frequency of the current-share loop (typically 10Hz to 100Hz), f_C is the unity-gain crossover frequency of the main output loop, $G_{PS}(s)$ is the gain of the power stage from the reference voltage input of the error amplifier to the output ($G_{PS} = V_{OUT}/V_{IREF}$), R_S is the current-sense resistor, and R_{LOAD} is the load resistance. Note that the current-share loop bandwidth is highest for the lowest value of R_{LOAD} (maximum load).

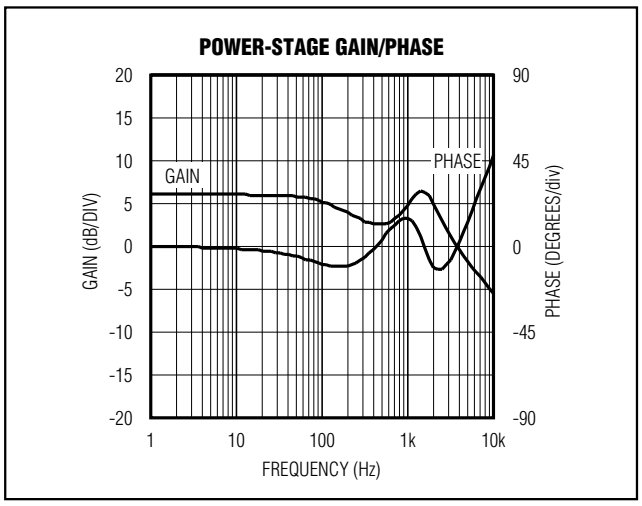


Figure 16. Idealized (with Ideal Power Stage and Optocoupler) Frequency Response ($G_{PS}(s)$) from Noninverting Input of the Error Amplifier to the Output of the Power Supply for the Typical Application Circuit of Figure 18

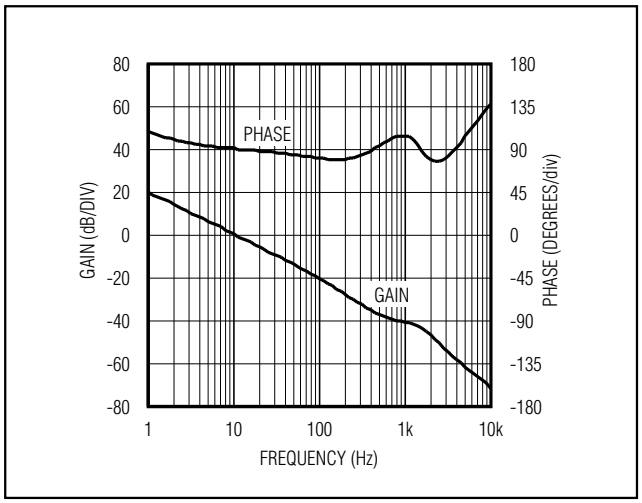


Figure 17. Overall Open-Loop Response of the Current-Share Loop

Figure 16 shows the idealized small-signal response of the *Typical Application Circuit* from the noninverting input of the error amplifier to the output. This response shows that the unity-gain crossover frequency of the current-share loop can easily be placed between 10Hz and 100Hz, while at the same time avoiding interaction with the main voltage-control loop.

For frequencies below 100Hz, $G_T(s)$ can be written as (using the DC gain value for $G_{PS}(s)$):

$$G_T(s) = 20 \times \frac{(500\mu S)}{s \times C_{COMPS}} \times (1.15\mu A/V) \times R_{IREF} \times \frac{V_{OUT}}{V_{IREF}} \times \frac{R_S}{R_S + R_{LOAD}}$$

Equating $|G_T| = 1$ and solving for C_{COMPS} yields:

$$C_{COMPS} = \frac{(36.61\mu F \times Hz/V) \times R_S \times V_{OUT}}{f_{CS} \times (R_S + R_{LOAD})}$$

The current-sharing loop is compensated with a capacitor from COMPS to GND. This results in a dominant pole that forces the loop gain of the current-share loop to cross 0dB with a single pole (20dB/decade) rolloff.

When $R_{LOAD} >> R_S$, the above can be simplified further.

$$C_{COMPS} = \frac{(36.61\mu F \times Hz/V) \times R_S \times V_{OUT}}{f_{CS} \times R_{LOAD}}$$

Example:

R_S = 2mΩ

V_{OUT} = 3.3V

f_{CS} = 10Hz

R_{LOAD} = 0.22Ω

$$C_{COMPS} = \frac{(36.61\mu F \times Hz/V) \times (0.002\Omega) \times (3.3V)}{(10Hz) \times (0.22\Omega)} \cong 0.11\mu F$$

The resulting overall open-loop response of the current-share control loop is shown in Figure 17.

Applications Information

Isolated 48V Input Power Supply

Figure 18 shows a complete design of an isolated synchronously rectified power supply with a +36V to +75V telecom input voltage range. This design uses the MAX5051 as the primary-side controller and the MAX5058 as the secondary-side synchronous rectifier driver. Figures 19 though 24 show some of the performance aspects of this power-supply design. This power supply can sustain a continuous short circuit at its output terminals. This circuit is available as a completely built and tested evaluation kit (MAX5058EVKIT).

Parallelable Secondary-Side Synchronous Rectifier Driver and Feedback-Generator Controller ICs

Typical Application Circuit

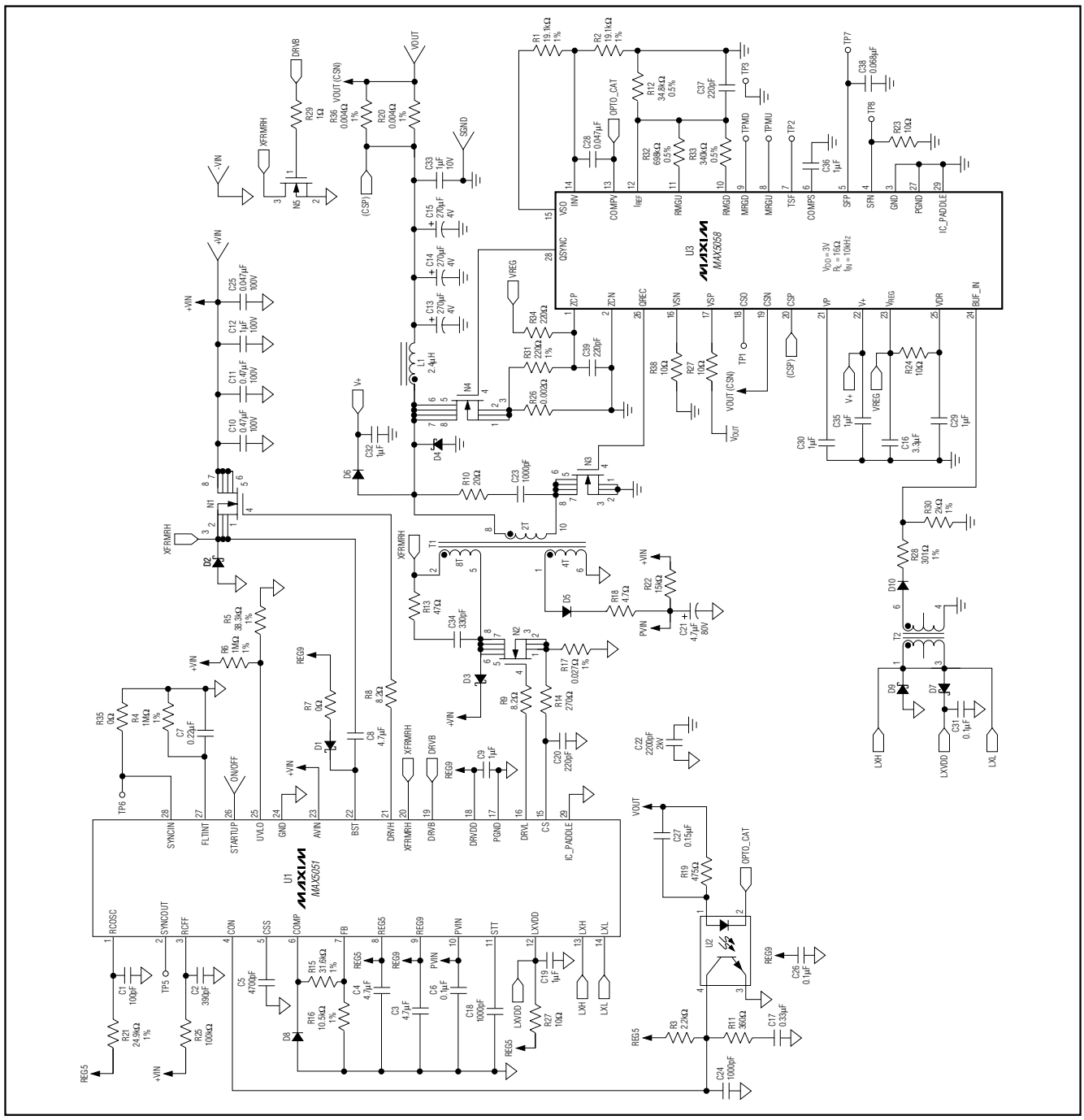


Figure 18. Schematic of a +48V Input, 3.3V at 15A Output, Synchronous Rectified, Isolated Power Supply

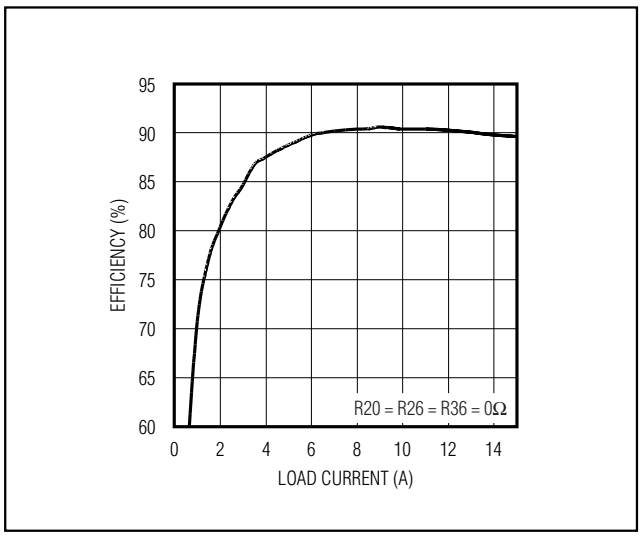


Figure 19. Efficiency at Nominal 3.3V Output Voltage vs. Load Current (48V Nominal Input Voltage)

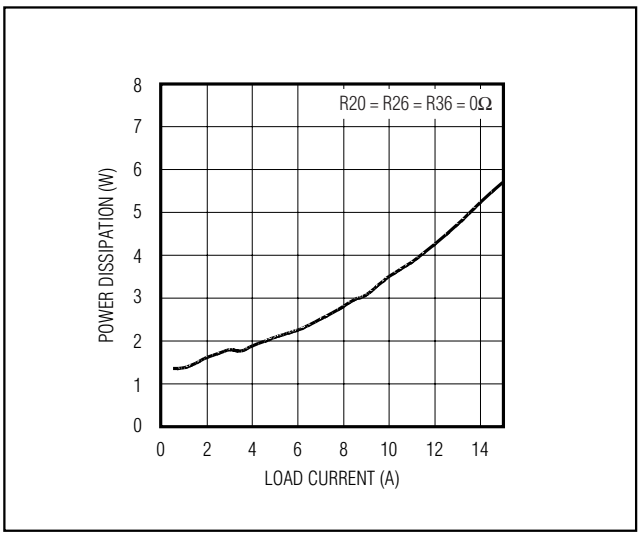


Figure 20. Power Dissipation at Nominal 3.3V Output Voltage vs. Load Current (48V Nominal Input Voltage)

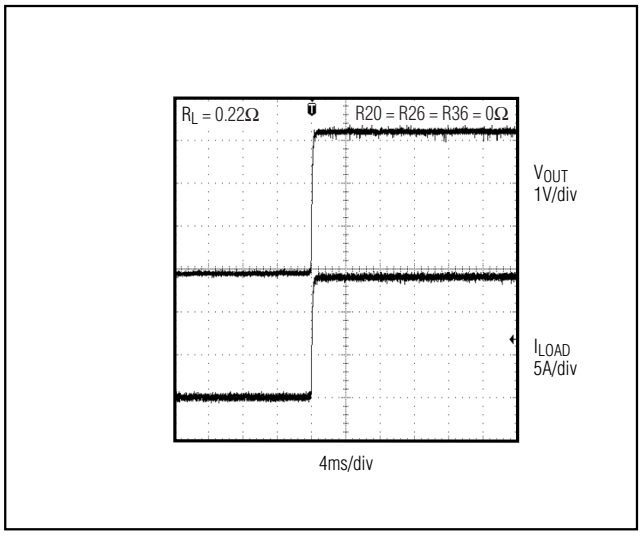


Figure 21. Turn-On Transient at Full Load (Resistive Load) V_{OUT}

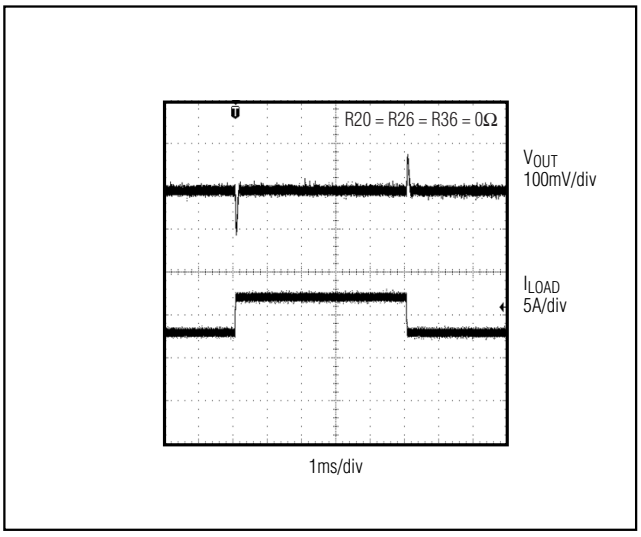


Figure 22. Output Voltage Response to Step Change in Load Current (I_{LOAD} from 50%, max to 75%, max)

Parallelable Secondary-Side Synchronous Rectifier Driver and Feedback-Generator Controller ICs

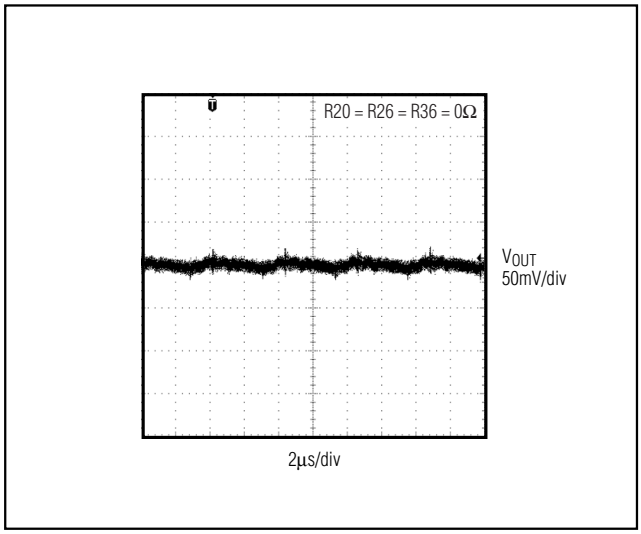


Figure 23. Output Voltage Ripple at +48V Nominal Input Voltage and Full Load Current (Scope Bandwidth = 20MHz)

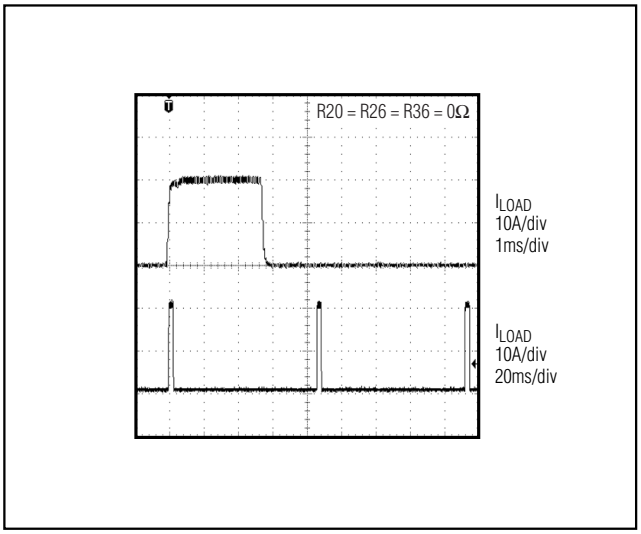
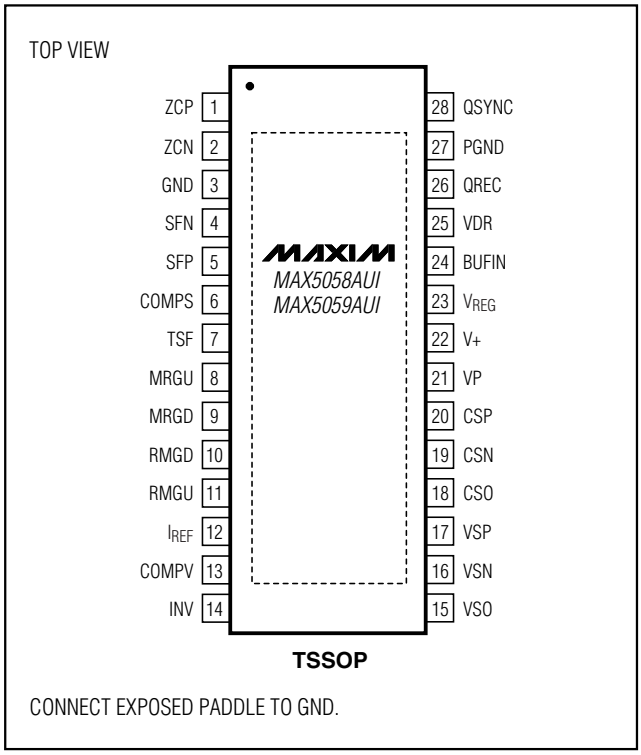


Figure 24. Load Current (10A/div) as a Function of Time when the Converter Attempts to Turn On into a 50mΩ Short Circuit

Pin Configuration



Chip Information

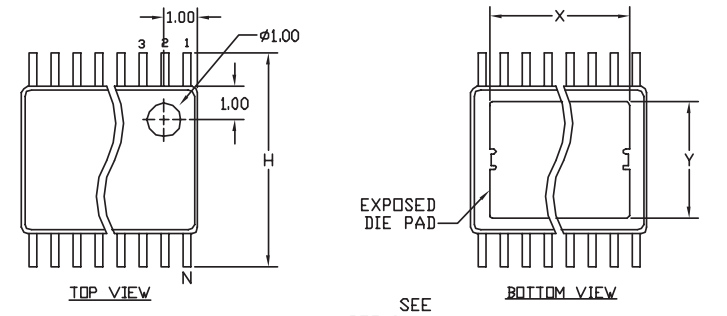
TRANSISTOR COUNT: 1762

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP 4.4mm BODY.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	--	1.10	--	0.043
A1	0.05	0.15	0.002	0.006
A2	0.85	0.95	0.33	0.037
b	0.19	0.30	0.007	0.012
b1	0.19	0.25	0.007	0.010
c	0.090	0.20	0.004	0.008
c1	0.090	0.135	0.004	0.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
H	6.25	6.50	0.246	0.256
L	0.50	0.70	0.020	0.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	0.112	0.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
ABT-1	14	D	4.90	5.10	0.193	0.201
		X	2.95	3.25	0.116	0.128
ABT	16	D	4.90	5.10	0.193	0.201
		X	2.85	3.15	0.112	0.124
ACT	20	D	6.40	6.60	0.252	0.260
		X	4.00	4.34	0.157	0.171
AET	28	D	9.60	9.80	0.378	0.386
		X	5.35	5.65	0.211	0.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES, ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0108	C	1/1