



ELECTRICAL SPECIFICATIONS:

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|-----|--|---|
| 1.0 | URNS RATIO (P7-P6-P8) : (J3-J6) | : 1CT : 1CT ± 3% |
| | (P1-P3-P2) : (J1-J2) | : 1CT : 1CT ± 3% |
| 2.0 | INDUCTANCE (P7-P8) | : 350uH MIN. @ 0.1V , 100KHz, 8mA DC Bias |
| | (P1-P2) | : 350uH MIN. @ 0.1V, 100KHz, 8mA DC Bias |
| 3.0 | LEAKAGE INDUCTANCE P8-P6-P7 (WITH J6 AND J3 SHORT) | : 0.3uH MAX. @ 1MHz |
| | P2-P3-P1 (WITH J2 AND J1 SHORT) | : 0.3uH MAX. @ 1MHz |
| 4.0 | INTERWINDING CAPACITANCE (P8,P6,P7) TO (J6,J3) | : 30pf MAX @ 1MHz |
| | (P2,P3,P1) TO (J2,J1) | : 30pf MAX @ 1MHz |
| 5.0 | DC RESISTANCE (J6-J3)=(J2-J1) | : 1.2 ohms Max. |

NOTES

1.0 PINS WITHOUT ELECTRICAL CONNECTION ARE OMITTED.

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6.0 RETURN LOSS: $\langle P7-P8 \rangle = 100 \text{ } \Omega$ MS AND $\langle P1-P2 \rangle = 100 \text{ } \Omega$ M REF.
 1MHz TO 30MHz : 18dB MIN.
 30MHz TO 80MHz : 12dB MIN.
 NOTE: 100 Ω MS CONNECTED TO $\langle J2-J1 \rangle$ OR $\langle J6-J3 \rangle$.



7.0 VOLTAGE WITHSTAND:
 $\langle J1, J2 \rangle$ TO $\langle P1, P2 \rangle$: 1500 VAC
 $\langle J3, J6 \rangle$ TO $\langle P7, P8 \rangle$: 1500 VAC

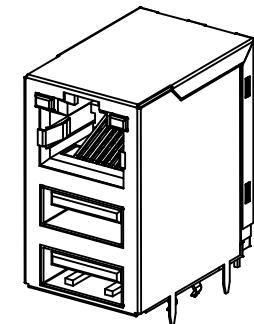
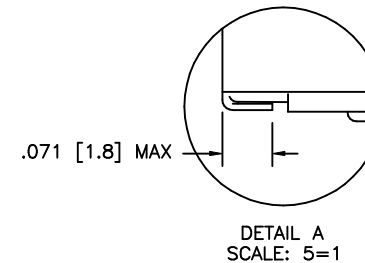
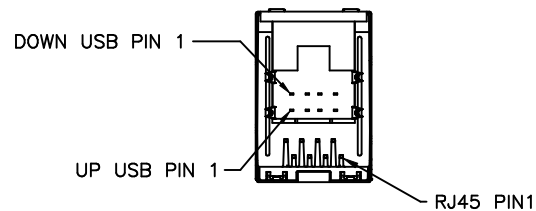
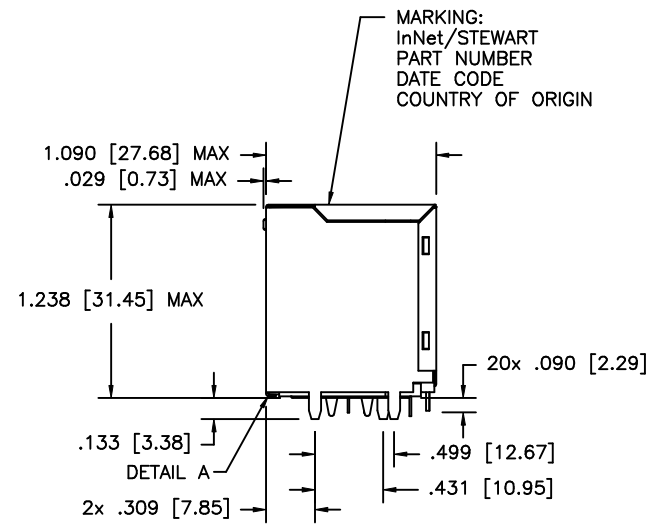
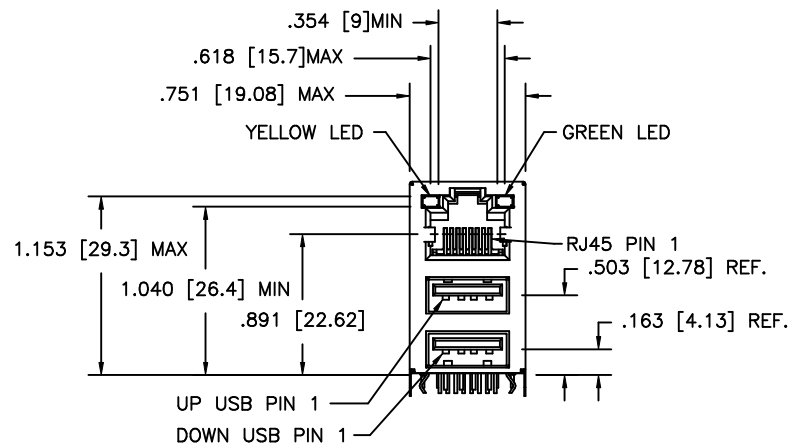
8.0 INSERTION LOSS: $R_S = R_L = 100 \text{ ohms}$
 100KHz TO 100MHz 1.1 dB TYP

9.0 RISE TIME: $R_S = 100 \text{ } \Omega$ MS AND $R_L = 100 \text{ } \Omega$ MS
 OUTPUT VOLTAGE = 1 V peak 3.0 nS MAX
 PULSE WIDTH = 112nS 3.0 nS MAX

10.0 CROSS TALK:
 1-100 MHz 30 dB TYP

11.0 COMMON TO COMMON MODE ATTENUATION:
 1MHz TO 100MHz 35dB TYP

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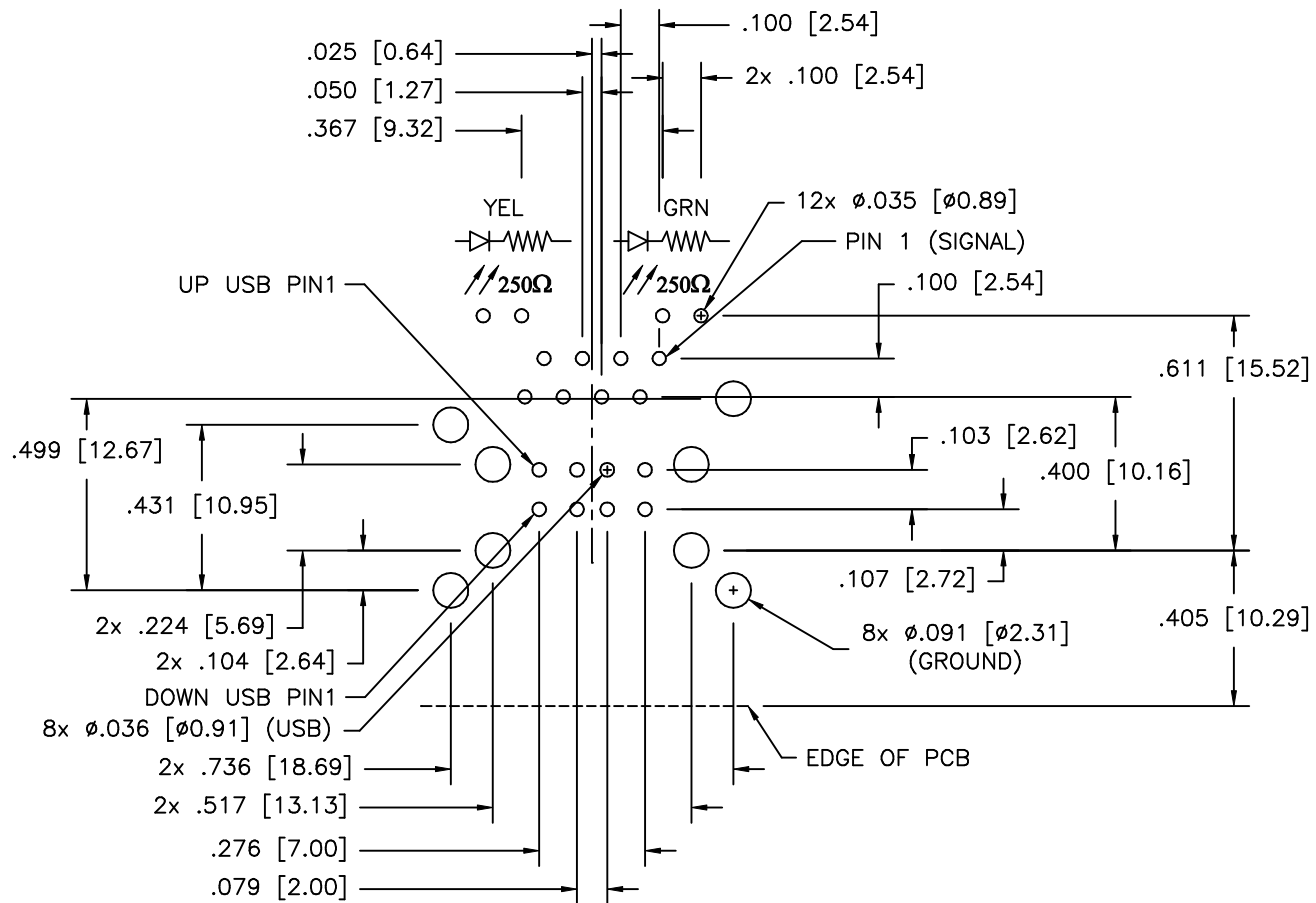


NOTES:

- 1.0 TOLERANCE COMPLY WITH FCC DIMENSION REQUIREMENTS.
- 2.0 PIN NOT ELECTRICALLY CONNECTED MAY BE OMITTED. SEE ELECTRICAL DRAWING FOR OMITTED PINS.
- 3.0 MATERIAL:
 - PLASTIC: UL94V-Ø
 - TERMINAL USB: PLATING PER USB SPEC 2.0
 - TERMINAL RJ45: 50 MICROINCHES Au OVER 50 MICROINCHES Ni OVER PHOSBRONZE SHIELD, BOTH USB AND RJ45: BRASS PLATED W/EITHER Ni OR TIN-LEAD
- 4.0 GENERAL TOLERANCE: ±.005 [.127]



PRELIMINARY
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PC BOARD LAYOUT COMPONENT SIDE SHOWN
 TOLERANCE: \pm .003 [.08] UNLESS OTHERWISE SPECIFIED

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