Document order number: MM908E626
Rev 3.0, 12/2005

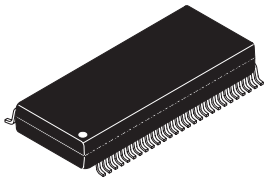
Integrated Stepper Motor Driver with Embedded MCU and LIN Serial Communication

908E626

STEPPER MOTOR DRIVER WITH EMBEDDED MCU AND LIN

The 908E626 is an integrated single-package solution that includes a high-performance HC08 microcontroller with a *SMARTMOS*™ analog control IC. The HC08 includes flash memory, a timer, enhanced serial communications interface (ESCI), an analog-to-digital converter (ADC), serial peripheral interface (SPI) (only internal), and an internal clock generator (ICG) module. The analog control die provides fully protected H-Bridge outputs, voltage regulator, autonomous watchdog, and local interconnect network (LIN) physical layer.

The single-package solution, together with LIN, provides optimal application performance adjustments and space-saving PCB design. It is well suited for the control of automotive stepper applications like climate control and light-levelling.



DWB SUFFIX
98ARL105910
54-TERMINAL SOICWB-EP

Device	Temperature Range (T_A)	Package
MM908E626AVDWB	-40°C to 115°C	54 SOIC WB-EP

Features

- High-Performance M68HC08EY16 Core
- 16 K Bytes of On-Chip Flash Memory
- 512 Bytes of RAM
- Internal Clock Generation Module
- Two 16-Bit, 2-Channel Timers
- 10-Bit Analog-to-Digital Converter
- Four Low $R_{DS(ON)}$ Half-Bridge Outputs
- 13 Microcontroller I/Os

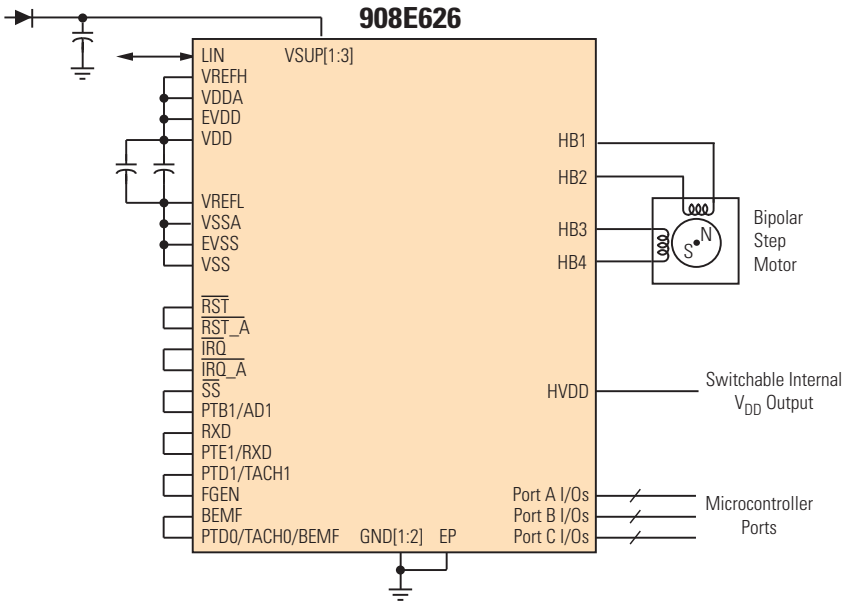


Figure 1. 908E626 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

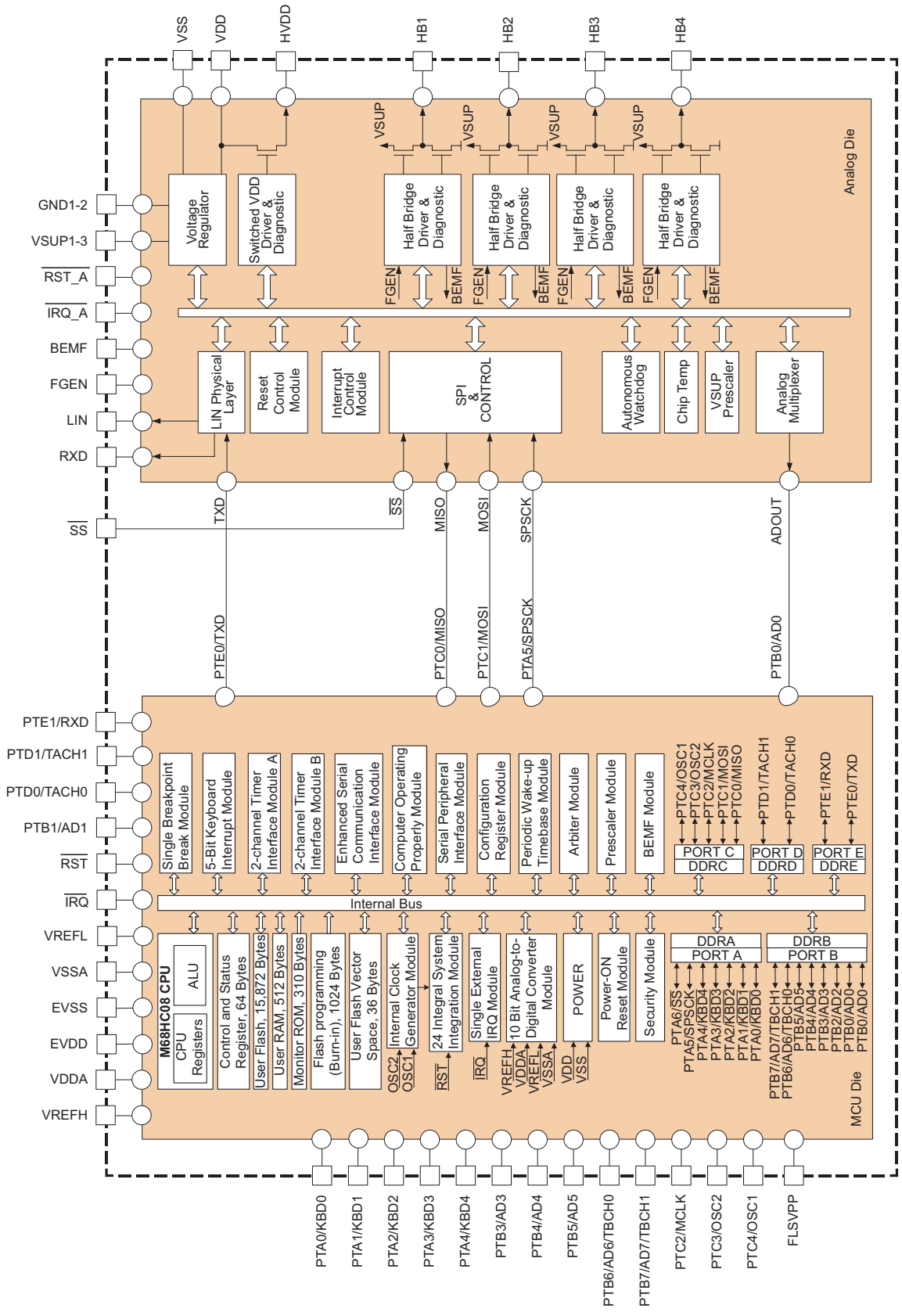


Figure 2. Figure 1. 908E626 Simplified Internal Block Diagram

TERMINAL CONNECTIONS

Transparent Top View of Package

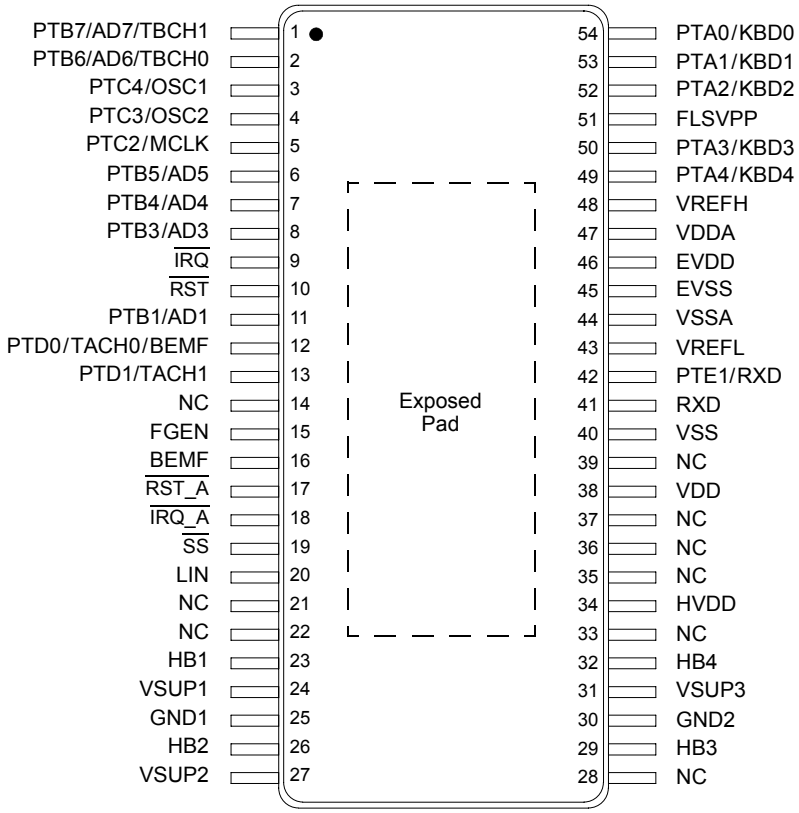


Figure 3. 908E626 Terminal Connections

Table 1. 908E626 TERMINAL DEFINITIONS

A functional description of each terminal can be found in the Functional Terminal Description section beginning on page 14.

Die	Terminal	Terminal Name	Formal Name	Definition
MCU	1 2 6 7 8 11	PTB7/AD7/TBCH1 PTB6/AD6/TBCH0 PTB5/AD5 PTB4/AD4 PTB3/AD3 PTB1/AD1	Port B I/Os	These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU.
MCU	3 4 5	PTC4/OSC1 PTC3/OSC2 PTC2/MCLK	Port C I/Os	These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU.
MCU	9	IRQ	External Interrupt Input	This terminal is an asynchronous external interrupt input terminal.
MCU	10	RST	External Reset	This terminal is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted.
MCU	12 13	PTD0/TACH0/BEMF PTD1/TACH1	Port D I/Os	These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU.
–	14, 21, 22, 28, 33, 35, 36, 37, 39	NC	No Connect	Not connected.

Table 1. 908E626 TERMINAL DEFINITIONS

A functional description of each terminal can be found in the Functional Terminal Description section beginning on page 14.

Die	Terminal	Terminal Name	Formal Name	Definition
MCU	42	PTE1/RXD	Port E I/O	This terminal is a special-function, bidirectional I/O port terminal that can is shared with other functional modules in the MCU.
MCU	43 48	VREFL VREFH	ADC References	These terminals are the reference voltage terminals for the analog-to-digital converter (ADC).
MCU	44 47	VSSA VDDA	ADC Supply Terminals	These terminals are the power supply terminals for the analog-to-digital converter.
MCU	45 46	EVSS EVDD	MCU Power Supply Terminals	These terminals are the ground and power supply terminals, respectively. The MCU operates from a single power supply.
MCU	49 50 52 53 54	PTA4/KBD4 PTA3/KBD3 PTA2/KBD2 PTA1/KBD1 PTA0/KBD0	Port A I/Os	These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU.
MCU	51	FLSVPP	Test Terminal	For test purposes only. Do not connect in the application.
Analog	15	FGEN	Current Limitation Frequency Input	This is the input terminal for the half-bridge current limitation PWM frequency.
Analog	16	BEMF	Back Electromagnetic Force Output	This terminal gives the user information about back electromagnetic force (BEMF).
Analog	17	$\overline{\text{RST\_A}}$	Internal Reset	This terminal is the bidirectional reset terminal of the analog die.
Analog	18	$\overline{\text{IRQ\_A}}$	Internal Interrupt Output	This terminal is the interrupt output terminal of the analog die indicating errors or wake-up events.
Analog	19	$\overline{\text{SS}}$	Slave Select	This terminal is the SPI slave select terminal for the analog chip.
Analog	20	LIN	LIN Bus	This terminal represents the single-wire bus transmitter and receiver.
Analog	23 26 29 32	HB1 HB2 HB3 HB4	Half-Bridge Outputs	This device includes power MOSFETs configured as four half-bridge driver outputs. These outputs may be configured for step motor drivers, DC motor drivers, or as high-side and low-side switches.
Analog	24 27 31	VSUP1 VSUP2 VSUP3	Power Supply Terminals	These terminals are device power supply terminals.
Analog	25 30	GND1 GND2	Power Ground Terminals	These terminals are device power ground connections.
Analog	34	HVDD	Switchable V_{DD} Output	This terminal is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply; e.g., 3-terminal Hall-effect sensors.
Analog	38	VDD	Voltage Regulator Output	The +5.0 V voltage regulator output terminal is intended to supply the embedded microcontroller.
Analog	40	VSS	Voltage Regulator Ground	Ground terminal for the connection of all non-power ground connections (microcontroller and sensors).
Analog	41	RXD	LIN Transceiver Output	This terminal is the output of LIN transceiver.
–	EP	Exposed Pad	Exposed Pad	The exposed pad terminal on the bottom side of the package conducts heat from the chip to the PCB board.

MAXIMUM RATINGS

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any terminal may cause permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage Analog Chip Supply Voltage under Normal Operation (Steady-State) Analog Chip Supply Voltage under Transient Conditions (1) Microcontroller Chip Supply Voltage	 $V_{SUP(SS)}$ $V_{SUP(PK)}$ V_{DD}	 -0.3 to 28 -0.3 to 40 -0.3 to 6.0	V
Input Terminal Voltage Analog Chip Microcontroller Chip	 $V_{IN(ANALOG)}$ $V_{IN(MCU)}$	 -0.3 to 5.5 V_{SS}-0.3 to V_{DD}+0.3	V
Maximum Microcontroller Current per Terminal All Terminals Except VDD, VSS, PTA0:PTA6, PTC0:PTC1 Terminals PTA0:PTA6, PTC0:PTC1	 $I_{PIN(1)}$ $I_{PIN(2)}$	 ±15 ±25	mA
Maximum Microcontroller V_{SS} Output Current	I_{MVSS}	100	mA
Maximum Microcontroller V_{DD} Input Current	I_{MVDD}	100	mA
LIN Supply Voltage Normal Operation (Steady-State) Transient Conditions (1)	 $V_{BUS(SS)}$ $V_{BUS(DYNAMIC)}$	 -18 to 28 40	V
ESD Voltage Human Body Model (2) Machine Model (3) Charge Device Model (4)	 V_{ESD1} V_{ESD2} V_{ESD3}	 ±3000 ±150 ±500	V
THERMAL RATINGS			
Storage Temperature	T_{STG}	-40 to 150	°C
Operating Case Temperature (5)	T_C	-40 to 115	°C
Operating Junction Temperature(6)	T_J	-40 to 135	°C
Peak Package Reflow Temperature During Solder Mounting (7)	T_{SOLDER}	245	°C

Notes

1. Transient capability for pulses with a time of t < 0.5 sec.
2. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
3. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
4. ESD3 testing is performed in accordance with Charge Device Model, robotic (C_{ZAP} = 4.0 pF).
5. The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking.
6. The temperature of analog and MCU die is strongly linked via the package, but can differ in dynamic load conditions, usually because of higher power dissipation on the analog die. The analog die temperature must not exceed 150°C under these conditions
7. Terminal soldering temperature is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

STATIC ELECTRICAL CHARACTERISTICS

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 135°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE					
Nominal Operating Voltage	V_{SUP}	8.0	–	18	V
SUPPLY CURRENT					
NORMAL Mode V_{SUP} = 12 V, Power Die ON (PSON=1), MCU Operating Using Internal Oscillator at 32 MHz (8.0 MHz Bus Frequency), SPI, ESCI, ADC Enabled	I_{RUN}	–	20	–	mA
DIGITAL INTERFACE RATINGS (ANALOG DIE)					
Output Terminals $\overline{RST\_A}$, $\overline{IRQ\_A}$ Low-State Output Voltage (I_{OUT} = -1.5 mA) High-State Output Voltage (I_{OUT} = 1.0 µA)	 V_{OL} V_{OH}	 – 3.85	 – –	 0.4 –	V
Output Terminals BEMF, RXD Low-State Output Voltage (I_{OUT} = -1.5 mA) High-State Output Voltage (I_{OUT} = 1.5 mA)	 V_{OL} V_{OH}	 – 3.85	 – –	 0.4 –	V
Output Terminal RXD–Capacitance [8]	C_{IN}	–	4.0	–	pF
Input Terminals $\overline{RST\_A}$, FGEN, $\overline{SS}$ Input Logic Low Voltage Input Logic High Voltage	 V_{IL} V_{IH}	 – 3.5	 – –	 1.5 –	V
Input Terminals $\overline{RST\_A}$, FGEN, $\overline{SS}$–Capacitance [8]	C_{IN}	–	4.0	–	pF
Terminals $\overline{RST\_A}$, $\overline{IRQ\_A}$–Pullup Resistor	$R_{PULLUP1}$	–	10	–	kΩ
Terminal $\overline{SS}$–Pullup Resistor	$R_{PULLUP2}$	–	60	–	kΩ
Terminals FGEN, MOSI, SPSCK–Pulldown Resistor	$R_{PULLDOWN}$	–	60	–	kΩ
Terminal TXD–Pullup Current Source	I_{PULLUP}	–	35	–	µA

Notes

8. This parameter is guaranteed by process monitoring but is not production tested.

STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 135°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SYSTEM RESETS AND INTERRUPTS					
High-Voltage Reset					V
Threshold	V_{HVRON}	27	30	33	
Hysteresis	V_{HVRH}	–	1.5	–	
Low-Voltage Reset					
Threshold	V_{LVRON}	3.6	4.0	4.7	V
Hysteresis	V_{LVRH}	–	100	–	mV
High-Voltage Interrupt					V
Threshold	V_{HVION}	17.5	21	23	
Hysteresis	V_{HVIH}	–	1.0	–	
Low-Voltage Interrupt					V
Threshold	V_{LVION}	6.5	–	8.0	
Hysteresis	V_{LVIH}	–	0.4	–	
High-Temperature Reset (9)					°C
Threshold	T_{RON}	–	170	–	
Hysteresis	T_{RH}	5.0	–	–	
High-Temperature Interrupt (10)					°C
Threshold	T_{ION}	–	160	–	
Hysteresis	T_{IH}	5.0	–	–	
VOLTAGE REGULATOR					
Normal Mode Output Voltage	V_{DDRUN}				V
I_{OUT} = 60 mA, 6.0 V < V_{SUP} < 18 V		4.75	5.0	5.25	
Load Regulation	V_{LR}				mV
I_{OUT} = 80 mA, V_{SUP} = 9.0 V		–	–	100	

Notes

9. This parameter is guaranteed by process monitoring but is not production tested.
10. High-Temperature Interrupt (HTI) threshold is linked to High-Temperature Reset (HTR) threshold (HTR = HTI + 10°C).

STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 135°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Output Low Level TXD LOW, 500 Ω Pullup to V_{SUP}	$V_{LIN-LOW}$	–	–	1.4	V
Output High Level TXD HIGH, I_{OUT} = 1.0 µA	$V_{LIN-HIGH}$	V_{SUP}-1.0	–	–	V
Pullup Resistor to V_{SUP}	R_{SLAVE}	20	30	60	kΩ
Leakage Current to GND Recessive State (-0.5 V < V_{LIN} < V_{SUP})	$I_{BUS\_PAS\_REC}$	0.0	–	20	µA
Leakage Current to GND (V_{SUP} Disconnected) Including Internal Pullup Resistor, V_{LIN} @ -18 V Including Internal Pullup Resistor, V_{LIN} @ +18 V	 $I_{BUS\_NO\_GND}$ I_{BUS}	 – –	 -600 25	 – –	µA
LIN Receiver Recessive Dominant Threshold Input Hysteresis	 V_{IH} V_{IL} V_{ITH} V_{IHY}	 0.6 V_{LIN} 0 – 0.01 V_{SUP}	 – – V_{SUP}/2 –	 V_{SUP} 0.4 V_{LIN} – 0.1 V_{SUP}	V

STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 135°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HALF-BRIDGE OUTPUTS (HB1:HB4)					
Switch ON Resistance @ T_J = 25°C with I_{LOAD} = 1.0 A					mΩ
High Side	$R_{DS(ON)HB\_HS}$	–	425	500	
Low Side	$R_{DS(ON)HB\_LS}$	–	400	500	
High-Side Overcurrent Shutdown	I_{HBHSOC}	3.0	–	7.5	A
Low-Side Overcurrent Shutdown	I_{HBLSOC}	2.5	–	7.5	A
Low-Side Current Limitation @ T_J = 25°C					mA
Current Limit 1 (CLS2 = 0, CLS1 = 1, CLS0 = 1)	I_{CL1}	–	55	–	
Current Limit 2 (CLS2 = 1, CLS1 = 0, CLS0 = 0)	I_{CL2}	210	260	315	
Current Limit 3 (CLS2 = 1, CLS1 = 0, CLS0 = 1)	I_{CL3}	300	370	440	
Current Limit 4 (CLS2 = 1, CLS1 = 1, CLS0 = 0)	I_{CL4}	450	550	650	
Current Limit 5 (CLS2 = 1, CLS1 = 1, CLS0 = 1)	I_{CL5}	600	740	880	
Half-Bridge Output HIGH Threshold for BEMF Detection	V_{BEMFH}	–	-30	0.0	V
Half-Bridge Output LOW Threshold for BEMF Detection	V_{BEMFL}	–	-60	-5.0	mV
Hysteresis for BEMF Detection	V_{BEMFHY}	–	30	–	mV
Low-Side Current-to-Voltage Ratio (V_{ADOUT} [V]/I_{HB} [A])					V/A
CSA = 1	$RATIO_H$	7.0	12.0	14.0	
CSA = 0	$RATIO_L$	1.0	2.0	3.0	
SWITCHABLE V_{DD} OUTPUT (HVDD)					
Overcurrent Shutdown Threshold	$I_{HVDDOCT}$	24	30	40	mA
V_{SUP} DOWN-SCALER					
Voltage Ratio ($RATIO_{VSUP}$ = V_{SUP} /V_{ADOUT})	$RATIO_{VSUP}$	4.8	5.1	5.35	–
INTERNAL DIE TEMPERATURE SENSOR					
Voltage/Temperature Slope	S_{TTOV}	–	19	–	mV/°C
Output Voltage @ 25°C	V_{T25}	1.7	2.1	2.5	V

DYNAMIC ELECTRICAL CHARACTERISTICS

DYNAMIC ELECTRICAL CHARACTERISTICS

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 135°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Propagation Delay (11), (12)					µs
TXD LOW to LIN LOW	$t_{TXD-LIN-LOW}$	–	–	6.0	
TXD HIGH to LIN HIGH	$t_{TXD-LIN-HIGH}$	–	–	6.0	
LIN LOW to RXD LOW	$t_{LIN-RXD-LOW}$	–	4.0	8.0	
LIN HIGH to RXD HIGH	$t_{LIN-RXD-HIGH}$	–	4.0	8.0	
TXD Symmetry	$t_{TXD-SYM}$	-2.0	–	2.0	
RXD Symmetry	$t_{RXD-SYM}$	-2.0	–	2.0	
Output Falling Edge Slew Rate (11), (13)	SR_F				V/µs
80% to 20%		-1.0	-2.0	-3.0	
Output Rising Edge Slew Rate (11), (13)	SR_R				V/µs
20% to 80%, R_{BUS} > 1.0 kΩ, C_{BUS} < 10 nF		1.0	2.0	3.0	
LIN Rise/Fall Slew Rate Symmetry (11), (13)	SR_S	-2.0	–	2.0	µs
AUTONOMOUS WATCHDOG (AWD)					
AWD Oscillator Period	t_{OSC}	–	40	–	µs
AWD Period Low = 512 t_{OSC}	t_{AWDPH}	16	22	28	ms
AWD Period High = 256 t_{OSC}	t_{AWDPL}	8.0	11	14	ms

Notes

11. All LIN characteristics are for initial LIN slew rate selection (20 kbaud) (SRS0:SRS1= 00).
12. See Figure 4, page 12.
13. See Figure 5, page 12.

MICROCONTROLLER PARAMETRICS

MICROCONTROLLER

For a detailed microcontroller description, refer to the MC68HC908EY16 datasheet.

Module	Description
Core	High-Performance HC08 Core with a Maximum Internal Bus Frequency of 8.0 MHz
Timer	Two 16-Bit Timers with Two Channels (TIM A and TIM B)
Flash	16 K Bytes
RAM	512 Bytes
ADC	10-Bit Analog-to-Digital Converter
SPI	SPI Module
ESCI	Standard Serial Communication Interface (SCI) Module Bit-Time Measurement Arbitration Prescaler with Fine Baud-Rate Adjustment
ICG	Internal Clock Generation Module
BEMF Counter	Special Counter for *SMARTMOS* BEMF Output

TIMING DIAGRAMS

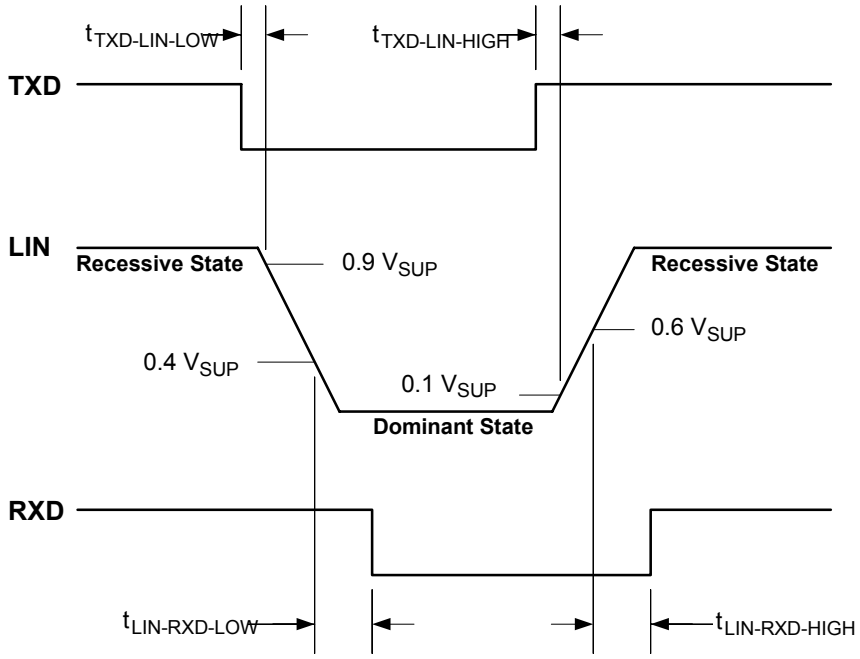
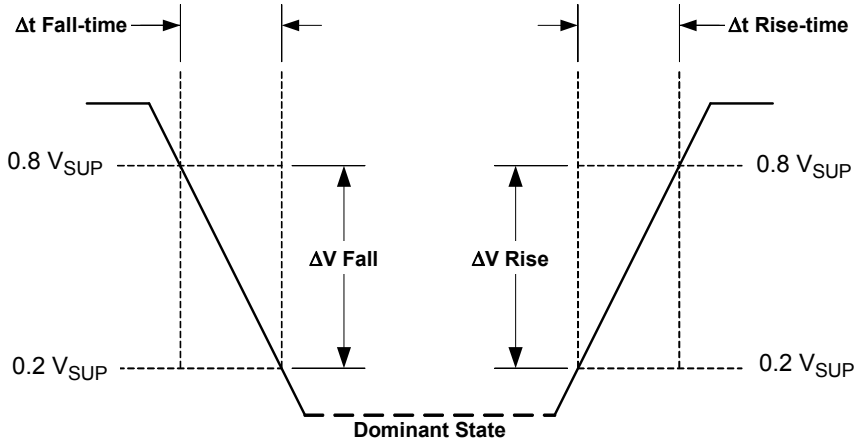


Figure 4. LIN Timing Description



$$SR_F = \frac{\Delta V\ Fall}{\Delta t\ Fall\text{-}time} \qquad SR_R = \frac{\Delta V\ Rise}{\Delta t\ Rise\text{-}time}$$

Figure 5. LIN Slew Rate Description

Functional Diagrams

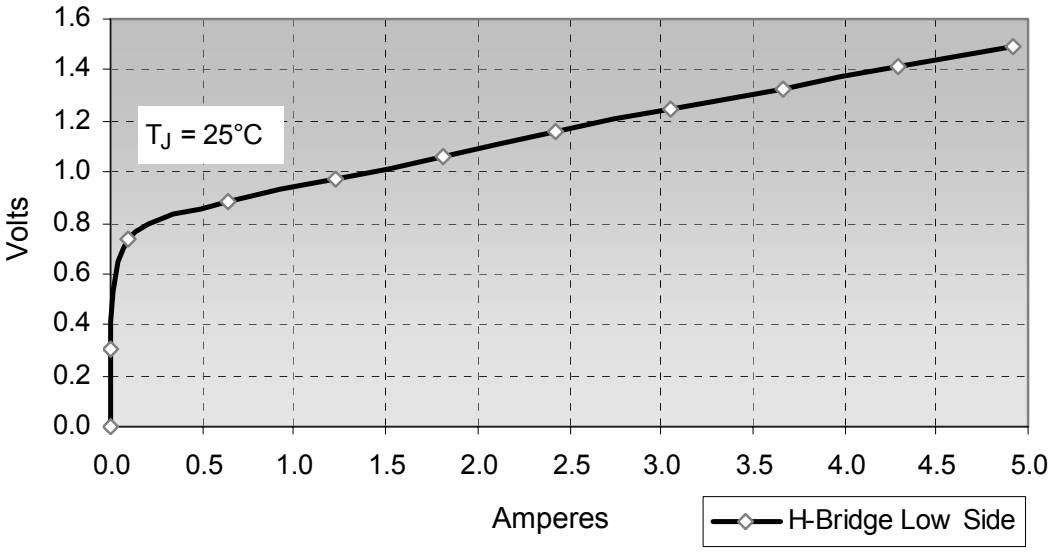


Figure 6. Free Wheel Diode Forward Voltage

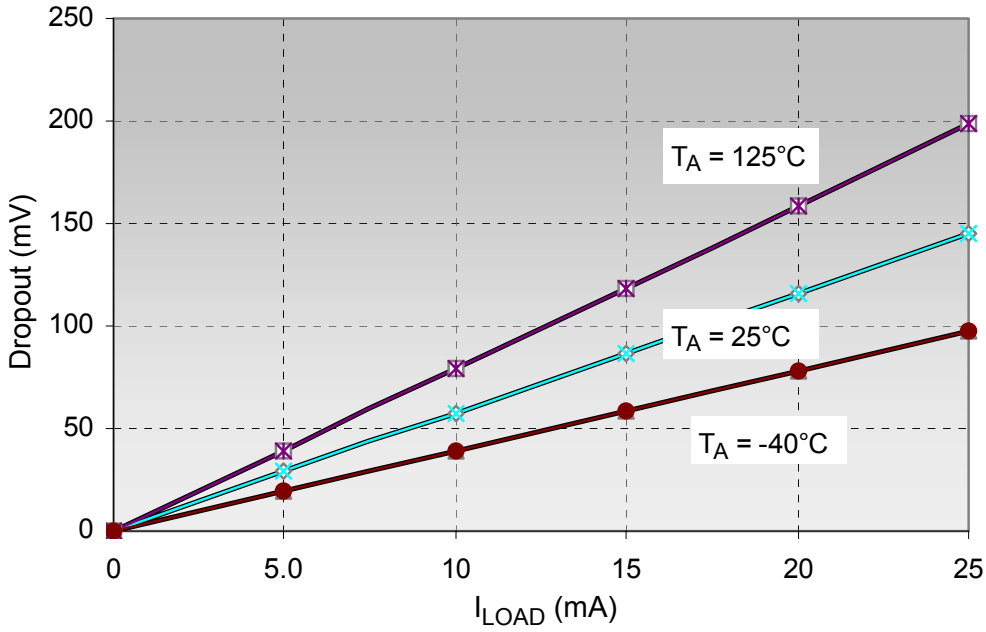


Figure 7. Dropout Voltage on HVDD

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 908E626 device was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 908E626 is well suited to perform stepper motor control, e.g. for climate or light-levelling control via a 3-wire LIN bus.

This device combines an standard HC08 MCU core (68HC908EY16) with flash memory together with a *SMARTMOS* IC chip. The *SMARTMOS* IC chip combines power and control in one chip. Power switches are provided on the *SMARTMOS* IC configured as four half-bridge outputs. Other ports are also provided including a selectable HVDD terminal. An internal voltage regulator is provided on the *SMARTMOS* IC chip, which provides power to the MCU chip.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables the device to be compatible with 3-wire bus systems, where one wire is used for communication, one for battery, and the third for ground.

FUNCTIONAL TERMINAL DESCRIPTION

See Figures 1, for a graphic representation of the various terminals referred to in the following paragraphs. Also, see the terminal diagram on Figures 3 for a depiction of the terminal locations on the package.

PORT A I/O TERMINALS (PTA0:4)

These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU. PTA0:PTA4 are shared with the keyboard interrupt terminals, KBD0:KBD4.

The PTA5/SPSCK terminal is not accessible in this device and is internally connected to the SPI clock terminal of the analog die. The PTA6/$\overline{SS}$ terminal is likewise not accessible.

For details refer to the 68HC908EY16 datasheet.

PORT B I/O TERMINALS (PTB1, PTB3:7)

These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU. All terminals are shared with the ADC module. The PTB6:PTB7 terminals are also shared with the Timer B module.

PTB0/AD0 is internally connected to the ADOUT terminal of the analog die, allowing diagnostic measurements to be calculated; e.g., current recopy, V_{SUP}, etc. The PTB2/AD2 terminal is not accessible in this device.

For details refer to the 68HC908EY16 datasheet.

PORT C I/O TERMINALS (PTC2:4)

These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU. For example, PTC2:PTC4 are shared with the ICG module.

PTC0/MISO and PTC1/MOSI are not accessible in this device and are internally connected to the MISO and MOSI SPI terminals of the analog die.

For details refer to the 68HC908EY16 datasheet.

PORT D I/O TERMINALS (PTD0:1)

PTD1/TACH1 and PTD0/TACH0/BEMF are special-function, bidirectional I/O port terminals that can also be programmed to be timer terminals.

In step motor applications the PTD0 terminal should be connected to the BEMF output of the analog die in order to evaluate the BEMF signal with a special BEMF module of the MCU.

PTD1 terminal is recommended for use as an output terminal for generating the FGEN signal (PWM signal) if required by the application.

PORT E I/O TERMINAL (PTE1)

PTE1/RXD and PTE0/TXD are special-function, bidirectional I/O port terminals that can also be programmed to be enhanced serial communication.

PTE0/TXD is internally connected to the TXD terminal of the analog die. The connection for the receiver must be done externally.

EXTERNAL INTERRUPT TERMINAL ($\overline{IRQ}$)

The $\overline{IRQ}$ terminal is an asynchronous external interrupt terminal. This terminal contains an internal pullup resistor that is always activated, even when the $\overline{IRQ}$ terminal is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

EXTERNAL RESET TERMINAL ($\overline{RST}$)

A logic [0] on the $\overline{RST}$ terminal forces the MCU to a known startup state. $\overline{RST}$ is bidirectional, allowing a reset of the entire system. It is driven LOW when any internal reset source is asserted.

This terminal contains an internal pullup resistor that is always activated, even when the reset terminal is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

CURRENT LIMITATION FREQUENCY INPUT TERMINAL (FGEN)

Input terminal for the half-bridge current limitation PWM frequency. This input is not a real PWM input terminal; it should just supply the period of the PWM. The duty cycle will be generated automatically.

Important The recommended FGEN frequency should be in the range of 0.1 kHz to 20 kHz.

BACK ELECTROMAGNETIC FORCE OUTPUT TERMINAL (BEMF)

This terminal gives the user information about back electromagnetic force (BEMF). This feature allows stall detection and coil failures in step motor applications. In order to evaluate this signal the terminal must be directly connected to terminal PTD0/TACH0/BEMF.

RESET TERMINAL ($\overline{\text{RST\_A}}$)

$\overline{\text{RST\_A}}$ is the bidirectional reset terminal of the analog die. It is an open drain with pullup resistor and must be connected to the $\overline{\text{RST}}$ terminal of the MCU.

INTERRUPT TERMINAL ($\overline{\text{IRQ\_A}}$)

$\overline{\text{IRQ\_A}}$ is the interrupt output terminal of the analog die indicating errors or wake-up events. It is an open drain with pullup resistor and must be connected to the $\overline{\text{IRQ}}$ terminal of the MCU.

SLAVE SELECT TERMINAL ($\overline{\text{SS}}$)

This terminal is the SPI Slave Select terminal for the analog chip. All other SPI connections are done internally. $\overline{\text{SS}}$ must be connected to PTB1 or any other logic I/O of the microcontroller.

LIN BUS TERMINAL (LIN)

The LIN terminal represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

HALF-BRIDGE OUTPUT TERMINALS (HB1:HB4)

The 908E626 device includes power MOSFETs configured as four half-bridge driver outputs. The HB1:HB4 outputs may be configured for step motor drivers, DC motor drivers, or as high-side and low-side switches.

The HB1:HB4 outputs are short-circuit and overtemperature protected, and they feature current recopy, current limitation, and BEMF generation. Current limitation and recopy are done on the low-side MOSFETs.

POWER SUPPLY TERMINALS (VSUP1:VSUP3)

VSUP1:VSUP3 are device power supply terminals. The nominal input voltage is designed for operation from 12 V systems. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs, multiple VSUP terminals are provided.

All VSUP terminals must be connected to get full chip functionality.

POWER GROUND TERMINALS (GND1 AND GND2)

GND1 and GND2 are device power ground connections. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs multiple terminals are provided.

GND1 and GND2 terminals must be connected to get full chip functionality.

SWITCHABLE V_{DD} OUTPUT TERMINAL (HVDD)

The HVDD terminal is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply; The output is short-circuit protected.

+5.0 V VOLTAGE REGULATOR OUTPUT TERMINAL (VDD)

The VDD terminal is needed to place an external capacitor to stabilize the regulated output voltage. The VDD terminal is intended to supply the embedded microcontroller.

Important The VDD terminal should not be used to supply other loads; use the HVDD terminal for this purpose. The VDD, EVDD, VDDA, and VREFH terminals must be connected together.

VOLTAGE REGULATOR GROUND TERMINAL (VSS)

The VSS terminal is the ground terminal for the connection of all non-power ground connections (microcontroller and sensors).

Important VSS, EVSS, VSSA, and VREFL terminals must be connected together.

LIN TRANSCEIVER OUTPUT TERMINAL (RXD)

This terminal is the output of LIN transceiver. The terminal must be connected to the microcontroller's Enhanced Serial Communications Interface (ESCI) module (RXD terminal).

ADC REFERENCE TERMINALS (VREFL AND VREFH)

VREFL and VREFH are the reference voltage terminals for the ADC. It is recommended that a high-quality ceramic decoupling capacitor be placed between these terminals.

Important VREFH is the high reference supply for the ADC and should be tied to the same potential as VDDA via separate traces. VREFL is the low reference supply for the ADC and should be tied to the same potential as VSS via separate traces.

For details refer to the 68HC908EY16 datasheet.

ADC SUPPLY TERMINALS (VDDA AND VSSA)

VDDA and VSSA are the power supply terminals for the analog-to-digital converter (ADC). It is recommended that a high-quality ceramic decoupling capacitor be placed between these terminals.

Important VDDA is the supply for the ADC and should be tied to the same potential as EVDD via separate traces. VSSA is the ground terminal for the ADC and should be tied to the same potential as EVSS via separate traces.

For details refer to the 68HC908EY16 datasheet.

MCU POWER SUPPLY TERMINALS (EVDD AND EVSS)

EVDD and EVSS are the power supply and ground terminals. The MCU operates from a single power supply.

Fast signal transitions on MCU terminals place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details refer to the 68HC908EY16 datasheet.

TEST TERMINAL (FLSVPP)

This terminal is for test purposes only. This terminal should be either left open (not connected) or connected to GND.

EXPOSED PAD TERMINAL

The exposed pad terminal on the bottom side of the package conducts heat from the chip to the PCB board. For thermal performance the pad must be soldered to the PCB board. It is recommended that the pad be connected to the ground potential.

FUNCTIONAL DEVICE OPERATION

LOGIC COMMANDS AND REGISTERS

INTERRUPTS

The 908E626 has five different interrupt sources as described in the following paragraphs. The interrupts can be disabled or enabled via the SPI. After reset all interrupts are automatically disabled.

LOW-VOLTAGE INTERRUPT

The Low-Voltage Interrupt (LVI) is related to the external supply voltage, V_{SUP}. If this voltage falls below the LVI threshold, it will set the LVI flag. If the low-voltage interrupt is enabled, an interrupt will be initiated.

With LVI the H-Bridges (high-side MOSFET only) are switched off. All other modules are not influenced by this interrupt.

HIGH-VOLTAGE INTERRUPT

The High-Voltage Interrupt (HVI) is related to the external supply voltage, V_{SUP}. If this voltage rises above the HVI threshold, it will set the HVI flag. If the High-Voltage Interrupt is enabled, an interrupt will be initiated.

With HVI the H-Bridges (high-side MOSFET only) are switched off. All other modules are not influenced by this interrupt.

HIGH-TEMPERATURE INTERRUPT

The High-Temperature Interrupt (HTI) is generated by the on-chip temperature sensors. If the chip temperature is above the HTI threshold, the HTI flag will be set. If the High-Temperature Interrupt is enabled, an interrupt will be initiated.

LIN INTERRUPT

If the LINIE bit is set, a falling edge on the LIN terminal will generate an interrupt.

OVERCURRENT INTERRUPT

If an overcurrent condition on a half-bridge or the HVDD output is detected and the OCIE bit is set and an interrupt generated.

INTERRUPT FLAG REGISTER (IFR)

Register Name and Address: IFR - $05

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	LINF	HTF	LVF	HVF	OCF	0
Write								
Reset	0	0	0	0	0	0	0	0

LINF—LIN FLAG BIT

This read/write flag is set on the falling edge at the LIN data line. Clear LINF by writing a logic [1] to LINF. Reset clears the LINF bit. Writing a logic [0] to LINF has no effect.

- 1 = Falling edge on LIN data line has occurred.
- 0 = Falling edge on LIN data line has not occurred since last clear.

HTF—HIGH-TEMPERATURE FLAG BIT

This read/write flag is set on a high-temperature condition. Clear HTF by writing a logic [1] to HTF. If a high-temperature condition is still present while writing a logic [1] to HTF, the writing has no effect. Therefore, a high-temperature interrupt cannot be lost due to inadvertent clearing of HTF. Reset clears the HTF bit. Writing a logic [0] to HTF has no effect.

- 1 = High-temperature condition has occurred.
- 0 = High-temperature condition has not occurred.

LVF—LOW-VOLTAGE FLAG BIT

This read/write flag is set on a low-voltage condition. Clear LVF by writing a logic [1] to LVF. If a low-voltage condition is still present while writing a logic [1] to LVF, the writing has no effect. Therefore, a low-voltage interrupt cannot be lost due to inadvertent clearing of LVF. Reset clears the LVF bit. Writing a logic [0] to LVF has no effect.

- 1 = Low-voltage condition has occurred.
- 0 = Low-voltage condition has not occurred.

HVF—HIGH-VOLTAGE FLAG BIT

This read/write flag is set on a high-voltage condition. Clear HVF by writing a logic [1] to HVF. If high-voltage condition is still present while writing a logic [1] to HVF, the writing has no effect. Therefore, a high-voltage interrupt cannot be lost due to inadvertent clearing of HVF. Reset clears the HVF bit. Writing a logic [0] to HVF has no effect.

- 1 = High-voltage condition has occurred.
- 0 = High-voltage condition has not occurred.

OCF—OVERCURRENT FLAG BIT

This read-only flag is set on an overcurrent condition. Reset clears the OCF bit. To clear this flag, write a logic [1] to the appropriate overcurrent flag in the SYSSTAT Register. See Figure 8, which shows the two signals triggering the OCF.

- 1 = High-current condition has occurred.
- 0 = High-current condition has not occurred.

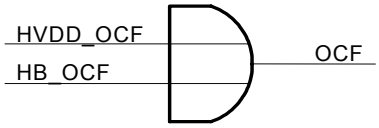


Figure 8. Principal Implementation for OCF

INTERRUPT MASK REGISTER (IMR)

Register Name and Address: IMR - $04

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	LINIE	HTIE	LVIE	HVIE	OCIE	0
Write								
Reset	0	0	0	0	0	0	0	0

LINIE—LIN LINE INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the LIN flag, LINF. Reset clears the LINIE bit.

- 1 = Interrupt requests from LINF flag enabled.
- 0 = Interrupt requests from LINF flag disabled.

HTIE—HIGH-TEMPERATURE INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the high-temperature flag, HTF. Reset clears the HTIE bit.

- 1 = Interrupt requests from HTF flag enabled.
- 0 = Interrupt requests from HTF flag disabled.

LVIE—LOW-VOLTAGE INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the low-voltage flag, LVF. Reset clears the LVIE bit.

- 1 = Interrupt requests from LVF flag enabled.
- 0 = Interrupt requests from LVF flag disabled.

HVIE—HIGH-VOLTAGE INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the high-voltage flag, HVF. Reset clears the HVIE bit.

- 1 = Interrupt requests from HVF flag enabled.
- 0 = Interrupt requests from HVF flag disabled.

OCIE—Overcurrent Interrupt Enable Bit

This read/write bit enables CPU interrupts by the overcurrent flag, OCF. Reset clears the OCIE bit.

- 1 = Interrupt requests from OCF flag enabled.
- 0 = Interrupt requests from OCF flag disabled.

RESET

The 908E626 chip has four internal reset sources and one external reset source, as explained in the paragraphs below. Figure 9 depicts the internal reset sources.

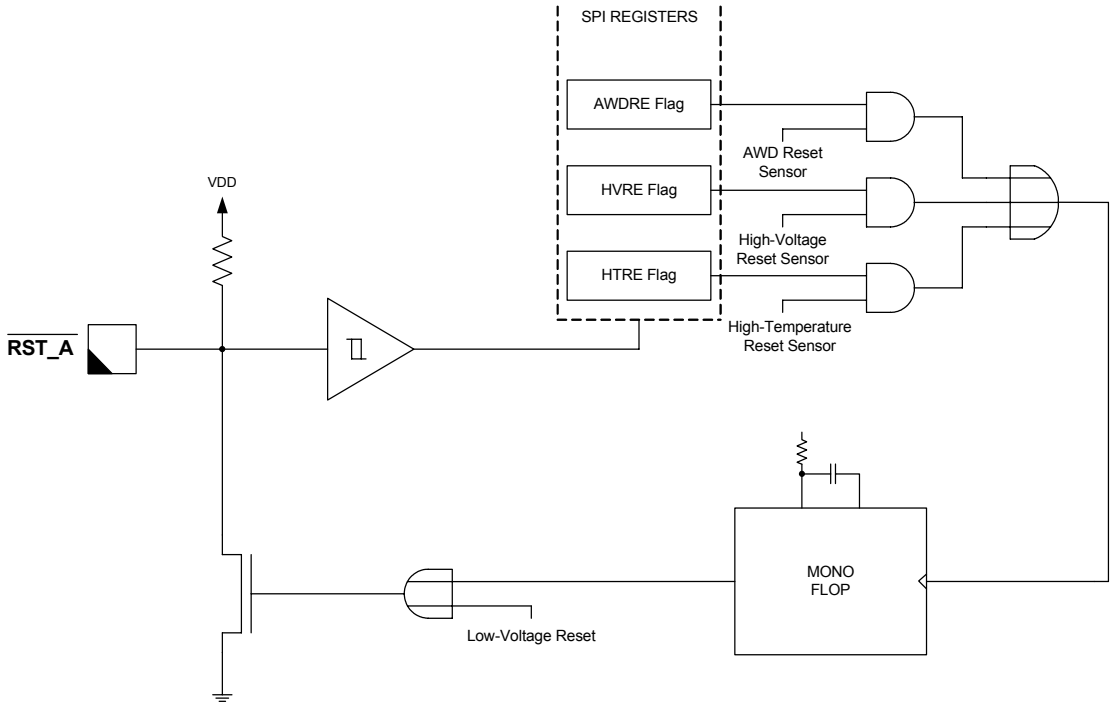


Figure 9. Internal Reset Routing

RESET INTERNAL SOURCES

Autonomous Watchdog

AWD modules generates a reset because of a timeout (watchdog function).

High-Temperature Reset

To prevent damage to the device, a reset will be initiated if the temperature rises above a certain value. The reset is maskable with bit HTRE in the Reset Mask Register. After a reset the high-temperature reset is disabled.

Low-Voltage Reset

The LVR is related to the internal V_{DD}. In case the voltage falls below a certain threshold, it will pull down the $\overline{\text{RST\_A}}$ terminal.

High-Voltage Reset

The HVR is related to the external V_{SUP} voltage. In case the voltage is above a certain threshold, it will pull down the $\overline{\text{RST\_A}}$ terminal. The reset is maskable with bit HVRE in the Reset Mask Register. After a reset the high-voltage reset is disabled.

RESET EXTERNAL SOURCE

External Reset Terminal

The microcontroller has the capability of resetting the *SMARTMOS* device by pulling down the $\overline{\text{RST}}$ terminal.

Reset Mask Register (RMR)

Register Name and Address: RMR - $06

	Bit7	6	5	4	3	2	1	Bit0
Read	TTEST	0	0	0	0	0	HVRE	HTRE
Write								
Reset	0	0	0	0	0	0	0	0

TTEST—High-Temperature Reset Test

This read/write bit is for test purposes only. It decreases the overtemperature shutdown limit for final test. Reset clears the HTRE bit.

- 1 = Low-temperature threshold enabled.
- 0 = Low-temperature threshold disabled.

HVRE—High-Voltage Reset Enable Bit

This read/write bit enables resets on high-voltage conditions. Reset clears the HVRE bit.

- 1 = High-voltage reset enabled.
- 0 = High-voltage reset disabled.

HTRE—High-Temperature Reset Enable Bit

This read/write bit enables resets on high-temperature conditions. Reset clears the HTRE bit.

- 1 = High-temperature reset enabled.
- 0 = High-temperature reset disabled.

SERIAL PERIPHERAL INTERFACE

The serial peripheral interface (SPI) creates the communication link between the microcontroller and the 908E626.

The interface consists of four terminals (see Figure 10):

- $\overline{\text{SS}}$—Slave Select
- MOSI—Master-Out Slave-In
- MISO—Master-In Slave-Out
- SPSCK—Serial Clock (maximum frequency 4.0 MHz)

A complete data transfer via the SPI consists of 2 bytes. The master sends address and data, slave system status, and data of the selected address.

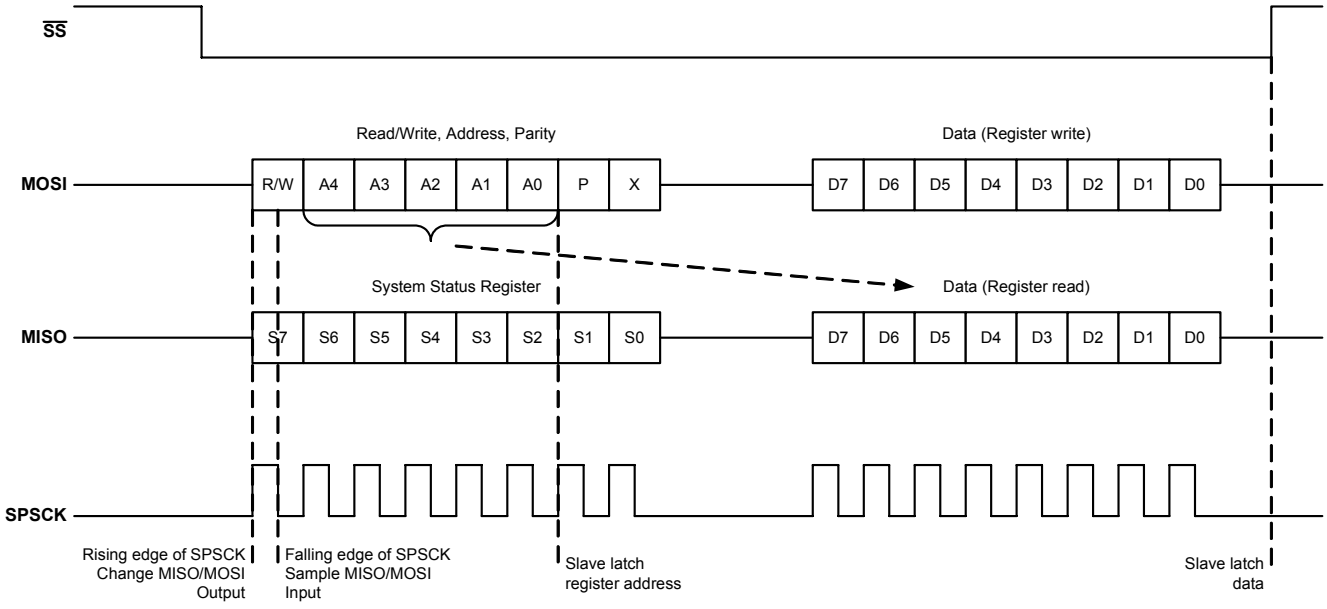


Figure 10. SPI Protocol

During the inactive phase of $\overline{SS}$, the new data transfer is prepared. The falling edge on the $\overline{SS}$ line indicates the start of a new data transfer and puts MISO in the low-impedance mode. The first valid data are moved to MISO with the rising edge of SPSCK.

The MISO output changes data on a rising edge of SPSCK. The MOSI input is sampled on a falling edge of SPSCK. The data transfer is only valid if exactly 16 sample clock edges are present in the active phase of $\overline{SS}$.

After a write operation, the transmitted data is latched into the register by the rising edge of $\overline{SS}$. Register read data is internally latched into the SPI at the time when the parity bit is transferred. $\overline{SS}$ HIGH forces MISO to high impedance.

MASTER ADDRESS BYTE

A4:A0

Contains the address of the desired register.

R/$\overline{W}$

Contains information about a read or a write operation.

- If R/$\overline{W}$ = 1, the second byte of master contains no valid information, slave just transmits back register data.
- If R/$\overline{W}$ = 0, the master sends data to be written in the second byte, slave sends concurrently contents of selected register prior to write operation, write data is latched in the *SMARTMOS* register on rising edge of $\overline{SS}$.

Parity P

The parity bit is equal to “0” if the number of 1 bits is an even number contained within R/$\overline{W}$, A4:A0. If the number of 1 bits is odd, P equals “1”. For example, if R/$\overline{W}$ = 1, A4:A0 = 00001, then P equals “0.”

The parity bit is only evaluated during a write operation.

Bit X

Not used.

Master Data Byte

Table 2. Contains data to be written or no valid data during a read operation.

Table 3. List of Registers

Addr	Register Name	R/W	Bit							
			7	6	5	4	3	2	1	0
$01	H-Bridge Output (HBOUT)	R	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
		W								
$02	H-Bridge Control (HBCTL)	R	OFC_EN	CSA	0	0	0	CLS2	CLS1	CLS0
		W								
$03	System Control (SYSCTL)	R	PSON	SRS1	SRS0	0	0	0	0	0
		W								
$04	Interrupt Mask (IMR)	R	0	0	LINIE	HTIE	LVIE	HVIE	OCIE	0
		W								
$05	Interrupt Flag (IFR)	R	0	0	LINF	HTF	LVF	HVF	OCF	0
		W								
$06	Reset Mask (RMR)	R	TTEST	0	0	0	0	0	HVRE	HTRE
		W								
$07	Analog Multiplexer Configuration (ADMUX)	R	0	0	0	0	SS3	SS2	SS1	SS0
		W								
$08	Reserved	R	0	0	0	0	0	0	0	0
		W								
$09	Reserved	R	0	0	0	0	0	0	0	0
		W								
$0a	AWD Control (AWDCTL)	R	0	0	0	AWDRE	0	0	AWDF	AWDR
		W			AWDRST					
$0b	Power Output (POUT)	R	0	0	0	0	0	0	HVDDON	0
		W								
$0c	System Status (SYSSTAT)	R	0	LINCL	HVDD_OCF	0	LVF	HVF	HB_OCF	HTF
		W								

Slave Status Byte

Contains the contents of the System Status Register ($0c) independent of whether it is a write or read operation or which register was selected.

Slave Data Byte

Contains the contents of selected register. During a write operation it includes the register content prior to a write operation.

SPI Register Overview

Table 3 summarizes the SPI Register addresses and the bit names of each register.

ANALOG DIE I/OS

LIN Physical Layer

The LIN bus terminal provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer specification.

The LIN driver is a low-side MOSFET with internal current limitation and thermal shutdown. An internal pullup resistor with a serial diode structure is integrated, so no external pullup components are required for the application in a slave node. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slew rate controls is guaranteed.

The LIN terminal offers high susceptibility immunity level from external disturbance, guaranteeing communication during external disturbance.

The LIN transmitter circuitry is enabled by setting the PSON bit in the System Control Register (SYSCTL). If the transmitter works in the current limitation region, the LINCL bit in the System Status Register (SYSSTAT) is set. Due to excessive power dissipation in the transmitter, software is advised to monitor this bit and turn the transmitter off immediately.

TXD Terminal

The TXD terminal is the MCU interface to control the state of the LIN transmitter (see Figure , page 2). When TXD is LOW, LIN output is low (dominant state). When TXD is HIGH, the LIN output MOSFET is turned off. The TXD terminal has an internal pullup current source in order to set the LIN bus in recessive state in the event, for instance, the microcontroller could not control it during system power-up or power-down.

RXD Terminal

The RXD transceiver terminal is the MCU interface, which reports the state of the LIN bus voltage. LIN HIGH (recessive state) is reported by a high level on RXD, LIN LOW (dominant state) by a low level on RXD.

Analog Multiplexer/ADOUT Terminal

The ADOUT terminal is the analog output interface to the ADC of the MCU (see Figure , page 2). An analog multiplexer is used to read six internal diagnostic analog voltages.

Current Recopy

The analog multiplexer is connected to the four low-side current sense circuits of the half-bridges. These sense circuits offer a voltage proportional to the current through the low-side MOSFET. High or low resolution is selectable: 5.0 V/2.5 A or 5.0 V/500 mA, respectively. (Refer to Half-Bridge Current Recopy on page 25.)

Temperature Sensor

The 908E626 includes an on-chip temperature sensor. This sensor offers a voltage that is proportional to the actual chip junction temperature.

V_{SUP} Prescaler

The V_{SUP} prescaler permits the reading or measurement of the external supply voltage. The output of this voltage is $V_{SUP}/RATIO_{VSUP}$.

The different internal diagnostic analog voltages can be selected with the ADMUX Register.

Analog Multiplexer Configuration Register (ADMUX)

Register Name and Address: ADMUX - $07

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0	0	SS3	SS2	SS1	SS0
Write								
Reset	0	0	0	0	0	0	0	0

SS3, SS2, SS1, and SS0—A/D Input Select Bits

These read/write bits select the input to the ADC in the microcontroller according to Table 4, page 22. Reset clears SS3, SS2, SS1, and SS0 bits.

Table 4. Analog Multiplexer Configuration Register

SS3	SS2	SS1	SS0	Channel
0	0	0	0	Current Recopy HB1
0	0	0	1	Current Recopy HB2
0	0	1	0	Current Recopy HB3
0	0	1	1	Current Recopy HB4
0	1	0	0	V_{SUP} Prescaler
0	1	0	1	Temperature Sensor
0	1	1	0	Not Used
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Power Output Register (POUT)

Register Name and Address: P_{OUT} - $0b

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0 (14)	0 (14)	0 (14)	0 (14)	HVDDON	0 (14)
Write								
Reset	0	0	0	0	0	0	0	0

Notes
14. This bit must always be set to 0.

HVDDON—HVDD On Bit

This read/write bit enables HVDD output. Reset clears the HVDDON bit.

- 1 = HVDD enabled.
- 0 = HVDD disabled.

HALF-BRIDGES

Outputs HB1:HB4 provide four low-resistive half-bridge output stages. The half-bridges can be used in H-Bridge, high-side, or low-side configurations.

Reset clears all bits in the H-Bridge Output Register (HBOUT) owing to the fact that all half-bridge outputs are switched off.

HB1:HB4 output features:

- Short circuit (overcurrent) protection on high-side and low-side MOSFETs.
- Current recopy feature (low side MOSFET).

- Overtemperature protection.
- Overvoltage and undervoltage protection.
- Current limitation feature (low side MOSFET).

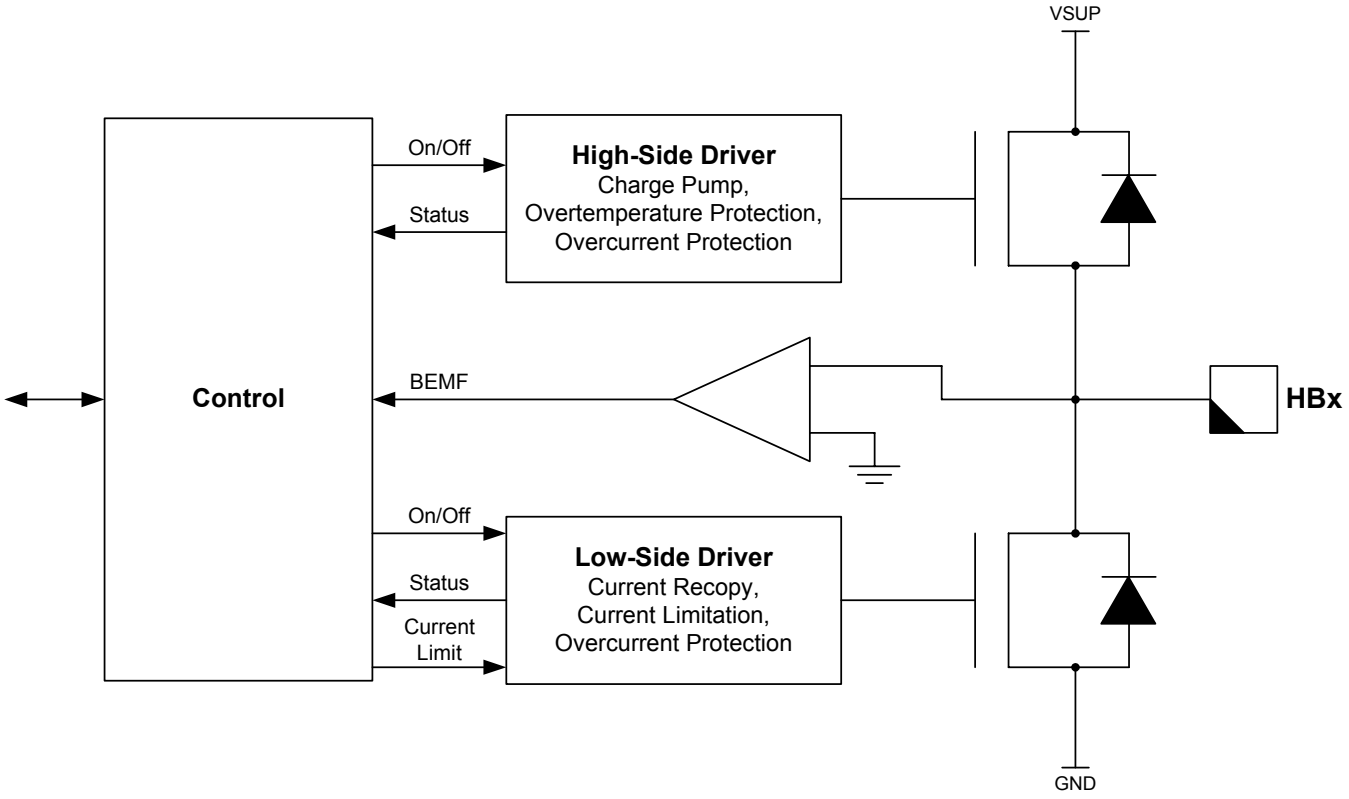


Figure 11. Half-Bridge Push-Pull Output Driver

Half-Bridge Control

Each output MOSFET can be controlled individually. The general enable of the circuitry is done by setting PSON in the System Control Register (SYSCTL). HBx_L and HBx_H form one half-bridge. It is not possible to switch on both MOSFETs in one half-bridge at the same time. If both bits are set, the high-side MOSFET has a higher priority.

To avoid both MOSFETs (high side and low side) of one half-bridge being on at the same time, a break-before-make circuit exists. Switching the high-side MOSFET on is inhibited as long as the potential between gate and V_{SS} is not below a certain threshold. Switching the low-side MOSFET on is blocked as long as the potential between gate and source of the high-side MOSFET did not fall below a certain threshold.

Half-Bridge Output Register (HBOUT)

Register Name and Address: HBOUT - $01

	Bit7	6	5	4	3	2	1	Bit0
Read Write	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
Reset	0	0	0	0	0	0	0	0

HBx_L—Low-Side On/Off Bits

These read/write bits turn on the low-side MOSFETs. Reset clears the HBx_L bits.

- 1 = Low-side MOSFET turned on for half-bridge output x.
- 0 = Low-side MOSFET turned off for half-bridge output x.

HBx_H—High-Side On/Off Bits

These read/write bits turn on the high-side MOSFETs. Reset clears the HBx_H bits.

- 1 = High-side MOSFET turned on for half-bridge output x.

- 0 = High-side MOSFET turned on for half-bridge output x.

HALF-BRIDGE CURRENT LIMITATION

Each low-side MOSFET offers a current limit or constant current feature. This features is realized by a pulse width modulation on the low-side MOSFET. The pulse width modulation on the outputs is controlled by the FGEN input and the load characteristics. The FGEN input provides the PWM frequency, whereas the duty cycle is controlled by the load characteristics.

The recommended frequency range for the FGEN and the PWM is 0.1 kHz to 20 kHz.

Functionality

Each low-side MOSFET switches off if a current above the selected current limit was detected. The 908E626 offers five different current limits (refer to Table 5, page 27, for current limit values). The low-side MOSFET switches on again if a rising edge on the FGEN input was detected (Figure 12).

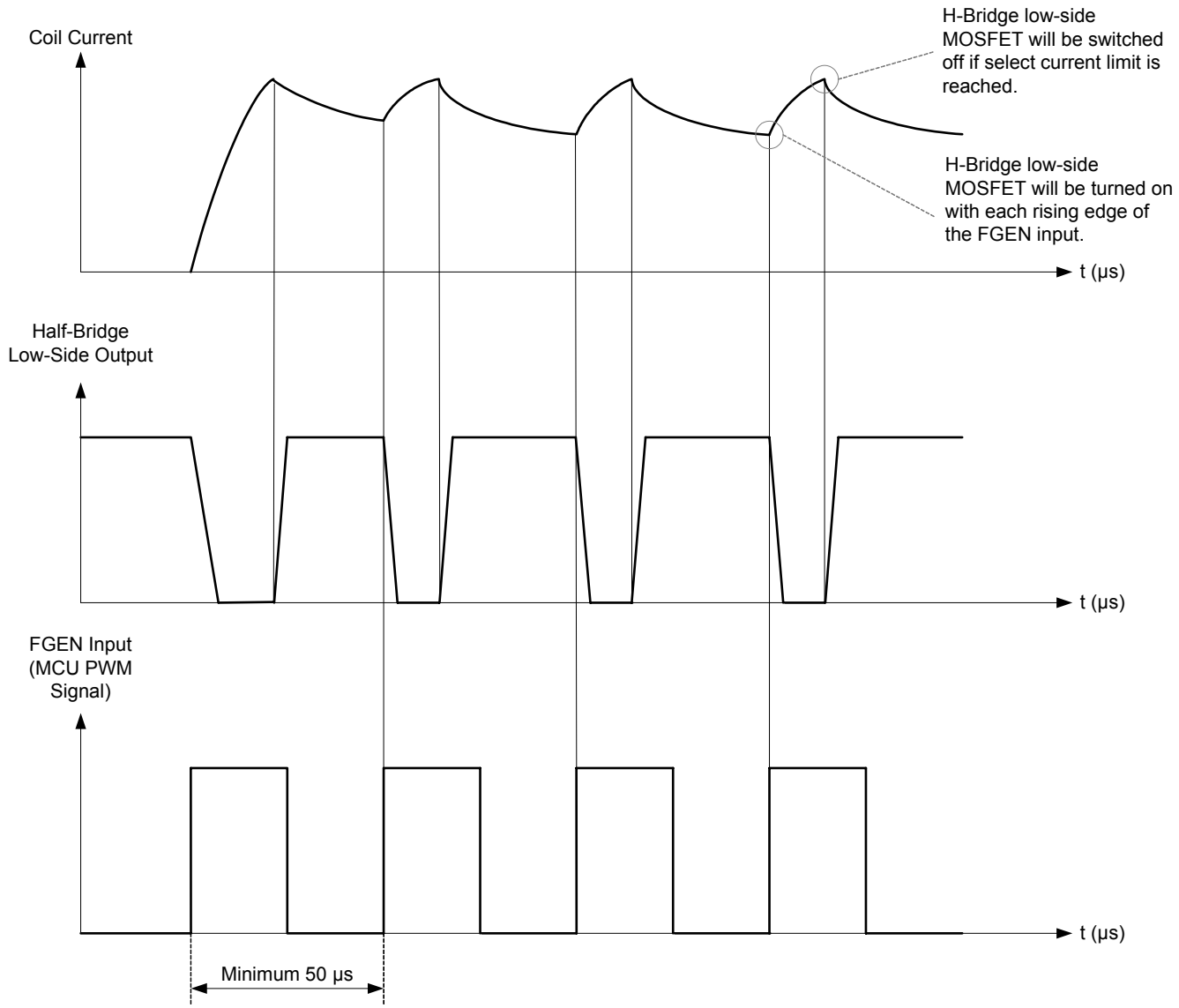


Figure 12. Half-Bridge Current Limitation

Offset Chopping

If bit OFC_EN in the H-Bridge Control Register (HBCTL) is set, HB1 and HB2 will continue to switch on the low-side MOSFETs with the rising edge of the FGEN signal and HB3 and HB4 will switch on the low-side MOSFETs with the falling edge on the FGEN input. In step motor applications, this

feature allows the reduction of EMI due to a reduction of the di/dt (Figure).

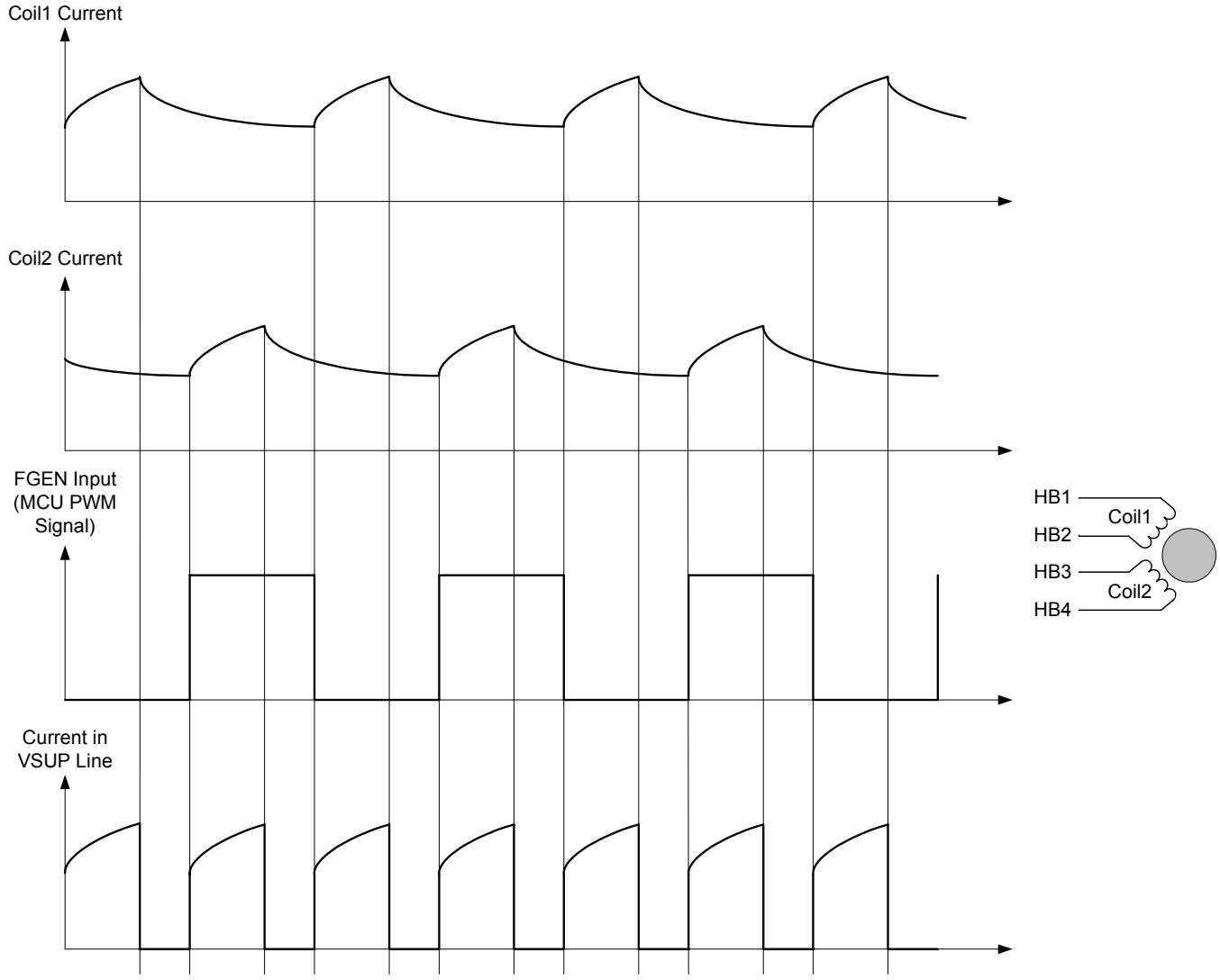


Figure 13. Offset Chopping for Step Motor Control

HALF-BRIDGE CURRENT RECOPY

Each low-side MOSFET has an additional sense output to allow a current recopy feature. This sense source is internally connected to a shunt resistor. The drop voltage is amplified and switched to the analog multiplexer.

The factor for the current sense amplification can be selected via bit CSA in the System Control Register.

- CSA = 1: Low resolution selected (500 mA measurement range).
- CSA = 0: High resolution selected (2.5 A measurement range).

HALF-BRIDGE BEMF GENERATION

The BEMF output is set to “1” if a recirculation current is detected in any half-bridge. This recirculation current flows via the two freewheeling diodes of the power MOSFETs. The BEMF circuitry detects that and generates a HIGH on the BEMF output as long as a recirculation current is detected. This signal provides a flexible and reliable detection of stall in step motor applications. For this the BEMF circuitry takes advantage of the instability of the electrical and mechanical behavior of a step motor when blocked. In addition the signal can be used for open load detection (absence of this signal) (see Figure 14, page 26).

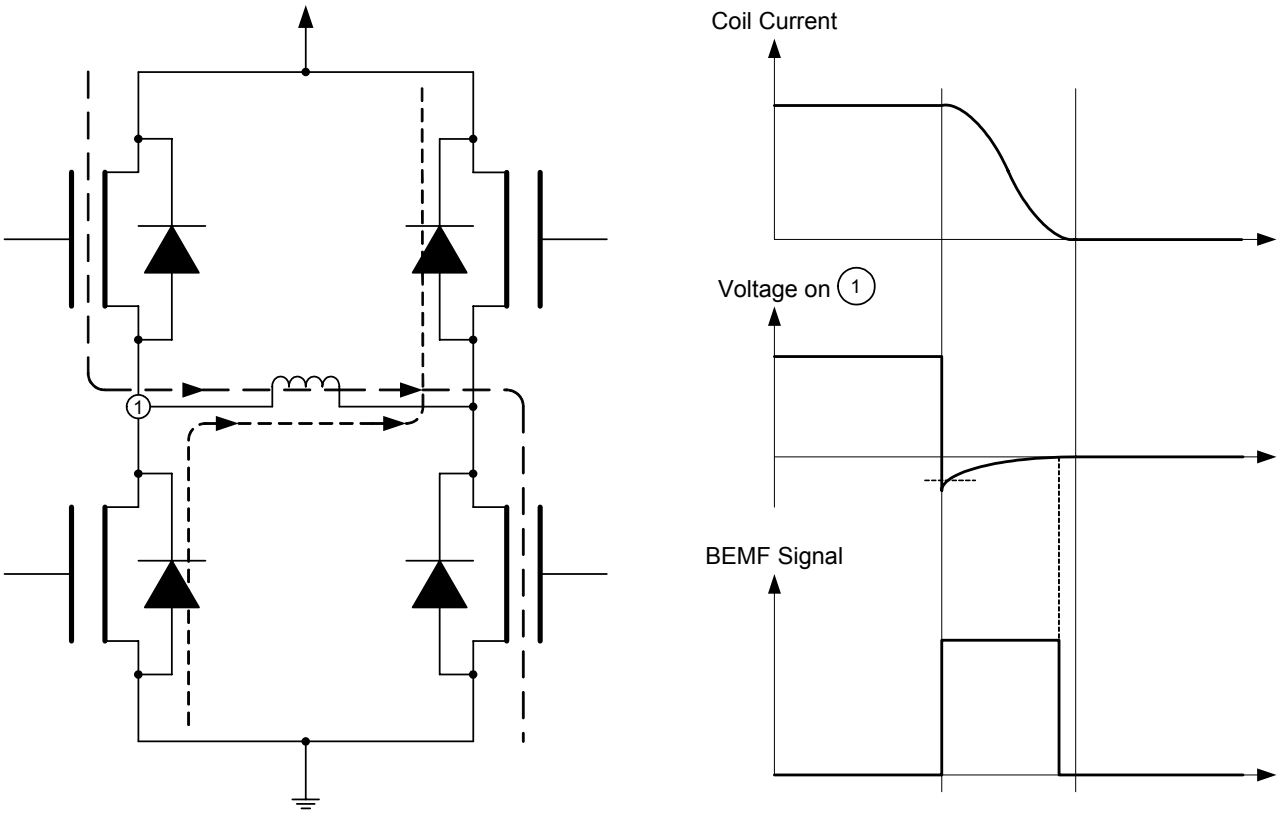


Figure 14. BEMF Signal Generation

HALF-BRIDGE OVERTEMPERATURE PROTECTION

The half-bridge outputs provide an overtemperature pre-warning with the HTF in the Interrupt Flag Register (IFR). In order to protect the outputs against overtemperature, the High-Temperature Reset must be enabled. If this value is reached, the part generates a reset and disables all power outputs.

HALF-BRIDGE OVERCURRENT PROTECTION

The half-bridges are protected against short to GND, short to VSUP, and load shorts.

In the event an overcurrent on the high side is detected, the high-side MOSFETs on all HB high-side MOSFETs are switched off automatically. In the event an overcurrent on the low side is detected, all HB low-side MOSFETs are switched off automatically. In both cases, the overcurrent status flag HB_OCF in the System Status Register (SYSSTAT) is set.

The overcurrent status flag is cleared (and the outputs re-enabled) by writing a logic [1] to the HB_OCF flag in the System Status Register or by reset.

HALF-BRIDGE OVERVOLTAGE/UNDERVOLTAGE

The half-bridge outputs are protected against undervoltage and overvoltage conditions. This protection is done by the low- and high-voltage interrupt circuitry. If one of these flags (LVF, HVF) is set, the outputs are automatically disabled.

The overvoltage/undervoltage status flags are cleared (and the outputs re-enabled) by writing a logic [1] to the LVF/HVF flags in the Interrupt Flag Register or by reset. Clearing this flag is useless as long as a high- or low-voltage condition is present.

Half-Bridge Control Register (HBCTL)

Register Name and Address: HBCTL - $02

	Bit7	6	5	4	3	2	1	Bit0
Read	OFC_EN	CSA	0	0	0	CLS2	CLS1	CLS0
Write								
Reset	0	0	0	0	0	0	0	0

OFC_EN—H-Bridge Offset Chopping Enable Bit

This read/write bit enables offset chopping. Reset clears the OFC_EN bit.

- 1 = Offset chopping enabled.
- 0 = Offset chopping disabled.

CSA—H-Bridges Current Sense Amplification Select Bit

This read/write bit selects the current sense amplification of the H-Bridges. Reset clears the CSA bit.

- 1 = Current sense amplification set for measuring 0.5 A.
- 0 = Current sense amplification set for measuring 2.5 A.

CLS2:CLS0—H-Bridge Current Limitation Selection Bits

These read/write bits select the current limitation value according to Table 5. Reset clears the CLS2:CLS0 bits.

Table 5. H-Bridge Current Limitation Value Selection

CLS2	CLS1	CLS0	Current Limit
0	0	0	No Limit
0	0	1	
0	1	0	
0	1	1	55 mA (typ)
1	0	0	260 mA (typ)
1	0	1	370 mA (typ)
1	1	0	550 mA (typ)
1	1	1	740 mA (typ)

Bits

Switchable VDD Outputs

The HVDD terminal is a switchable VDD output terminal. It can be used for driving external circuitry that requires a V_{DD} voltage. The output is enabled with bit PSON in the System Control Register and can be switched on/off with bit HVDDON in the Power Output Register. Low- or high-voltage conditions (LVI/HVI) have no influence on this circuitry.

HVDD Overtemperature Protection

Overtemperature protection is enabled if the high-temperature reset is enabled.

HVDD Overcurrent Protection

The HVDD output is protected against overcurrent. In the event the overcurrent limit is or was reached, the output automatically switches off and the HVDD overcurrent flag in the System Status Register is set.

System Control Register (SYSCTL)

Register Name and Address: SYSCTL - $03

	Bit7	6	5	4	3	2	1	Bit0
Read	PSON	SRS1	SRS0	0	0	0	0	0 (14)
Write								
Reset	0	0	0	0	0	0	0	0

Notes
15. This bit must always be set to 0.

PSON—Power Stages On Bit

This read/write bit enables the power stages (half-bridges, LIN transmitter and HVDD output). Reset clears the PSON bit.

- 1 = Power stages enabled.
- 0 = Power stages disabled.

SRS0:SRS1—LIN Slew Rate Selection Bits

These read/write bits enable the user to select the appropriate LIN slew rate for different baud rate configurations as shown in Table 6.

The high speed slew rates are used, for example, for programming via the LIN and are not intended for use in the application.

Table 6. LIN Slew Rate Selection Bits

SRS1	SRS0	LIN Slew Rate
0	0	Initial Slew Rate (20 kBaud)
0	1	Slow Slew Rate (10 kBaud)
1	0	High Speed II (8x)
1	1	High Speed I (4x)

System Status Register (SYSSTAT)

Register Name and Address: SYSSTAT - $0c

	Bit7	6	5	4	3	2	1	Bit0
Read	0	LINCL	HVDD_OCF	0	LVF	HVF	$\overline{HB\_OCF}$	HTF
Write								
Reset	0	0	0	0	0	0	0	0

LINCL — LIN Current Limitation Bit

This read-only bit is set if the LIN transmitter operates in current limitation region. Due to excessive power dissipation in the transmitter, software is advised to turn the transmitter off immediately.

- 1 = Transmitter operating in current limitation region.
- 0 = Transmitter not operating in current limitation region.

HVDD_OCF—HVDD Output Overcurrent Flag Bit

This read/write flag is set on an overcurrent condition at the HVDD terminal. Clear HVDD_OCF and enable the output by writing a logic [1] to the HVDD_OCF Flag. Reset clears the HVDD_OCF bit. Writing a logic [0] to HVDD_OCF has no effect.

- 1 = Overcurrent condition on HVDD has occurred.
- 0 = No overcurrent condition on HVDD has occurred.

LVF—Low-Voltage Bit

This read only bit is a copy of the LVF bit in the Interrupt Flag Register.

- 1 = Low-voltage condition has occurred.
- 0 = No low-voltage condition has occurred.

HVF—High-Voltage Sensor Bit

This read-only bit is a copy of the HVF bit in the Interrupt Flag Register.

- 1 = High-voltage condition has occurred.
- 0 = No high-voltage condition has occurred.

HB_OCF—H-Bridge Overcurrent Flag Bit

This read / write flag is set on an overcurrent condition at the H-Bridges. Clear HB_OCF and enable the H-Bridge driver by writing a logic [1] to HB_OCF. Reset clears the HB_OCF bit. Writing a logic [0] to HB_OCF has no effect.

- 1 = Overcurrent condition on H-Bridges has occurred.
- 0 = No overcurrent condition on H-Bridges has occurred.

HTF—Overtemperature Status Bit

This read-only bit is a copy of the HTF bit in the Interrupt Flag Register.

- 1 = Overtemperature condition has occurred.
- 0 = No overtemperature condition has occurred.

AUTONOMOUS WATCHDOG (AWD)

The Autonomous Watchdog module allows to protect the CPU against code runaways.

The AWD is enabled if AWDRE in the AWDCTL Register is set. If this bit is cleared, the AWD oscillator is disabled and the watchdog switched off.

Watchdog

The watchdog function is only available in RUN mode. On setting the AWDRE bit, watchdog functionality in RUN mode is activated. Once this function is enabled, it is not possible to disable it via software.

If the timer reaches end value and AWDRE is set, a system reset is initiated. Operations of the watchdog function cease in STOP mode. Normal operation will be continued when the system is back to RUN mode.

To prevent a watchdog reset, the watchdog timeout counter must be reset before it reaches the end value. This is done by a write to the AWDRST bit in the AWDCTL Register.

Autonomous Watchdog Control Register (AWDCTL)

Register Name and Address: AWDCTL - $0a

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0	AWDRE	0 (14)	0 (14)	0	AWDR
Write			AWDRST					
Reset	0	0	0	0	0	0	0	0

Notes
16. This bit must always be set to 0.

AWDRST—Autonomous Watchdog Reset Bit

This write-only bit resets the Autonomous Watchdog timeout period. AWDRST always reads 0. Reset clears AWDRST bit.

- 1 = Reset AWD and restart timeout period.
- 0 = No effect.

AWDRE—Autonomous Watchdog Reset Enable Bit

This read/write bit enables resets on AWD time-outs. A reset on the $\overline{\text{RST\_A}}$ is asserted when the Autonomous Watchdog has reached the timeout and the Autonomous Watchdog is enabled. AWDRE is one-time setable (write once) after each reset. Reset clears the AWDRE bit.

- 1 = Autonomous watchdog enabled.
- 0 = Autonomous watchdog disabled.

AWDR—Autonomous Watchdog Rate Bit

This read/write bit selects the clock rate of the Autonomous Watchdog. Reset clears the AWDR bit.

- 1 = Fast rate selected (10 ms).
- 0 = Slow rate selected (20 ms).

VOLTAGE REGULATOR

The 908E626 chip contains a low-power, low-drop voltage regulator to provide internal power and external power for the MCU. The V_{DD} regulator accepts a unregulated input supply and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD terminal to provide the 5.0 V to the microcontroller.

FACTORY TRIMMING AND CALIBRATION

To enhance the ease-of-use of the 908E626, various parameters (e.g. ICG trim value) are stored in the flash memory of the device. The following flash memory locations are reserved for this purpose and might have a value different from the *empty* (0xFF) state:

- 0xFD80:0xFDDF Trim and Calibration Values
- 0xFFFE:0xFFFF Reset Vector

In the event the application uses these parameters, one has to take care not to erase or override these values. If these parameters are not used, these flash locations can be erased and otherwise used.

Trim Values

Below the usage of the trim values located in the flash memory is explained

Internal Clock Generator (ICG) Trim Value

The internal clock generator (ICG) module is used to create a stable clock source for the microcontroller without using any external components. The untrimmed frequency of the low-frequency base clock (IBASE), will vary as much as ±25 percent due to process, temperature, and voltage dependencies. To compensate this dependancies a ICG trim values is located at adress $FDC2. After trimming the ICG is a range of typ. ±2% (±3% max.) at nominal conditions (filtered (100nF) and stabilized (4,7uF) V_{DD} = 5V, $T_{Ambient}$~25°C) and will vary over temperature and voltage (VDD) as indicated in the 68HC908EY16 datasheet.

To trim the ICG this values has to be copied to the ICG Trim Register ICGTR at adress $38 of the MCU.

Important The value has to be copied after every reset.

TYPICAL APPLICATIONS

DEVELOPMENT SUPPORT

As the 908E626 has the MC68HC908EY16 MCU embedded typically all the development tools available for the MCU also apply for this device, however due to the fact of the additional analog die circuitry and the nominal +12V supply voltage some additional items have to be considered:

- nominal 12V rather than 5V or 3V supply
- high voltage V_{TST} might be applied not only to $\overline{IRQ}$ terminal, but $\overline{IRQ\_A}$ terminal

For a detailed information on the MCU related development support see the MC68HC908EY16 datasheet - section development support.

The programming is principially possible at two stages in the manufacturing process - first on chip level, before the IC is soldered onto a pcb board and second after the IC is soldered onto the pcb board.

Chip level programming

On Chip level the easiest way is to only power the MCU with +5V (see Figure 15) and not to provide the analog chip with VSUP, in this setup all the analog terminal should be left open (e.g. VSUP[1:3]) and interconnections between MCU and analog die have to be separated (e.g. $\overline{IRQ}$ - $\overline{IRQ\_A}$).

This mode is well descripted in the MC68HC908EY16 datasheet - section development support.

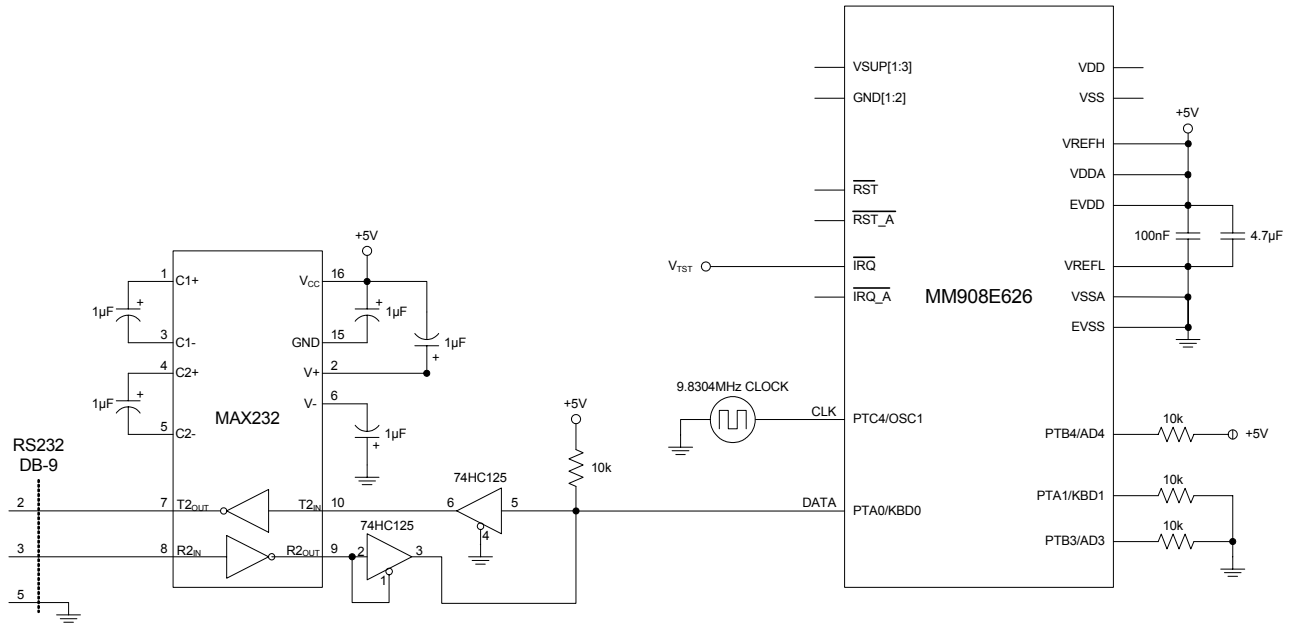


Figure 15. Normal Monitor Mode Circuit (MCU only)

Of course its also possible to supply the whole system with Vsup (12V) instead as descibted in Figure 16, page 31.

PCB level programming

If the IC is soldered onto the pcb board its typically not possible to seperately power the MCU with +5V, the whole

system has to be powered up providing V_{SUP} (see Figure 16).

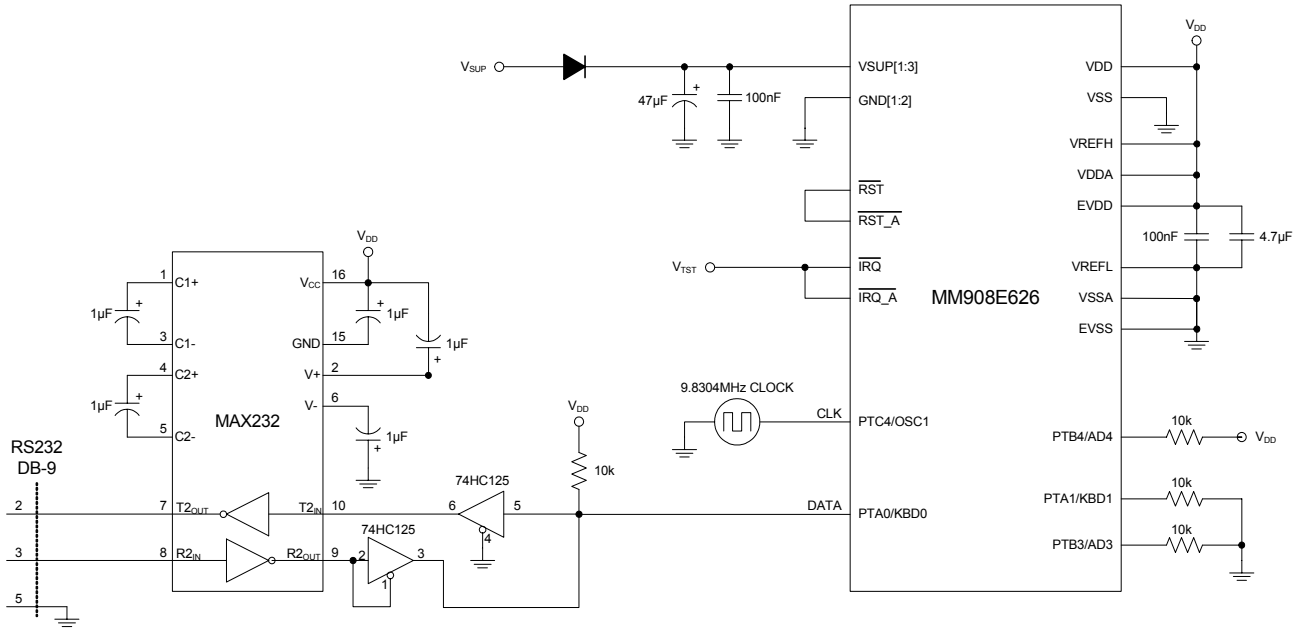


Figure 16. Normal Monitor Mode Circuit

Table 7 summarizes the possible configurations and the necessary setups.

Table 7. Monitor Mode Signal Requirements and Options

Mode	IRQ	RST	Reset Vector	Serial Communication		Mode Selection		ICG	COP	Normal Request Timeout	Communication Speed		
				PTA0	PTA1	PTB3	PTB4				External Clock	Bus Frequency	Baud Rate
Normal Monitor	V_{TST}	V_{DD}	X	1	0	0	1	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
Forced Monitor	V_{DD}	V_{DD}	$FFFF (blank)	1	0	X	X	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
	GND							ON	disabled	disabled	—	Nominal 1.6MHz	Nominal 6300
User	V_{DD}	V_{DD}	not $FFFF (not blank)	X	X	X	X	ON	enabled	enabled	—	Nominal 1.6MHz	Nominal 6300

Notes

1. PTA0 must have a pullup resistor to V_{DD} in monitor mode
2. External clock is a 4.9152MHz, 9.8304MHz or 19.6608MHz canned oscillator on OCS1
3. Communication speed with external clock is depending on external clock value. Baud rate is bus frequency / 256
4. X = don't care
5. V_{TST} is a high voltage $V_{DD} + 3.5V \le V_{TST} \le V_{DD} + 4.5V$

EMC/EMI RECOMMENDATIONS

This paragraph gives some device specific recommendations to improve EMC/EMI performance. Further generic design recommendations can be e.g. found on the Freescale website www.freescale.com.

VSUP terminals (VSUP1:VSUP3)

Its recommended to place a high-quality ceramic decoupling capacitor close to the VSUP terminals to improve EMC/EMI behaviour.

LIN terminal

For DPI (Direct Power Injection) and ESD (Electro Static Discharge) its recommended to place a high-quality ceramic decoupling capacitor near the LIN terminal. An additional varistor will further increase the immunity against ESD. A ferrit in the LIN line will suppress some of the noise induced.

Voltage regulator output terminals (VDD and AGND)

Use a high-quality ceramic decoupling capacitor to stabilize the regulated voltage.

MCU digital supply terminals (EVDD and EVSS)

Fast signal transitions on MCU terminals place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU. It is recommended that a high-quality ceramic decoupling capacitor be placed between these terminals.

MCU analog supply terminals (VREFH, VDDA and VREFL, VSSA)

To avoid noise on the analog supply terminals its important to take special care on the layout. The MCU digital and analog supplies should be tied to the same potential via seperate traces and connected to the voltage regulator output.

Figure 17 and Figure 18 show the recommendations on schematics and layout level and Table 8 incidates recommended external components and layout considerations.

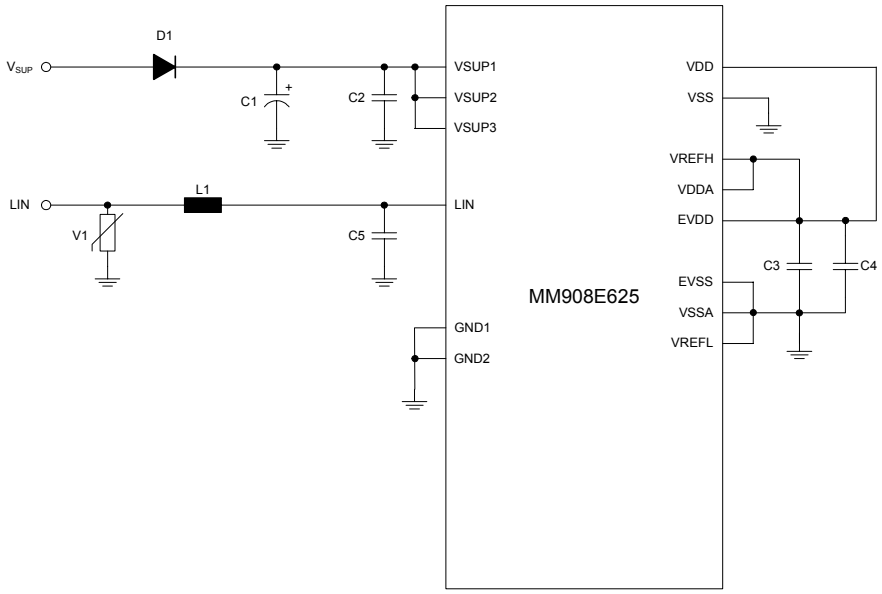


Figure 17. EMC/EMI recommendations

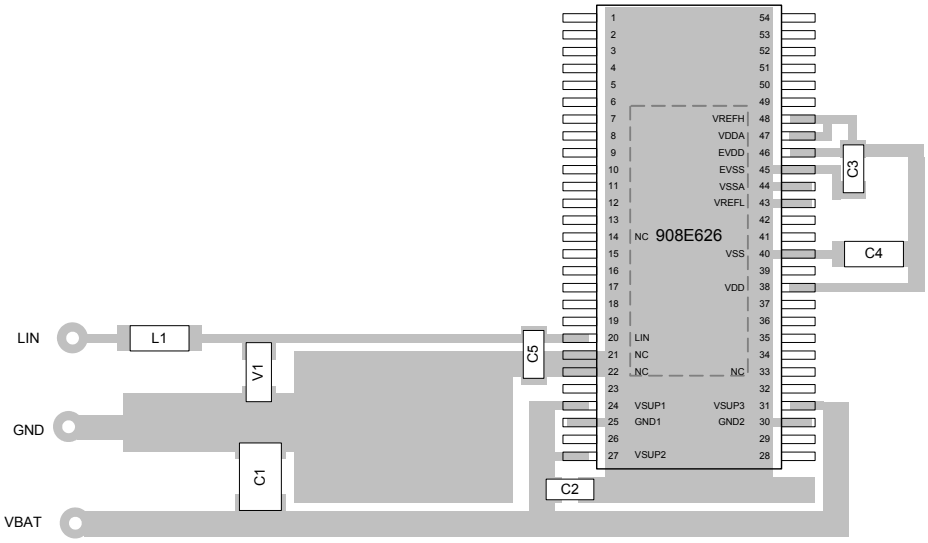


Figure 18. PCB Layout Recommendations

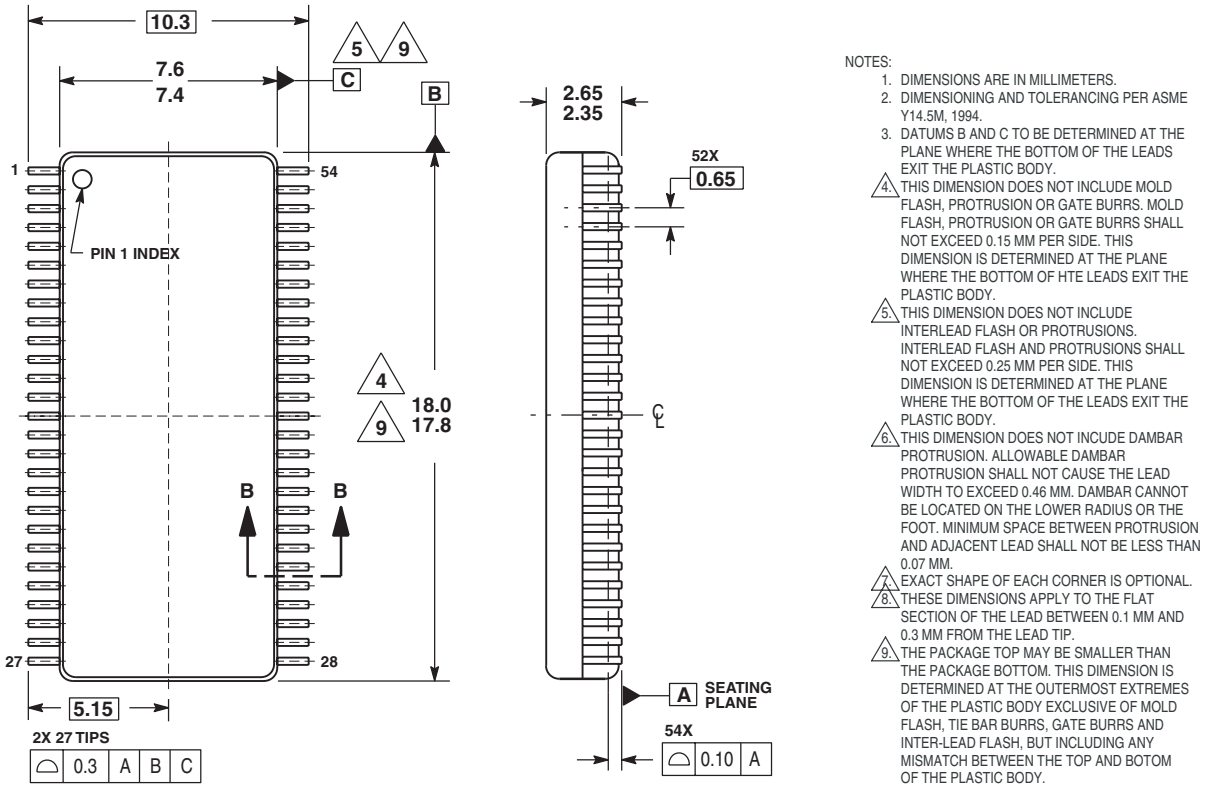
Table 8. Component Value Recommendation

Component	Recommended Value[1]	Comments / Signal routing
C1	Bulk Capacitor	
C2	100nF, SMD Ceramic, Low ESR	Close (<5mm) to VSUP1, VSUP2 terminals with good ground return
C3	100nF, SMD Ceramic, Low ESR	Close (<3mm) to digital supply terminals (EVDD, EVSS) with good ground return. The positive analog (VREFH, VDDA) and the digital (EVDD) supply should be connected right at the C3.
C4	4,7uF, SMD Ceramic, Low ESR	Bulk Capacitor
C5	180pF, SMD Ceramic, Low ESR	Close (<5mm) to LIN terminal. Total Capacitance on LIN has to be below 220pF. (C_{total} = $C_{LIN-Terminal}$ + C5 + $C_{Varistor}$ ~ 10pF + 180pF + 15pF)
V1[2]	Varistor Type TDK AVR-M1608C270MBAAB	Optional (close to LIN connector)
L1[2]	SMD Ferrite Bead Type TDK MMZ2012Y202B	Optional, (close to LIN connector)

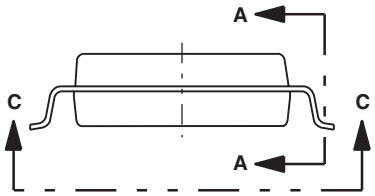
Notes
1. Freescale does not assume liability, endorse, or want components from external manufactures that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.
2. Components are recommended to improve EMC and ESD performance.

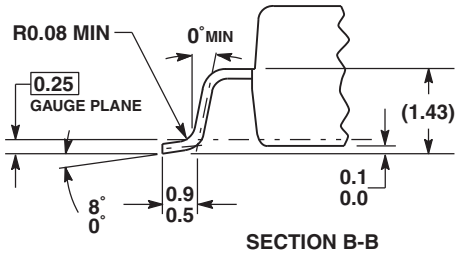
PACKAGING DIMENSIONS

Important: For the most current revision of the package, visit www.freescale.com and perform a keyword search on 98ARL105910.

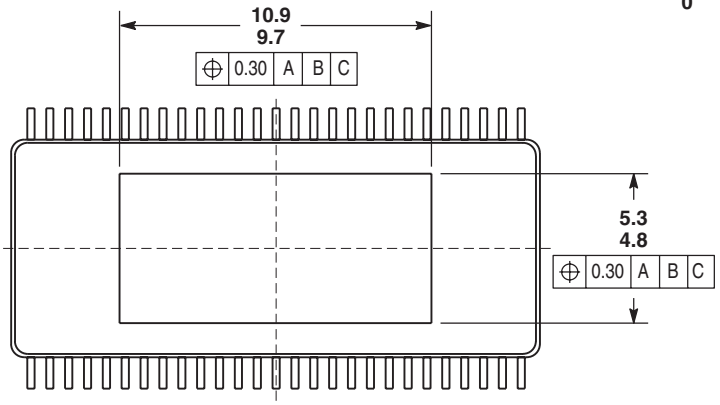


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF HTE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 MM.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.3 MM FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTOM OF THE PLASTIC BODY.

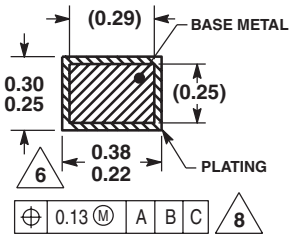




SECTION B-B



VIEW C-C



SECTION A-A
ROTATED 90° CLOCKWISE

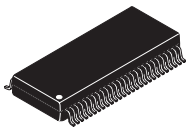
908E626

ADDITIONAL DOCUMENTATION

THERMAL ADDENDUM (REV 1.0)

908E626

54-TERMINAL SOICW-EP



DWB SUFFIX
98ARL105910
54-TERMINAL SOICW-EP

Note For package dimensions, refer to the 908E626 device datasheet.

Introduction

This thermal addendum ia provided as a supplement to the MM908E626 technical data sheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application and packaging information is provided in the data sheet.

Package and Thermal Considerations

This MM908E626 is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2. This results in two junction temperatures, T_{J1} and T_{J2}, and a thermal resistance matrix with $R_{\theta JAmn}$.

For *m*, *n* = 1, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1.

For *m* = 1, *n* = 2, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2. This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

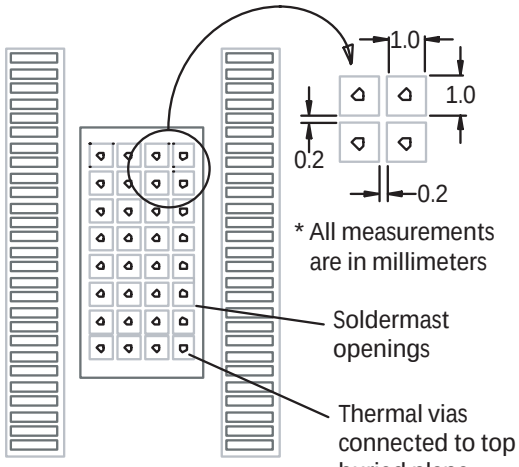
The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 9. Thermal Performance Comparison

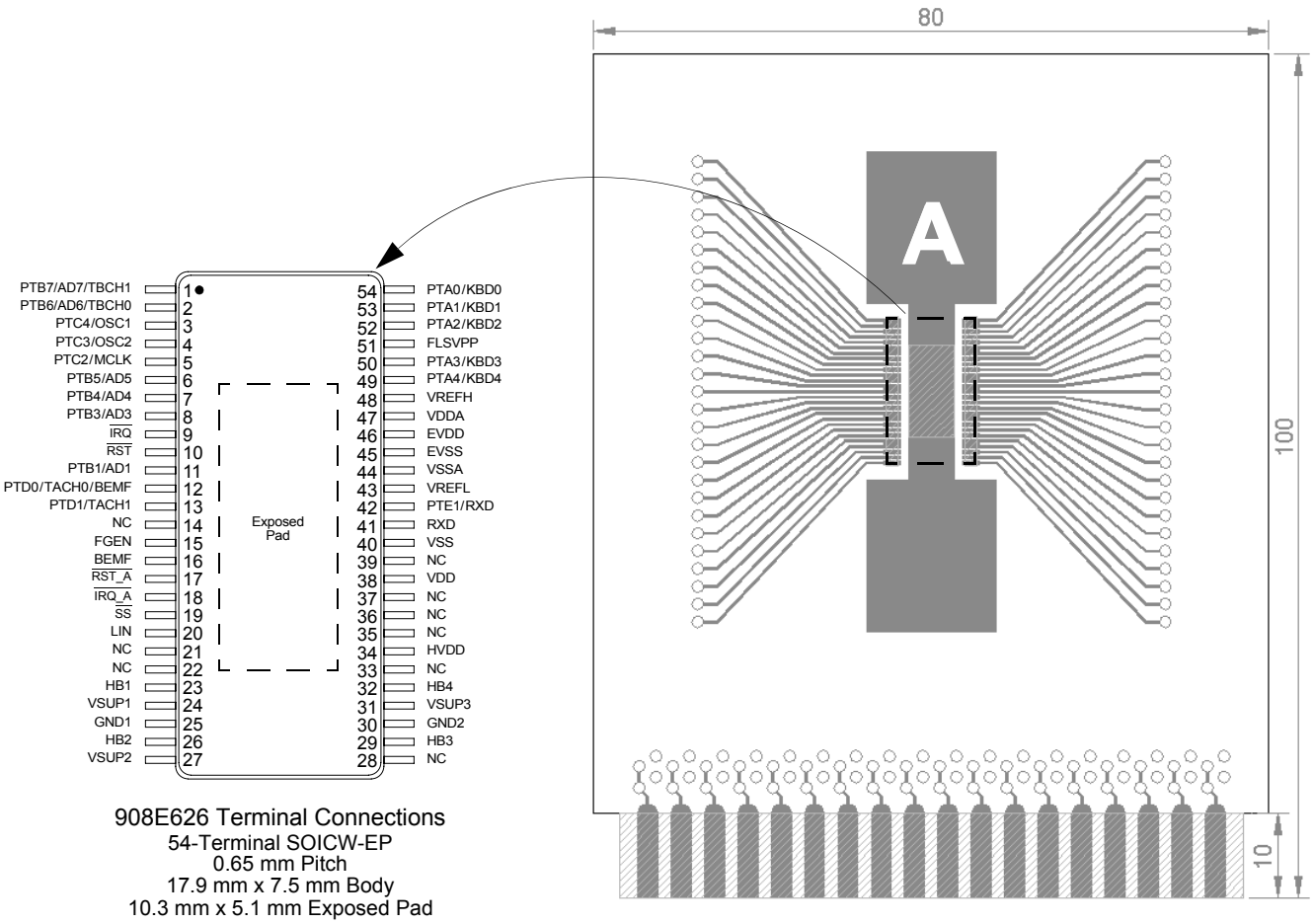
Thermal Resistance	1 = Power Chip, 2 = Logic Chip [°C/W]		
	***m* = 1, *n* = 1**	***m* = 1, *n* = 2** ***m* = 2, *n* = 1**	***m* = 2, *n* = 2**
$R_{\theta JAmn}$ (1)(2)	23	20	24
$R_{\theta JBmn}$ (2)(3)	9.0	6.0	10
$R_{\theta JAmn}$ (1)(4)	52	47	52
$R_{\theta JCmn}$ (5)	1.0	0	2.0

Notes:
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, “infinite” heat sink attached to exposed pad.



54 Terminal SOIC-EP
0.65 mm Pitch
17.9 mm x 7.5 mm Body
10.3 mm x 5.1 mm Exposed Pad

Figure 19. Thermal Land Pattern for Direct Thermal Attachment Per JEDEC JESD51-5Thermal Test Board



908E626 Terminal Connections
54-Terminal SOICW-EP
0.65 mm Pitch
17.9 mm x 7.5 mm Body
10.3 mm x 5.1 mm Exposed Pad

Figure 20. Thermal Test Board

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area **A**:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 10. Thermal Resistance Performance

Thermal Resistance	Area A (mm^2)	1 = Power Chip, 2 = Logic Chip (°C/W)		
		m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$	0	53	48	53
	300	39	34	38
	600	35	30	34
$R_{\theta JSmn}$	0	21	16	20
	300	15	11	15
	600	14	9.0	13

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

$R_{\theta JSmn}$ is the thermal resistance between die junction and the reference location on the board surface near a center lead of the package.

This device is a dual die package. Index *m* indicates the die that is heated. Index *n* refers to the number of the die where the junction temperature is sensed.

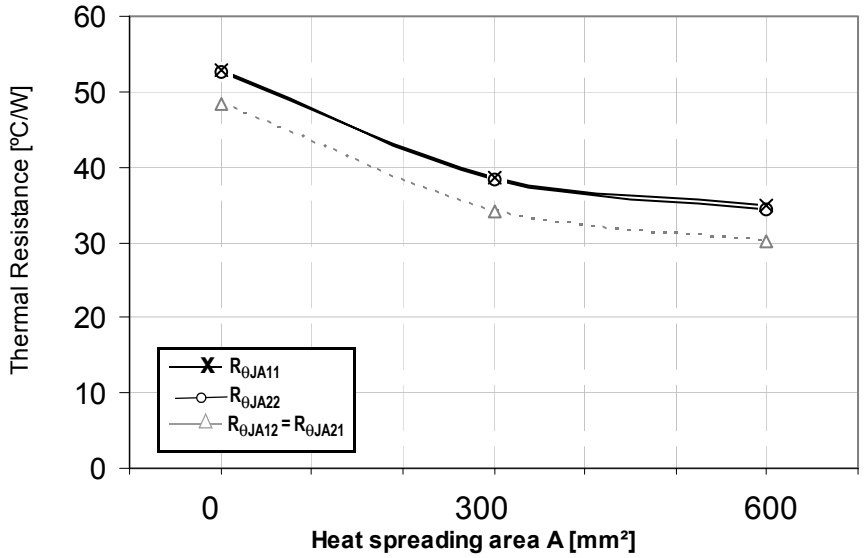


Figure 21. Device on Thermal Test Board $R_{\theta JA}$

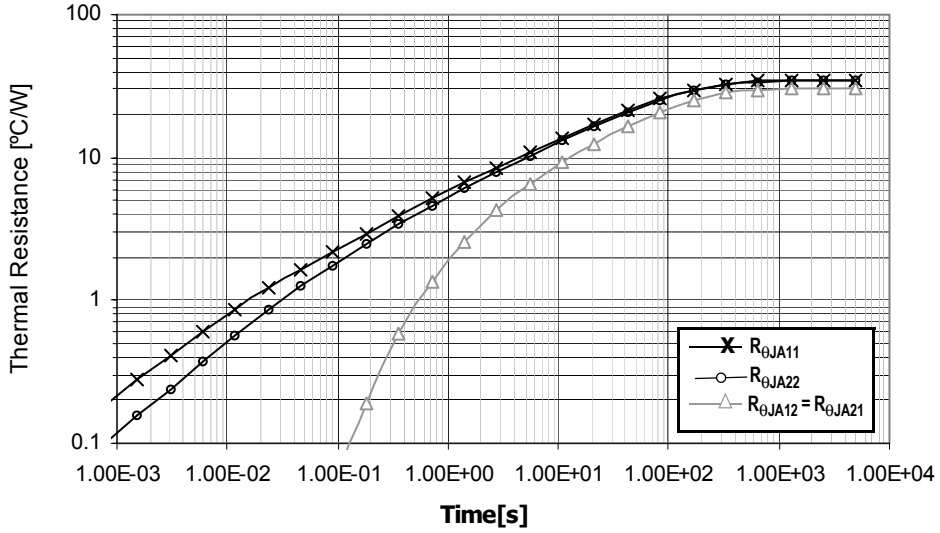


Figure 22. Transient Thermal Resistance $R_{\theta JA}$ (1.0 W Step Response)
Device on Thermal Test Board Area A = 600 (mm^2)

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MM908E626
Rev 3.0
12/2005

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