

## Multichannel Seismic Evaluation System

### Features

- Four-channel Seismic Acquisition Node
  - CS3301 geophone amplifiers (2x)
  - CS3302 hydrophone amplifiers (2x)
  - CS5372 dual  $\Delta\Sigma$  modulators (2x)
  - CS5376A quad digital filter (1x)
  - CS4373A  $\Delta\Sigma$  test DAC (1x)
  - Precision voltage reference
  - Clock recovery PLL
- On-board Microcontroller
  - SPI™ interface to digital filter
  - USB communication with PC
- PC Evaluation Software
  - Register setup & control
  - FFT frequency analysis
  - Time domain analysis
  - Noise histogram analysis

### General Description

The CDB5376 board is used to evaluate the functionality and performance of the Cirrus Logic multichannel seismic chip set. Data sheets for the CS3301, CS3302, CS4373A, CS5371/72, and CS5376A devices should be consulted when using the CDB5376 evaluation board.

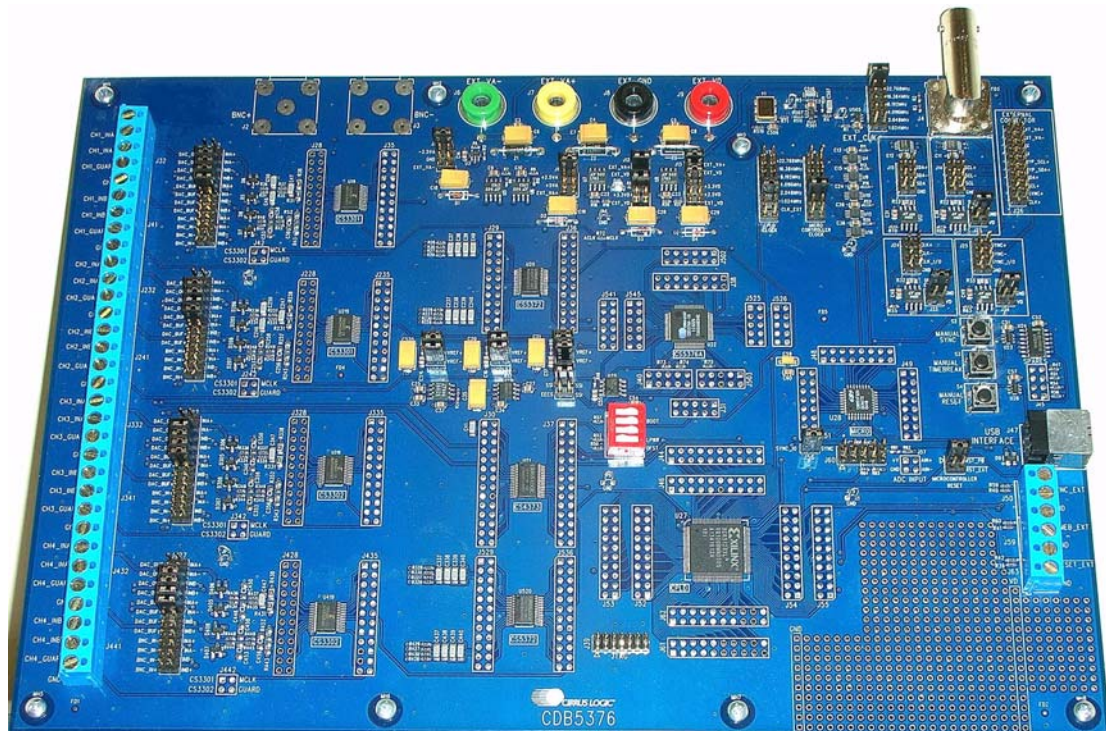
Screw terminals connect external differential geophone or hydrophone sensors to the analog inputs of the measurement channels. An on-board test DAC creates precision differential analog signals for in-circuit performance testing without an external signal source.

The evaluation board includes an 8051-type microcontroller with hardware SPI™ and USB serial interfaces. The microcontroller communicates with the digital filter via SPI and with the PC evaluation software via USB. The PC software controls register and coefficient initialization and performs time domain, histogram, and FFT frequency analysis on captured data.

### ORDERING INFORMATION

CDB5376

Evaluation Board



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## Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative. To find the one nearest to you go to [www.cirrus.com](http://www.cirrus.com)

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## **1. INITIAL SETUP**

### **1.1 Kit Contents**

The CDB5376 evaluation kit includes:

- CDB5376 Evaluation Board
- USB Cable (A to B)
- Software Download Information Card

The following are required to operate CDB5376, and are not included:

- Bipolar Power Supply with Banana Jack Outputs (+/-12 V @ 100 mA)
- Banana Jack Cables (4x)
- PC Running Windows 2000 or XP with an Available USB Port
- Internet Access to Download the Evaluation Software

### **1.2 Hardware Setup**

To set up the CDB5376 evaluation board:

- Set all jumpers and DIP switches to their default settings (see next sections).
- With power off, connect the CDB5376 power inputs to the power supply outputs.
  - VA- = -12 V
  - VA+ = +12 V
  - GND = 0 V
  - VD = +12 V
- Connect the USB cable between the CDB5376 USB connector and the PC USB port.
- Proceed to the Software Setup section to install the evaluation software and USB driver.

**1.2.1 Default Jumper Settings**

| J27, J227, J327, J427                         |    |       |   |    |      |
|---|----|-------|---|----|------|
| CH1, CH2, CH3, CH4<br>Analog Input Selections |    |       |   |    |      |
| DAC_OUT+                                      | 1  | *     | * | 2  | INA+ |
| DAC_OUT-                                      | 3  | *     | * | 4  | INA- |
| DAC_OUT-                                      | 5  | ----- |   | 6  | INB- |
| DAC_OUT+                                      | 7  | ----- |   | 8  | INB+ |
| DAC_BUF+                                      | 9  | ----- |   | 10 | INA+ |
| DAC_BUF-                                      | 11 | ----- |   | 12 | INA- |
| DAC_BUF-                                      | 13 | *     | * | 14 | INB- |
| DAC_BUF+                                      | 15 | *     | * | 16 | INB+ |
| BNC_IN+                                       | 17 | *     | * | 18 | INA+ |
| BNC_IN-                                       | 19 | *     | * | 20 | INA- |
| BNC_IN-                                       | 21 | *     | * | 22 | INB- |
| BNC_IN+                                       | 23 | *     | * | 24 | INB+ |

**Table 1. Analog Inputs Default Jumper Settings**

| J519, J19, J20            |   |       |   |
|---------------------------|---|-------|---|
| Voltage Reference Jumpers |   |       |   |
| VREF+                     | 1 | ----- | 2 |
| VREF-                     | 3 | ----- | 4 |

| J43                   |   |       |   |     |     |
|-----------------------|---|-------|---|-----|-----|
| SPI Chip Select Input |   |       |   |     |     |
| SSI                   | 1 | ----- | 2 | SSI |     |
| EECS                  | 3 | *     | * | 4   | SSI |

| J56                   |   |       |   |      |
|-----------------------|---|-------|---|------|
| SYNC Source Selection |   |       |   |      |
| SYNC_IO               | 1 | ----- | 2 | SYNC |

| J58                    |   |       |   |   |
|------------------------|---|-------|---|---|
| RESET Source Selection |   |       |   |   |
| RST_PB                 | 1 | ----- | 2 |   |
| RST_EXT                | 3 | *     | * | 4 |

**Table 2. VREF, SPI, SYNC, RESET Default Jumper Settings**

| <b>J10</b>                   |   |       |   |
|------------------------------|---|-------|---|
| <b>VA- Voltage Selection</b> |   |       |   |
| -2.5VA                       | 1 | ----- | 2 |
| GND                          | 3 | * *   | 4 |
| EXT_VA-                      | 5 | * *   | 6 |

| <b>J11</b>                   |   |       |   |
|------------------------------|---|-------|---|
| <b>VA+ Voltage Selection</b> |   |       |   |
| +2.5VA                       | 1 | ----- | 2 |
| +5VA                         | 3 | * *   | 4 |
| EXT_VA+                      | 5 | * *   | 6 |

| <b>J12</b>                     |   |       |   |
|--------------------------------|---|-------|---|
| <b>VD Input Voltage Source</b> |   |       |   |
| EXT_VA+                        | 1 | * *   | 2 |
| EXT_VD                         | 3 | ----- | 4 |

| <b>J13</b>                        |   |       |   |
|-----------------------------------|---|-------|---|
| <b>VCORE Input Voltage Source</b> |   |       |   |
| EXT_VA+                           | 1 | * *   | 2 |
| EXT_VD                            | 3 | ----- | 4 |

| <b>J22</b>                  |   |       |   |
|-----------------------------|---|-------|---|
| <b>VD Voltage Selection</b> |   |       |   |
| +3.3VD                      | 1 | ----- | 2 |
| EXT_VD                      | 3 | * *   | 4 |

| <b>J21</b>                     |   |       |   |
|--------------------------------|---|-------|---|
| <b>VCORE Voltage Selection</b> |   |       |   |
| +3.3VD                         | 1 | ----- | 2 |
| +2.5VD                         | 3 | * *   | 4 |
| EXT_VD                         | 3 | * *   | 4 |

**Table 3. Power Supplies Default Jumper Settings**

| <b>J16</b>                       |    |       |    |
|----------------------------------|----|-------|----|
| <b>PLL Input Clock Selection</b> |    |       |    |
| 32.768 MHz                       | 1  | ----- | 2  |
| 16.384 MHz                       | 3  | * *   | 4  |
| 8.192 MHz                        | 5  | * *   | 6  |
| 4.096 MHz                        | 7  | * *   | 8  |
| 2.048 MHz                        | 9  | * *   | 10 |
| 1.024 MHz                        | 11 | * *   | 12 |

| <b>J17, J18</b>                                     |    |       |    |
|---|----|-------|----|
| <b>CPLD, Microcontroller Input Clock Selections</b> |    |       |    |
| 32.768 MHz  | 1  | * *   | 2  |
| 16.384 MHz  | 3  | * *   | 4  |
| 8.192 MHz   | 5  | * *   | 6  |
| 4.096 MHz   | 7  | * *   | 8  |
| 2.048 MHz   | 9  | * *   | 10 |
| 1.024 MHz   | 11 | ----- | 12 |
| CLK_EXT   | 13 | * *   | 14 |
|   | 15 | * *   | 16 |

**Table 4. Clock Inputs Default Jumper Settings**

|                 |   |       |   |
|-----------------|---|-------|---|
| <b>J15</b>      |   |       |   |
| <b>I2C Data</b> |   |       |   |
| SDA+            | 1 | ----- | 2 |
| SDA-            | 3 | ----- | 4 |
| SDA             | 5 | * *   | 6 |
| GND             | 7 | * *   | 8 |

|                  |   |       |   |
|------------------|---|-------|---|
| <b>J14</b>       |   |       |   |
| <b>I2C Clock</b> |   |       |   |
| SCL+             | 1 | ----- | 2 |
| SCL-             | 3 | ----- | 4 |
| SCL              | 5 | * *   | 6 |
| GND              | 7 | * *   | 8 |

|                                |   |       |   |
|--------------------------------|---|-------|---|
| <b>J23</b>                     |   |       |   |
| <b>I2C Clock Driver Enable</b> |   |       |   |
| GND                            | 1 | ----- | 2 |
| VD                             | 3 | * *   | 4 |

|                     |   |       |   |
|---------------------|---|-------|---|
| <b>J24</b>          |   |       |   |
| <b>Clock Source</b> |   |       |   |
| CLK+                | 1 | ----- | 2 |
| CLK-                | 3 | ----- | 4 |
| CLK_I/O             | 5 | * *   | 6 |
| GND                 | 7 | * *   | 8 |

|                    |   |       |   |
|--------------------|---|-------|---|
| <b>J25</b>         |   |       |   |
| <b>Sync Source</b> |   |       |   |
| SYNC+              | 1 | ----- | 2 |
| SYNC-              | 3 | ----- | 4 |
| SYNC_I/O           | 5 | * *   | 6 |
| GND                | 7 | * *   | 8 |

|                            |   |       |   |
|----------------------------|---|-------|---|
| <b>J33</b>                 |   |       |   |
| <b>Clock Driver Enable</b> |   |       |   |
| GND                        | 1 | ----- | 2 |
| VD                         | 3 | * *   | 4 |

|                           |   |       |   |
|---------------------------|---|-------|---|
| <b>J34</b>                |   |       |   |
| <b>Sync Driver Enable</b> |   |       |   |
| GND                       | 1 | ----- | 2 |
| VD                        | 3 | * *   | 4 |

**Table 5. RS-485 Default Jumper Settings**

### 1.2.2 Default DIP Switch Settings

|                  |   |   |   |   |
|------------------|---|---|---|---|
| <b>S5</b>        |   |   |   |   |
| * = down, - = up |   |   |   |   |
| BOOT             | 1 | * | - | 2 |
|                  | 3 | * | - | 4 |
| LPWR             | 5 | * | - | 6 |
| OFST             | 7 | - | * | 8 |

**Table 6. DIP Switch Default Settings**



## 1.3 Software Setup

### 1.3.1 PC Requirements

The PC hardware requirements for the Cirrus Seismic Evaluation system are:

- *Windows XP™, Windows 2000™, Windows NT®*
- *Intel® Pentium® 600MHz or higher microprocessor*
- *VGA resolution or higher video card*
- *Minimum 64MB RAM*
- *Minimum 40MB free hard drive space*

### 1.3.2 Seismic Evaluation Software Installation

**Important:** For reliable USB communication, the USBXpress driver must be installed after the Seismic Evaluation Software installation but **before** launching the application. The USBXpress driver files are included in a sub-folder as part of the installation.

To install the Cirrus Logic Seismic Evaluation Software:

- Go to the Cirrus Logic Industrial Software web page (<http://www.cirrus.com/industrialsoftware>). Click the link for “*Cirrus Seismic Evaluation GUI*” to get to the download page and then click the link for “*Cirrus Seismic Evaluation GUI Release Vxx*” (xx indicates the version number).
- Read the software license terms and click “*Accept*” to download the “*SeismicEvalGUI\_vxx.zip*” file to any directory on the PC.
- Unzip the downloaded file to any directory and a “*distribution*” sub-folder containing the installation application will automatically be created.
- Open the “*distribution*” sub-folder and run “*setup.exe*”. If the Seismic Evaluation Software has been previously installed, the uninstall wizard will automatically remove the previous version and you will need to run “*setup.exe*” again.
- Follow the instructions presented by the Cirrus Seismic Evaluation Installation Wizard. The default installation location is “*C:\Program Files\Cirrus Seismic Evaluation*”.

An application note, AN271 - *Cirrus Seismic Evaluation GUI Installation Guide*, is available from the Cirrus Logic web site with step-by-step instructions on installing the Seismic Evaluation Software.

### 1.3.3 USBXpress Driver Installation

**Important:** For reliable USB communication, the USBXpress driver must be installed after the Seismic Evaluation Software installation but **before** launching the application. The USBXpress driver files are included in a sub-folder as part of the installation.

The Cirrus Logic Seismic Evaluation Software communicates with CDB5376 via USB using the USBXpress driver from Silicon Laboratories (<http://www.silabs.com>). For convenience, the USBXpress driver files are included as part of the installation package.

To install the USBXpress driver (after installing the Seismic Evaluation Software):

- Connect CDB5376 to the PC through an available USB port and apply power. The PC will detect CDB5376 as an unknown USB device.
- If prompted for a USB driver, skip to the next step. If not, using Windows Hardware Device Manager go to the properties of the unknown USB API device and select “*Update Driver*”.
- Select “*Install from a list or specific location*”, then select “*Include this location in the search*” and then browse to “*C:\Program Files\Cirrus Seismic Evaluation\Driver\*”. The PC will recognize and install the USBXpress device driver.
- After driver installation, cycle power to CDB5376. The PC will automatically detect it and add it as a USBXpress device in the Windows Hardware Device Manager.

An application note, AN271 - *Cirrus Seismic Evaluation GUI Installation Guide*, is available from the Cirrus Logic web site with step-by-step instructions on installing the USBXpress driver.

### 1.3.4 **Launching the Seismic Evaluation Software**

**Important:** For reliable USB communication, the USBXpress driver must be installed after the Seismic Evaluation Software installation but **before** launching the application. The USBXpress driver files are included in a sub-folder as part of the installation.

To launch the Cirrus Seismic Evaluation Software, go to:

- *Start ⇒ Programs ⇒ Cirrus Seismic Evaluation ⇒ Cirrus Seismic Evaluation*

or:

- *C:\Program Files\Cirrus Seismic Evaluation\SeismicGUI.exe*

For the most up-to-date information about the software, please refer to its help file:

- Within the software: *Help ⇒ Contents*

or:

- *Start ⇒ Programs ⇒ Cirrus Seismic Evaluation ⇒ SEISMICGUI*

or:

- *C:\Program Files\Cirrus Seismic Evaluation\SEISMICGUI.HLP*

## 1.4 Self-testing CDB5376

Noise and distortion self-tests can be performed once hardware and software setup are complete.

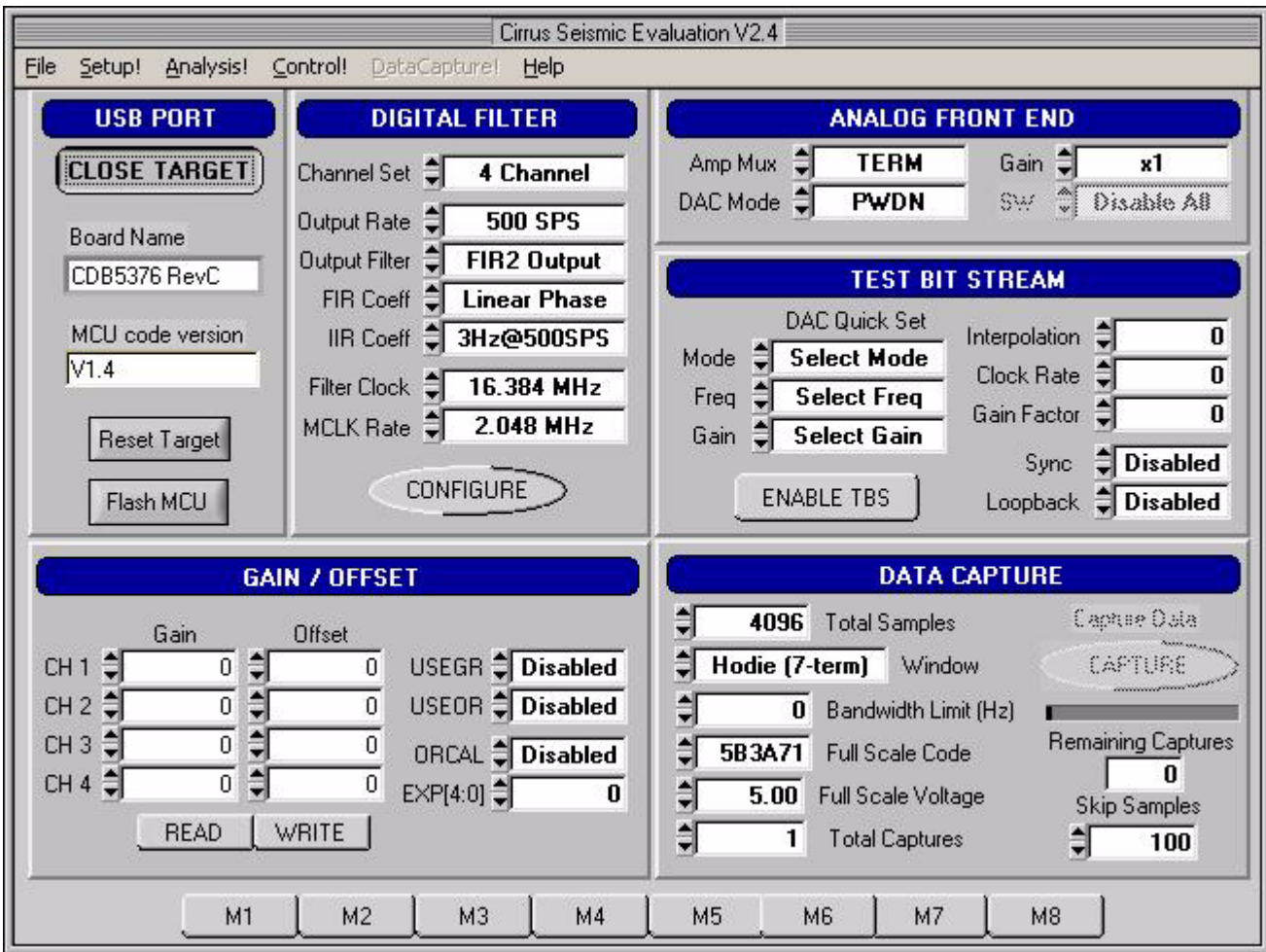
First, initialize the CDB5376 evaluation system:

- Launch the evaluation software and apply power to CDB5376.
- Click 'OK' on the **About** panel to get to the **Setup** panel.
- On the **Setup** panel, select *Open Target* on the **USB Port** sub-panel.
- When connected, the *Board Name* and *MCU code version* will be displayed.

### 1.4.1 Noise test

Noise performance of the measurement channel can be tested as follows:

- Set the controls on the **Setup** panel to match the picture:



The screenshot shows the 'Setup' panel of the 'Cirrus Seismic Evaluation V2.4' software. The panel is divided into several sections:

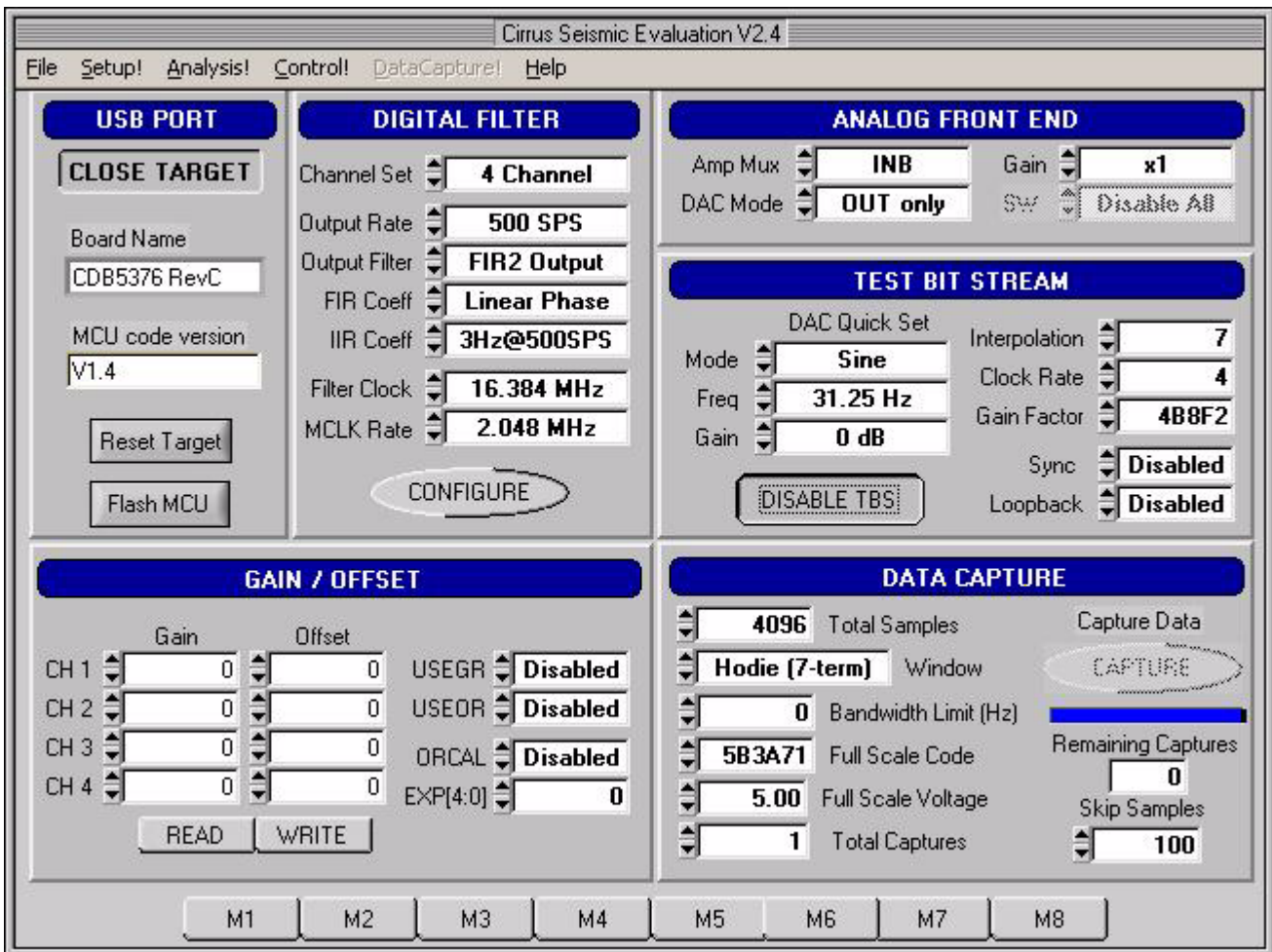
- USB PORT:** Includes a 'CLOSE TARGET' button, fields for 'Board Name' (CDB5376 RevC) and 'MCU code version' (V1.4), and buttons for 'Reset Target' and 'Flash MCU'.
- DIGITAL FILTER:** Includes dropdowns for 'Channel Set' (4 Channel), 'Output Rate' (500 SPS), 'Output Filter' (FIR2 Output), 'FIR Coeff' (Linear Phase), 'IIR Coeff' (3Hz@500SPS), 'Filter Clock' (16.384 MHz), and 'MCLK Rate' (2.048 MHz). A 'CONFIGURE' button is at the bottom.
- ANALOG FRONT END:** Includes dropdowns for 'Amp Mux' (TERM) and 'DAC Mode' (PWDN), and spinners for 'Gain' (x1) and 'SW' (Disable All).
- TEST BIT STREAM:** Includes a 'DAC Quick Set' section with 'Mode' (Select Mode), 'Freq' (Select Freq), and 'Gain' (Select Gain) dropdowns. It also has spinners for 'Interpolation' (0), 'Clock Rate' (0), and 'Gain Factor' (0). 'Sync' and 'Loopback' are set to 'Disabled'. An 'ENABLE TBS' button is present.
- GAIN / OFFSET:** Includes a table for Gain and Offset for CH 1 through CH 4, all set to 0. It also has dropdowns for 'USEGR' (Disabled), 'USEOR' (Disabled), 'ORCAL' (Disabled), and 'EXP[4:0]' (0). 'READ' and 'WRITE' buttons are at the bottom.
- DATA CAPTURE:** Includes spinners for 'Total Samples' (4096), 'Bandwidth Limit (Hz)' (0), 'Full Scale Code' (5B3A71), and 'Full Scale Voltage' (5.00). It also has a 'Window' dropdown (Hodie (7-term)), 'Total Captures' (1), and 'Skip Samples' (100). A 'CAPTURE' button is circled.

At the bottom of the interface are buttons labeled M1 through M8.

- Once the **Setup** panel is set, select *Configure* on the **Digital Filter** sub-panel.
- After digital filter configuration is complete, click *Capture* to collect a data record.
- Once the data record is collected, the **Analysis** panel is automatically displayed.
- Select *Noise FFT* from the *Test Select* control to display the calculated noise statistics.
- Verify the noise performance (S/N) is 124 dB or better.

### 1.4.2 Distortion Test

- Set the controls on the **Setup** panel to match the picture:



The screenshot shows the Cirrus Seismic Evaluation V2.4 software interface. The **Setup** panel is active, displaying various configuration options:

- USB PORT:** Board Name: CDB5376 RevC, MCU code version: V1.4. Buttons: Reset Target, Flash MCU.
- DIGITAL FILTER:** Channel Set: 4 Channel, Output Rate: 500 SPS, Output Filter: FIR2 Output, FIR Coeff: Linear Phase, IIR Coeff: 3Hz@500SPS, Filter Clock: 16.384 MHz, MCLK Rate: 2.048 MHz. Button: CONFIGURE.
- ANALOG FRONT END:** Amp Mux: INB, Gain: x1, DAC Mode: OUT only, SW: Disable All.
- TEST BIT STREAM:** DAC Quick Set: Sine, Mode: Sine, Freq: 31.25 Hz, Gain: 0 dB, Interpolation: 7, Clock Rate: 4, Gain Factor: 4B8F2, Sync: Disabled, Loopback: Disabled. Button: DISABLE TBS.
- GAIN / OFFSET:** Gain and Offset controls for CH 1, 2, 3, and 4. USEGR, USEOR, ORCAL, and EXP[4:0] are all Disabled. Buttons: READ, WRITE.
- DATA CAPTURE:** Total Samples: 4096, Window: Hodie (7-term), Bandwidth Limit (Hz): 0, Full Scale Code: 5B3A71, Full Scale Voltage: 5.00, Total Captures: 1. Capture Data: CAPTURE, Remaining Captures: 0, Skip Samples: 100.

At the bottom of the interface are buttons labeled M1 through M8.

- Once the **Setup** panel is set, select *Configure* on the **Digital Filter** sub-panel.
- After digital filter configuration is complete, click *Capture* to collect a data record.
- Once the data record is collected, the **Analysis** panel is automatically displayed.
- Select *Signal FFT* from the *Test Select* control to display the calculated signal statistics.
- Verify the distortion performance (S/D) is 112 dB or better.



## 2. HARDWARE DESCRIPTION

### 2.1 Block Diagram

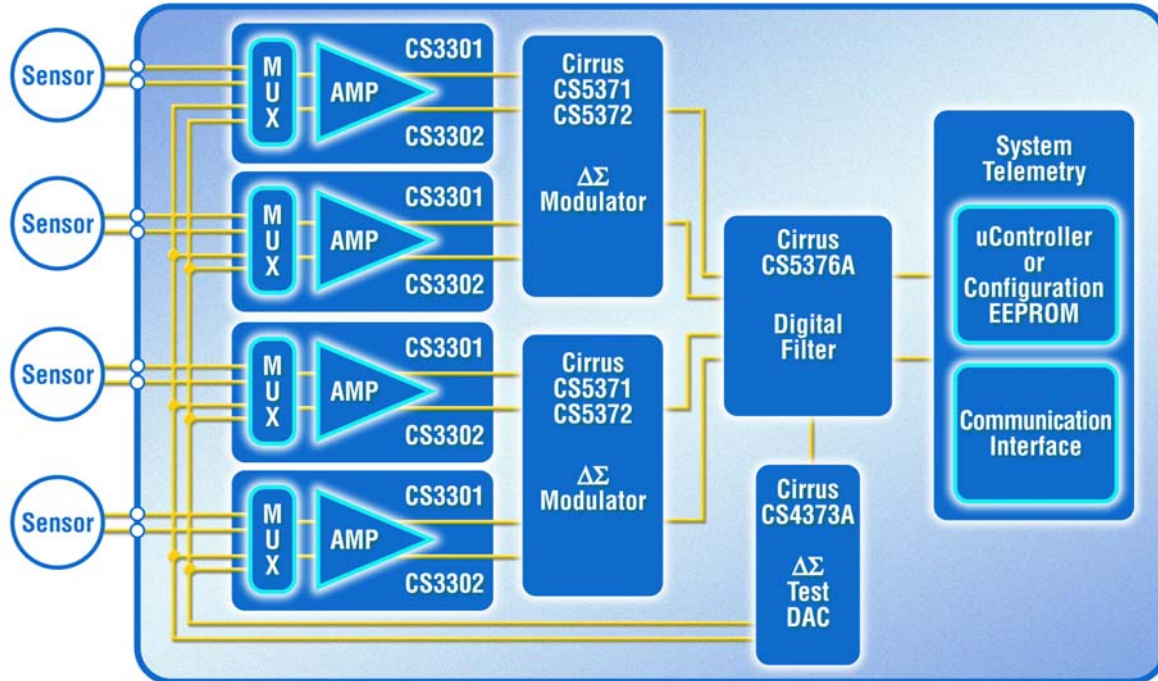


Figure 1. CDB5376 Block Diagram

Major blocks of the CDB5376 evaluation board include:

- **CS3301 Geophone Amplifier (2x)**
- **CS3302 Hydrophone Amplifier (2x)**
- **CS5372 Dual  $\Delta\Sigma$  Modulators (2x)**
- **CS5376A Quad Digital Filter**
- **CS4373A  $\Delta\Sigma$  Test DAC**
- **Precision Voltage Reference**
- **Interface CPLD**
- **Microcontroller with USB**
- **Phase Locked Loop**
- **RS-485 Transceivers**
- **Voltage Regulators**

## 2.2 Analog Hardware

### 2.2.1 Analog Inputs

#### 2.2.1.1 External Inputs - INA, INB, BNC

External signals into CDB5376 are from two major classes of sensors, moving coil geophones and piezo-electric hydrophones. Geophones are low-impedance sensors optimized to measure vibrations in land applications. Hydrophones are high-impedance sensors optimized to measure pressure in marine applications. Other sensors for earthquake monitoring and military applications are considered as geophones for this datasheet.

External signals connect to CDB5376 through screw terminals on the left side of the PCB. For each channel (CH1, CH2, CH3, CH4), these screw terminals make connections to two external differential inputs, INA and INB. In addition, GND and GUARD connections are provided for connecting sensor cable shields, if present.

| Signal Input | Screw Terminal |
|--------------|----------------|
| CH1 INA      | J32            |
| CH1 INB      | J41            |
| CH2 INA      | J232           |
| CH2 INB      | J241           |
| CH3 INA      | J332           |
| CH3 INB      | J341           |
| CH4 INA      | J432           |
| CH4 INB      | J441           |

**Table 7. Screw Terminal Input Connectors**

BNC inputs for connecting external signals are not populated during board manufacture, but the empty PCB footprints exist and can be installed. The inner conductors of the BNC inputs make connections to the differential signal traces, with the outer shields connected to ground. The BNC inputs can be connected to any channel's INA or INB inputs through the input selection jumpers.

#### 2.2.1.2 GUARD Output, GND Connection

The CS3302 hydrophone amplifier provides a GUARD signal output designed to actively drive the cable shield of a high impedance sensor with the common mode voltage of the sensor differential signal. This GUARD output on the cable shield minimizes leakage by minimizing the voltage differential between the sensor signal and the cable shield.

By default, the GUARD signal is output to screw terminals on the left side of the PCB for channels 3 and 4, which use the CS3302 amplifier. There is no GUARD signal output for channels 1 and 2 since they use the CS3301 amplifier, so the GUARD screw terminals for these channels are left floating.

A separate GND connection screw terminal for each channel is also provided if a ground connection to the sensor cable shield is preferred.

### 2.2.1.3 Internal Inputs - DAC\_OUT, DAC\_BUF

The CS4373A test DAC has two high-performance differential test outputs, a precision output (DAC\_OUT) and a buffered output (DAC\_BUF). These test outputs can be connected to the INA or INB inputs of any channel through the input selection jumpers.

By default, CDB5376 is populated with passive RC filter components on the INA inputs, and no filter components on the INB inputs (though the component footprints are present on the INB inputs). Because the CS4373A precision output will not tolerate significant loading, on CDB5376 the DAC\_OUT signal should only jumper to the INB inputs. The CS4373A buffered outputs are less sensitive to the RC filter load and DAC\_BUF can be jumpered to either the INA or INB inputs.

### 2.2.1.4 Input Protection

Sensor inputs must have circuitry to protect the analog electronics from voltage spikes. Geophone coils are susceptible to magnetic fields (especially from lightning) and hydrophones can produce large voltage spikes if located near an air gun source.

Discrete switching diodes quickly clamp the analog inputs to the power supply rails when the input voltage spikes. These diodes are reverse biased in normal operation and have low reverse bias leakage and capacitance characteristics to maintain high linearity on the analog inputs.

| <b>Specification</b>                                       | <b>Value</b>                |
|--|-----------------------------|
| Dual Series Switching Diode - ON Semiconductor             | BAV99LT1                    |
| Surface Mount Package Type                                 | SOT-23                      |
| Non-Repetitive Peak Forward Current (1 $\mu$ s, 1 ms, 1 s) | 2.0 A, 1.0 A, 500 mA        |
| Reverse Bias Leakage (25 C to 85 C)                        | 0.004 $\mu$ A - 0.4 $\mu$ A |
| Reverse Bias Capacitance (0 V to 5 V)                      | 1.5 pF - 0.54 pF            |

### 2.2.1.5 Input RC Filters

Following the diode clamps is an RC filter network that bandwidth limits the sensor inputs into the amplifiers to “chop the tops off” residual voltage spikes not clamped by the discrete diodes. In addition, all Cirrus Logic component ICs have built in ESD protection diodes guaranteed to 2000 V HBM / 200 V MM (JEDEC standard). The small physical size of these ESD diodes restricts their current capacity to 10 mA.

For land applications using the CS3301 amplifier (CDB5376 channels 1 and 2), the INA input has a common mode and differential RC filter. The common mode filter sets a low-pass corner to shunt very high-frequency components to ground with minimal noise contribution. The differential filter sets a low-pass corner high enough not to affect the magnitude response of the measurement bandwidth.

For marine applications that use the CS3302 amplifier (CDB5376 channels 3 and 4), a differential low-pass filter rejects high-frequency signals into the amplifier. The cutoff frequency for the low-pass filter is high enough not to affect the magnitude response of the measurement bandwidth.

| <b>Land Common Mode Filter Specification</b> | <b>Value</b>     |
|--|------------------|
| Common Mode Capacitance                      | 10 nF $\pm$ 10%  |
| Common Mode Resistance                       | 200 $\Omega$     |
| Common Mode -3 dB Corner @ 6 dB/octave       | 80 kHz $\pm$ 10% |

| <b>Land Differential Filter Specification</b> | <b>Value</b>                               |
|---|--|
| Differential Capacitance                      | 10 nF $\pm$ 10%                            |
| Differential Resistance                       | 200 $\Omega$ + 200 $\Omega$ = 400 $\Omega$ |
| Differential -3 dB Corner @ 6 dB/octave       | 40 kHz $\pm$ 10%                           |

| <b>Marine Differential Filter Specification</b> | <b>Value</b>                               |
|---|--|
| Differential Capacitance                        | 10 nF $\pm$ 10%                            |
| Differential Resistance                         | 200 $\Omega$ + 200 $\Omega$ = 400 $\Omega$ |
| -3 dB Corner @ 6 dB/octave                      | 40 kHz $\pm$ 10%                           |

### 2.2.1.6 Common Mode Bias

Differential analog signals into the CS3301/02 amplifiers are required to be biased to the center of the power supply voltage range, which for bipolar supplies is near ground potential. This common mode bias voltage is created by buffering the voltage reference, which is nominally +2.5 V relative to the VA- power supply.

Resistors to create the common mode bias are selected based on the sensor impedance and may need to be modified from the CDB5376 defaults depending on the sensor to be used. Refer to the recommended operating bias conditions for the selected sensor, which are available from the sensor manufacturer.

| <b>Specification</b>              | <b>Value</b>                                   |
|-----------------------------------|--|
| Geophone Sensor Bias Resistance   | 20 k $\Omega$    20 k $\Omega$ = 10 k $\Omega$ |
| Hydrophone Sensor Bias Resistance | 18 M $\Omega$    18 M $\Omega$ = 9 M $\Omega$  |



## 2.2.2 Differential Amplifiers

The CS3301/02 amplifiers act as a low-noise gain stage for internal or external differential analog signals.

| Analog Signals | Description                            |
|----------------|--|
| INA            | Sensor analog input                    |
| INB            | Test DAC analog input                  |
| OUTR, OUTF     | Analog rough / fine outputs            |
| GUARD          | CS3302 guard output (jumper selection) |

| Digital Signals | Description                           |
|-----------------|---------------------------------------|
| MUX[0..1]       | Input mux selection                   |
| GAIN[0..2]      | Gain range selection                  |
| PWDN            | Power down mode enable                |
| CLK             | CS3301 clock input (jumper selection) |

### 2.2.2.1 ACLK Input vs. GUARD Output

By default, channels 1 and 2 of CDB5376 use the CS3301 geophone amplifier while channels 3 and 4 use the CS3302 hydrophone amplifier. The CS3301 amplifier is chopper stabilized and connects pin 13 to a clock source (ACLK) to run the chopper circuitry synchronous to the modulator analog sampling clock. The CS3302 device is not chopper stabilized (with 1/f noise typically buried below the low-frequency ocean noise) to achieve very high input impedance. To minimize leakage from high-impedance sensors connected to the CS3302 amplifier, pin 13 produces a GUARD signal output to actively drive a sensor cable shield with the common mode voltage of the sensor signal.

Comparing the CS3301 and CS3302 amplifiers, the functionality of pin 13 (ACLK input vs. GUARD output) is the only external difference. CDB5376 can be converted to use any combination of CS3301 and CS3302 amplifiers by replacing the amplifier device and properly setting the pin 13 jumper (J42, J242, J342, J442). By default these jumpers are not populated and have shorting traces between pins on the back side of the PCB. Converting between amplifier types requires *carefully* cutting the default short and installing a jumper.

Common amplifier configurations for CDB5376 include 3x or 4x CS3301 amplifiers for land applications, 4x CS3302 amplifiers for marine streamer applications, and 3x CS3301 amplifiers plus 1x CS3302 amplifier for seabed reservoir monitoring applications. Replacement amplifiers can be requested as samples from your local Cirrus Logic sales representative.

### 2.2.2.2 Rough-Fine Outputs - OUTR, OUTF

The analog outputs of the CS3301/02 differential amplifiers are split into rough-charge and fine-charge signals for input to the CS5372  $\Delta\Sigma$  modulators. The amplifier outputs include integrated series resistors to create the anti-alias RC filters required to limit the modulator input signal bandwidth.

Analog signal traces out of the CS3301/02 amplifiers and into the CS5372 modulators are 4-wire INR+ / INF+ / INF- / INR- quad groups, and are routed with INF+ and INF- as a traditional differential pair and INR+ and INR- as guard traces outside the respective INF+ and INF- traces.

### 2.2.2.3 Anti-alias RC Filters

The CS5372  $\Delta\Sigma$  modulator is 4th order and high-frequency input signals can cause instability. Simple single-pole anti-alias RC filters are required between the CS3301/02 amplifier outputs and the CS5372 modulator inputs to bandwidth limit analog signals into the modulator.

The CS3301/02 amplifier outputs include internal series resistors, so a differential anti-alias RC filter is created by connecting 20 nF of high-linearity differential capacitance (2x 10 nF C0G) between each half of the rough and fine signals. External 0-ohm resistors are included in series with the amplifier internal anti-alias resistors to support testing of other anti-alias RC filter configurations.

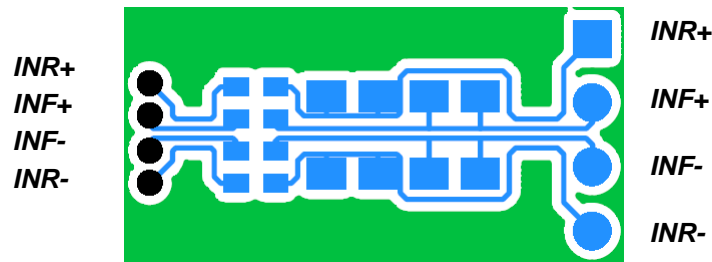


Figure 2. RC Filter External Components

### 2.2.3 Delta-Sigma Modulators

A single CS5372 dual modulator performs the A/D function for differential analog signals from two CS3301/02 amplifiers. The digital outputs are oversampled  $\Delta\Sigma$  bit streams.

| Analog Signals | Description                          |
|----------------|--------------------------------------|
| INR1, INF1     | Channel 1 analog rough / fine inputs |
| INR2, INF2     | Channel 2 analog rough / fine inputs |
| VREF           | Voltage reference analog inputs      |

| Digital Signals | Description                                       |
|-----------------|---|
| MDATA[1..2]     | Modulator delta-sigma data outputs                |
| MFLAG[1..2]     | Modulator over-range flag outputs                 |
| MCLK            | Modulator clock input                             |
| MSYNC           | Modulator synchronization input                   |
| PWDN[1..2]      | Power down mode enable                            |
| OFST            | Internal offset enable (+VD when using CS3301/02) |

#### 2.2.3.1 Rough-Fine Inputs - INR, INF

The modulator analog inputs are separated into rough and fine signals, each of which has an anti-alias RC filter to limit the signal bandwidth into the modulator inputs.

### 2.2.3.2 Offset Enable - OFST

The CS5372  $\Delta\Sigma$  modulator requires differential offset to be enabled to eliminate idle tones for a terminated input. The use of internal offset to eliminate idle tones is described in the CS5372 data sheet. OFST is enabled by closing dip switch #4 (S5, #4 - HI).

### 2.2.4 Delta-Sigma Test DAC

The CS4373A DAC creates differential analog signals for system tests. Multiple test modes are available and their use is described in the CS4373A data sheet.

| <b>Analog Signals</b> | <b>Description</b>                                  |
|-----------------------|---|
| OUT                   | Precision differential analog output                |
| BUF                   | Buffered differential analog output                 |
| CAP                   | Capacitor connection for internal anti-alias filter |
| VREF                  | Voltage reference analog inputs                     |

| <b>Digital Signals</b> | <b>Description</b>          |
|------------------------|-----------------------------|
| TDATA                  | Delta-sigma test data input |
| MCLK                   | Clock input                 |
| SYNC                   | Synchronization input       |
| MODE[0..2]             | Test mode selection         |
| ATT[0..2]              | Attenuation range selection |

#### 2.2.4.1 Precision Output - DAC\_OUT

The CS4373A test DAC has a precision output (DAC\_OUT) that is routed to the input selection jumpers for each channel. This output is sensitive to loading, and on CDB5376 should only be jumpered into the INB inputs which do not have passive RC filter components installed. The input impedance of the CS3301/02 INB amplifier inputs are high enough that the precision output can be directly connected to the INB inputs of all channels simultaneously.

#### 2.2.4.2 Buffered Output - DAC\_BUF

The CS4373A test DAC has a buffered output (DAC\_BUF) that is routed to the input selection jumpers for each channel. This output is less sensitive to loading than the precision outputs, and can be jumpered into either the INA or INB inputs without affecting performance. The buffered output can also drive a sensor attached to the input screw terminals, provided the sensor meets the impedance requirements specified in the CS4373A data sheet.

## 2.2.5 Voltage Reference

A voltage reference on CDB5376 creates a precision voltage from the regulated analog supplies for the modulator and test DAC VREF inputs. Because the voltage reference output is generated relative to the negative analog power supply, VREF+ is near GND potential for bipolar power supplies.

| Specification                       | Value                |
|-------------------------------------|----------------------|
| Precision Reference - Linear Tech   | LT1019AIS8-2.5       |
| Surface Mount Package Type          | SO-8                 |
| Output Voltage Tolerance            | +/- 0.05%            |
| Temperature Drift                   | 10 ppm / degC        |
| Quiescent Current                   | 0.65 mA              |
| Output Voltage Noise, 10 Hz - 1 kHz | 4 ppm <sub>RMS</sub> |
| Ripple Rejection, 10 Hz - 200 Hz    | > 100 dB             |

### 2.2.5.1 VREF\_MOD12, VREF\_MOD34, VREF\_DAC

The voltage reference output is provided to the CS5372  $\Delta\Sigma$  modulators and the CS4373A test DAC through separate low-pass RC filters. By separately filtering the voltage reference for each device, signal-dependent sampling of VREF by one device is isolated from other devices. Each voltage reference signal is routed as a separate differential pair from the large RC filter capacitor to control the sensitive VREF source-return currents and keep them out of the ground plane. In addition to the RC filter function, the 100  $\mu$ F filter capacitor provides a large charge well to help settle voltage reference sampling transients.

### 2.2.5.2 Common Mode Bias

A buffered version of the voltage reference is created as a low-impedance common mode bias source for the analog signal inputs. The bias resistors connected between the buffered voltage reference and each analog signal input half depends on the sensor type and should be modified to match the sensor manufacturer recommendations.

## 2.3 Digital Hardware

### 2.3.1 Digital Filter

The CS5376A quad digital filter performs filtering and decimation of four delta-sigma bit streams from the CS5372 modulators. It also creates a delta-sigma bit stream output to create analog test signals in the CS4373A test DAC.

The CS5376A requires several control signal inputs from the external system.

| <b>Control Signals</b> | <b>Description</b>                                  |
|------------------------|---|
| RESET <sub>z</sub>     | Reset input, active low                             |
| BOOT                   | Microcontroller / EEPROM boot mode select           |
| TIMEB                  | Time Break input, rising edge triggered             |
| CLK                    | Master clock input, 32.768 MHz                      |
| SYNC                   | Master synchronization input, rising edge triggered |

Configuration is completed through the SPI 1 port.

| <b>SPI1 Signals</b> | <b>Description</b>                            |
|---------------------|---|
| SS <sub>Iz</sub>    | Serial chip select input, active low          |
| SCK <sub>I</sub>    | Serial clock input                            |
| MISO                | Master in / slave out serial data             |
| MOSI                | Master out / slave in serial data             |
| SINT <sub>z</sub>   | Serial acknowledge output, active low         |
| SSO <sub>z</sub>    | Serial chip select output (unused on CDB5376) |

Data is collected through the SD port.

| <b>SD Port Signals</b> | <b>Description</b>                             |
|------------------------|--|
| SDTKI                  | Token input to initiate an SD port transaction |
| SDRDY <sub>z</sub>     | Data ready acknowledge, active low             |
| SDCLK                  | Serial clock input                             |
| SDDAT                  | Serial data output                             |
| SDTKO                  | Token output (unused on CDB5376)               |

Modulator  $\Delta\Sigma$  data is input through the modulator interface.

| <b>Modulator Signals</b> | <b>Description</b>                 |
|--------------------------|------------------------------------|
| MCLK                     | Modulator clock output             |
| MCLK/2                   | Modulator clock output, half-speed |
| MSYNC                    | Modulator synchronization output   |
| MDATA[1..4]              | Modulator delta-sigma data inputs  |
| MFLAG[1..4]              | Modulator over-range flag inputs   |

Test DAC  $\Delta\Sigma$  data is generated by the test bit stream generator.

| <b>Test Bit Stream Signals</b> | <b>Description</b>                        |
|--------------------------------|---|
| TBSDATA                        | Test DAC delta-sigma data output          |
| TBCLK                          | Test DAC clock output (unused on CDB5376) |

Amplifier, modulator, and test DAC digital pins are controlled by the GPIO port.

| <b>GPIO Signals</b>   | <b>Description</b>                     |
|-----------------------|--|
| GPIO[0..1]:MUX[0..1]  | Amplifier input mux selection          |
| GPIO[2..4]:GAIN[0..2] | Amplifier gain / test DAC attenuation  |
| GPIO[5..7]:MODE[0..2] | Test DAC mode selection                |
| GPIO[8]:PWDN          | Amplifier / modulator power down       |
| GPIO[9..10]           | Available general purpose input/output |
| GPIO[11]:EECS         | Chip select for boot EEPROM            |

The secondary serial port (SPI 2) and boundary scan JTAG port are unused on CDB5376.

| <b>SPI2 Signals</b> | <b>Description</b>                      |
|---------------------|---|
| SCK2                | Serial clock output (unused on CDB5376) |
| SO                  | Serial data output (unused on CDB5376)  |
| SI[1..4]            | Serial data inputs (unused on CDB5376)  |

| <b>JTAG Signals</b> | <b>Description</b>                        |
|---------------------|---|
| TRSTz               | JTAG reset (unused on CDB5376)            |
| TMS                 | JTAG test mode select (unused on CDB5376) |
| TCK                 | JTAG test clock input (unused on CDB5376) |
| TDI                 | JTAG test data input (unused on CDB5376)  |
| TDO                 | JTAG test data output (unused on CDB5376) |

### 2.3.1.1 MCLK Conversion to ACLK

The CS5376A digital filter creates the analog sampling clock used by the CS5372  $\Delta\Sigma$  modulators and CS4373A test DAC (MCLK). This clock has strict jitter requirements to guarantee the accuracy of analog-to-digital and digital-to-analog conversion, and so is carefully routed between the digital filter and modulators/test DAC.

The CS3301 amplifier also receives a version of the analog sampling clock (ACLK) to run the internal chopper stabilization circuitry, but without the strict jitter requirement since it is an analog-input/analog-output device. To isolate the sensitive modulator/test DAC analog sampling clock route from the long route of the amplifier clock, a 200  $\Omega$  series resistor connects the MCLK and ACLK traces together.

### 2.3.1.2 Configuration - SPI1 Port

Configuration of the CS5376A digital filter is through the SPI 1 port by the on-board 8051 microcontroller, which receives commands from the PC evaluation software via the USB interface. Evaluation software commands can write/read digital filter registers, specify digital filter coefficients and test bit stream data, and start/stop digital filter operation. Alternately, the digital filter can automatically load configuration information from an on-board serial EEPROM.

Configuration of the digital filter is selected by the BOOT signal from dip switch #1 (S5, #1). By default the BOOT signal is set low (S5, #1 - LO) to indicate configuration information is written by the microcontroller. If BOOT is set high (S5, #1 - HI), the digital filter attempts to automatically read configuration information from the serial EEPROM after reset. The serial EEPROM on CDB5376 is provided for custom programming convenience only and is not directly supported by the PC evaluation software or microcontroller firmware.

### 2.3.2 Interface CPLD

A Xilinx CPLD is included on CDB5376 (XCR3128XL-10VQ100I) as an interface between the CS5376A digital filter and the microcontroller. By default the CPLD only passes through the interface signals, but can be reprogrammed to disconnect the on-board 8051 microcontroller and connect to another external microcontroller through the spare dual-row headers. Control signals taken off the CDB5376 board to an external microcontroller should pair with a ground return wire to maintain signal integrity.

Free software tools and an inexpensive hardware programmer for the Xilinx CPLD are available from the internet (<http://www.xilinx.com>). The hardware programmer interfaces with the Xilinx JTAG programming port (J39) on CDB5376. Note that early versions of the Xilinx WebPack tools (7.1i SP1 and earlier) have a bug in the JEDEC programming file for the CPLD included on CDB5376, and WebPack version 7.1i SP2 or later is required.

Included below is the default Verilog HDL file used by CDB5376 inside the interface CPLD. Comparing the input and output definitions of this file with the CPLD schematic pinout should demonstrate how signals are selected and passed through from the microcontroller to the CS5376A digital filter. Several signal connections to the CPLD are not defined in the default HDL file, but are routed to the CPLD on CDB5376 for convenience during custom reprogramming.

```

////////////////////////////////////
// MODULE:    CDB5376 top module
//
// FILE NAME:  Top module for connecting CS5376 to C8051F320
// VERSION:    1.0
// DATE:       Jan. 18, 2006
// COPYRIGHT:  Cirrus Logic, Inc.
//
// CODE TYPE:  Register Transfer Level
//
// DESCRIPTION: This module includes assignments for signals between
//              the serial port of CS5376A and the SLAB micro.
//
////////////////////////////////////

module cdb5376 (
    sck_mc,
    mosi_mc,
    ssi_mc,
    sdtki_mc,
    timeb_mc,
    miso,
    drdy,
    sddat,
    sync_mc,
    sync_pb,
    timeb_pb,
    reset_pb,
    reset_ext,

    miso_mc,
    drdy_mc,
    sck,
    mosi,
    ssi,
    sdtki,
    timeb,
    sdclk,
    sync,
    reset );

////////////////////////////////////
// input signals
////////////////////////////////////

input sck_mc, mosi_mc, ssi_mc;
input sdtki_mc, timeb_mc;
input miso, drdy, sddat;
input sync_mc, sync_pb, timeb_pb;
input reset_pb, reset_ext;

////////////////////////////////////
//output signals
////////////////////////////////////

output miso_mc, drdy_mc;
output sck, mosi, ssi;
output sdtki, timeb, sdclk;
output sync, reset;

////////////////////////////////////
// signal assignments
////////////////////////////////////

assign sck = sck_mc;
assign sdclk = sck_mc;
assign mosi = mosi_mc;
assign ssi = ssi_mc;
assign sdtki = sdtki_mc;
assign drdy_mc = drdy;
assign miso_mc = (drdy)? miso:sddat;

assign timeb = timeb_mc | timeb_pb;
assign sync = sync_mc | sync_pb;
assign reset = reset_pb & reset_ext;

endmodule

```

**Figure 3. CPLD Default Signal Assignments**



### 2.3.3 Digital Control Signals

The reset, synchronization, and timebreak signals to the CS5376A digital filter can be generated by push buttons, received from external inputs or generated by the on-board microcontroller. By default, the push button RESET\_PB, SYNC\_PB, and TIMEB\_PB signals are connected through the interface CPLD to the CS5376A digital filter RESET, SYNC, and TIMEB inputs.

A four-position DIP switch on CDB5376 (S5) sets static digital control signals not normally changed during operation. The BOOT signal (S5, #1) controls how the CS5376A digital filter receives configuration data, either from a microcontroller or serial EEPROM. The LPWR signal (S5, #3) reduces the power consumption of the analog components at the expense of analog performance. The OFST signal (S5, #4) enables the internal offset within the CS5372 modulator device to eliminate  $\Delta\Sigma$  idle tones from a terminated input.

### 2.3.4 Microcontroller

Included on CDB5376 is an 8051-type microcontroller with integrated hardware SPI and USB interfaces. This C8051F320 microcontroller is a product of Silicon Laboratories (<http://www.silabs.com>). Key features of the C8051F320 microcontroller are:

- 8051 compatibility** - uses industry-standard 8051 software development tools
- In-circuit debugger** - software development on the target hardware
- Internal memory** - 16k flash ROM and 2k static RAM included on-chip
- Multiple serial connections** - SPI, USB, I2C, and UART
- High performance** - 25 MIPS maximum
- Low power** - 0.6 mA @ 1 MHz w/o USB, 9 mA @ 12 MHz with USB
- Small size** - 32 pin LQFP package, 9mm x 9mm
- Industrial temperature** - full performance (including USB) from -40 C to +85 C
- Internal temperature sensor** - with range violation interrupt capability
- Internal timers** - four general purpose plus one extended capability
- Power on reset** - can supply a reset signal to external devices
- Analog ADC** - 10 bit, 200 ksps SAR with internal voltage reference
- Analog comparators** - arbitrary high/low voltage compare with interrupt capability

The exact use of these features is controlled by embedded firmware.

C8051F320 has dedicated pins for power and the USB connection, plus 25 general-purpose I/O pins that connect to the various internal resources through a programmable crossbar. Hardware connections on CDB5376 limit how the blocks can operate, so the port mapping of microcontroller resources is detailed below.

| Pin # | Pin Name | Assignment | Description                                 |
|-------|----------|------------|---|
| 1     | P0.1     | SDTKI_MC   | Token to start CS5376A data transaction     |
| 2     | P0.0     | SYNC_IO    | SYNC signal from RS-485                     |
| 3     | GND      |            | Ground                                      |
| 4     | D+       |            | USB differential data transceiver           |
| 5     | D-       |            | USB differential data transceiver           |
| 6     | VDD      |            | +3.3 V power supply input                   |
| 7     | REGIN    |            | +5 V power supply input (unused on CDB5376) |
| 8     | VBUS     |            | USB voltage sense input                     |

| Pin # | Pin Name | Assignment | Description                       |
|-------|----------|------------|-----------------------------------|
| 9     | /RST     | RESETz     | Power on reset output, active low |
|       | C2CK     |            | Clock input for debug interface   |
| 10    | P3.0     | GPIO       | General purpose I/O               |
|       | C2D      |            | Data in/out for debug interface   |
| 11    | P2.7     | AIN-       | ADC input                         |
| 12    | P2.6     | AIN+       | ADC input                         |
| 13    | P2.5     | CPLD3_MC   | General Purpose I/O               |
| 14    | P2.4     | CPLD2_MC   | General Purpose I/O               |
| 15    | P2.3     | CPLD1_MC   | General Purpose I/O               |
| 16    | P2.2     | CPLD0_MC   | General Purpose I/O               |

| Pin # | Pin Name | Assignment | Description                        |
|-------|----------|------------|------------------------------------|
| 17    | P2.1     | TIMEB_MC   | Time Break signal to CS5376A       |
| 18    | P2.0     | SYNC_MC    | SYNC signal to CS5376A             |
| 19    | P1.7     | BYP_EN     | I2C bypass switch control          |
| 20    | P1.6     | SDA_DE     | I2C data driver enable             |
| 21    | P1.5     | SCL        | I2C clock in/out                   |
| 22    | P1.4     | SDA        | I2C data in/out                    |
| 23    | P1.3     | SSI_MCz    | SPI chip select output, active low |
| 24    | P1.2     | MOSI_MC    | SPI master out / slave in          |

| Pin # | Pin Name | Assignment | Assignment                                      |
|-------|----------|------------|---|
| 25    | P1.1     | MISO_MC    | SPI master in / slave out                       |
| 26    | P1.0     | SCK1_MC    | SPI serial clock                                |
| 27    | P0.7     |            | Internal VREF bypass capacitors                 |
| 28    | P0.6     | SINT_MCz   | Serial acknowledge from CS5376A, active low     |
| 29    | P0.5     | RX         | UART receiver                                   |
| 30    | P0.4     | TX         | UART transmitter                                |
| 31    | P0.3     | CLOCK_MC   | External clock input                            |
| 32    | P0.2     | SDRDY_MCz  | Data ready acknowledge from CS5376A, active low |

Many connections to the C8051F320 microcontroller are inactive by default, but are provided for convenience during custom reprogramming. Listed below are the default active connections to the microcontroller and how they are used.

#### **2.3.4.1 SPI Interface**

The microcontroller SPI interface communicates with the CS5376A digital filter to write/read configuration information from the SPI 1 port and collect conversion data from the SD port. Detailed information about interfacing to the digital filter SPI 1 and SD ports can be found in the CS5376A data sheet.

The hardware connection of the microcontroller MISO\_MC pin is selected automatically within the interface CPLD depending on the state of the digital filter SDRDYz pin. By default, SDRDYz is high and the CS5376A SPI 1 port MISO pin is connected to the microcontroller MISO\_MC pin, but when conversion data becomes available from the CS5376A SD port, SDRDYz goes low and the SDDAT pin is connected instead.

#### **2.3.4.2 USB Interface**

The microcontroller USB interface communicates with the PC evaluation software to receive configuration commands and return collected conversion data. The USB interface uses the Silicon Laboratories API and Windows drivers, which are available free from the internet (<http://www.silabs.com>).

#### **2.3.4.3 Reset Source**

By default, the C8051F320 microcontroller receives its reset signal from the RESET\_PBz push button.

#### **2.3.4.4 Clock Source**

By default, the C8051F320 microcontroller uses an internally generated 12 MHz clock for compatibility with USB standards.

#### **2.3.4.5 Timebreak Signal**

By default, the C8051F320 microcontroller sends the TIMEB\_MC signal to the digital filter for the first collected sample of a data record. Typically, some number of initial samples are skipped during data collection to ensure the CS5376A digital filters are fully settled, and the timebreak signal is automatically set for the first “real” collected sample.

#### **2.3.4.6 C2 Debug Interface**

Through the PC evaluation software, the microcontroller default firmware can be automatically flashed to the latest version without connecting an external programmer. To flash custom firmware, software tools and an inexpensive hardware programmer that connects to the C2 Debug Interface on CDB5376 is available for purchase from Silicon Laboratories (DEBUGADPTR1-USB).

### **2.3.5 Phase Locked Loop**

To make synchronous analog measurements throughout a distributed system, a synchronous system clock is required to be provided to each measurement node. For evaluation testing purposes, a BNC clock

input on CDB5376 can receive a lower-frequency system clock and create a synchronous higher-frequency clock using an on-board PLL.

| <b>Specification</b>              | <b>Value</b>   |
|-----------------------------------|--|
| Input Clock Frequency             | 1.024, 2.048, 4.096 MHz<br>8.192, 16.384, 32.768 MHz |
| Distributed Clock Synchronization | ± 240 ns   |
| Maximum Input Clock Jitter, RMS   | 1 ns   |
| <b>Specification</b>              | <b>Value</b>   |
| PLL Output Clock Frequency        | 32.768 MHz   |
| Maximum Output Jitter, RMS        | 300 ps   |
| Oscillator Type                   | VCXO   |
| Detector Architecture             | Phase / Frequency                                    |

The expected input clock frequency to the BNC clock input is set by the EXT\_CLK jumper (J16). If no external clock is supplied to CDB5376, the PLL will free-run at the nominal output frequency.

The PLL on CDB5376 uses a voltage-controlled crystal oscillator (VCXO) to minimize jitter, and has a single-gate phase/frequency detector and clock divider to minimize size and power.

| <b>Specification</b>                        | <b>Value</b>           |
|---|------------------------|
| Oscillator - Citizen 32.768 MHz VCXO        | CSX750VBEL32.768MTR    |
| Surface Mount Package Type                  | Leadless 6-Pin, 5x7 mm |
| Supply Voltage, Current                     | 3.3 V, 11 mA           |
| Frequency Stability, Pullability            | ± 50 ppm, ± 90 ppm     |
| Startup Time                                | 4 ms                   |
| <b>Specification</b>                        | <b>Value</b>           |
| Phase Detector - TI LittleLogic XOR         | SN74LVC1G86DBVR        |
| Surface Mount Package Type                  | SOT23-5                |
| Supply Voltage, Current                     | 3.3 V, 10 µA           |
| <b>Specification</b>                        | <b>Value</b>           |
| Loop Filter Integrator - Linear Tech Op-Amp | LT1783IS5              |
| Surface Mount Package Type                  | SOT23-5                |
| Supply Voltage, Current                     | 3.3 V, 375 µA          |
| <b>Specification</b>                        | <b>Value</b>           |
| Clock Divider - TI LittleLogic D-Flop       | SN74LVC2G74DCTR        |
| Surface Mount Package Type                  | SSOP8-199              |
| Supply Voltage, Current                     | 3.3 V, 10 µA           |

### 2.3.6 RS-485 Telemetry

By default, CDB5376 communicates with the PC evaluation software through the microcontroller USB port. Additional hardware is designed onto CDB5376 to use the microcontroller I2C port as a low-level local telemetry, but it is provided for custom programming convenience only and is not directly supported by the CDB5376 PC evaluation software or microcontroller firmware.

Telemetry signals enter CDB5376 through RS-485 transceivers, which are differential current mode transceivers that can reliably drive long distance communication. Data passes through the RS-485 transceivers to the microcontroller I2C interface and the clock and synchronization inputs.

| <b>Specification</b>                                  | <b>Value</b>            |
|---|-------------------------|
| RS-485 Transceiver - Linear Tech                      | LTC1480IS8              |
| Surface Mount Package Type                            | SOIC-8, 5mm x 6mm       |
| Supply Voltage, Quiescent Current                     | 3.3V, 600 $\mu$ A       |
| Maximum Data Rate                                     | 2.5 Mbps                |
| Transmitter Delay, Receiver Delay                     | 25 - 80 ns, 30 - 200 ns |
| Transmitter Current, Full Termination (60 $\Omega$ )  | 25 mA                   |
| Transmitter Current, Half Termination (120 $\Omega$ ) | 13 mA                   |

#### 2.3.6.1 CLK, SYNC

Clock and synchronization telemetry signals into CDB5376 are received through RS-485 twisted pairs. These signals are required to be distributed through the external system with minimal jitter and timing skew, and so are normally driven through high-speed bus connections.

| <b>Specification</b>             | <b>Value</b>           |
|----------------------------------|------------------------|
| Synchronous Inputs, 2 wires each | CLK $\pm$ , SYNC $\pm$ |

| <b>Specification</b>                     | <b>Value</b> |
|--|--------------|
| Distributed SYNC Signal Synchronization  | $\pm$ 240 ns |
| Distributed Clock Synchronization        | $\pm$ 240 ns |
| Analog Sampling Synchronization Accuracy | $\pm$ 480 ns |

Synchronization of the measurement channel is critical to ensure simultaneous analog sampling across a network. Several options are available for connecting a SYNC signal through the RS-485 telemetry to the digital filter.

A direct connection is made when the SYNC\_IO signal is received over the dedicated RS-485 twisted pair and sent directly to the digital filter SYNC pin through jumper J56. The incoming SYNC\_IO signal must be synchronized to the network at the transmitter since no local timing adjustment is available.

A microcontroller hardware connection is made when the SYNC\_IO signal is received over the dedicated RS-485 twisted pair and detected by a microcontroller interrupt. The microcontroller can then use an internal counter to re-time the SYNC\_MC signal output to the digital filter SYNC input as required.

A microcontroller software connection is made when the SYNC\_MC signal output is created by the microcontroller on command from the system telemetry. The microcontroller can use an internal counter to re-time the SYNC\_MC signal output to the digital filter SYNC input as required.

### 2.3.6.2 I<sup>2</sup>C - SCL, SDA, Bypass

The I2C<sup>®</sup> telemetry connections to CDB5376 transmit and receive through RS-485 twisted pairs. Because signals passing through the transceivers are actively buffered, full I2C bus arbitration and error detection cannot be used (i.e. high-impedance NACK).

The I2C inputs and outputs can be externally wired to create either a daisy chain or a bus-type network, depending how the telemetry system is to be implemented. Analog switches included on CDB5376 can bypass the I2C signals to create a bus network from a daisy chain network following address assignment.

| <b>Specification</b>      | <b>Value</b>                                |
|---------------------------|---|
| I2C Inputs, 2 wires each  | SCL <sub>±</sub> , SDA <sub>±</sub>         |
| I2C Outputs, 2 wires each | BYP_SCL <sub>±</sub> , BYP_SDA <sub>±</sub> |
| I2C Bypass Switch Control | BYP_EN                                      |

When CDB5376 is used in a distributed measurement network, each node must have a unique address. This address is used to transmit individual configuration commands and tag the source of returned conversion data. Address assignment can be either dynamic or static, depending how the telemetry system is to be implemented.

Dynamic address assignment uses daisy-chained I2C connections to assign an address to each measurement node. Once a node receives an address, it enables the I2C bypass switches to the next node so it can be assigned an address.

Static address assignment has a serial number assigned to each node during manufacturing. When placed in the network, the location is recorded and a master list of serial numbers vs. location is maintained. Alternately, a location-dependent serial number can be assigned during installation.

### 2.3.7 UART Connection

A UART connection on CRD5376 provides a low-speed standardized connection for telemetry solutions not using I2C. UART connections are provided for custom programming convenience only and are not directly supported by the CDB5376 PC evaluation software or microcontroller firmware.

| <b>Specification</b>           | <b>Value</b>   |
|--------------------------------|----------------|
| UART Connections, 2 wires each | TX/GND, RX/GND |

### 2.3.8 External Connector

Power supplies and telemetry signals route to a 20-pin double row connector with 0.1" spacing (J26). This header provides a compact standardized connection to the CDB5376 external signals.

| Pins   | Name               | Signal                |
|--------|--------------------|-----------------------|
| 1, 2   | CLK+, CLK-         | Clock Input           |
| 3, 4   | SYNC+, SYNC-       | Synchronization Input |
| 5, 6   | SCL+, SCL-         | I2C Clock             |
| 7, 8   | SDA+, SDA-         | I2C Data              |
| 9, 10  | BYP_SDA+, BYP_SDA- | I2C Data Bypass       |
| 11, 12 | BYP_SCL+, BYP_SCL- | I2C Clock Bypass      |
| 13, 14 | TX, GND            | UART transmit         |
| 15, 16 | RX, GND            | UART receive          |
| 17, 18 | EXT_VA-, GND       | Negative Power Supply |
| 19, 20 | EXT_VA+, GND       | Positive Power Supply |

## 2.4 Power Supplies

Power is supplied to CDB5376 through banana jacks (J6, J7, J8, J9) or through the external connector (J26). The banana jacks make separate connections to the EXT\_VA-, EXT\_VA+, GND, and EXT\_VD power supply nets, which connect to the analog and digital linear voltage regulator inputs. The external connector makes separate connections only to the EXT\_VA-, GND, and EXT\_VA+ power supply inputs and it is required to jumper EXT\_VA+ to EXT\_VD when powering CDB5376 from the external connector.

The EXT\_VA-, EXT\_VA+ and EXT\_VD power supply inputs have zener protection diodes that limit the maximum input voltages to +13 V or -13 V with respect to ground. Each input also has 100 uF bulk capacitance for bypassing and to help settle transients and another 0.01 uF capacitor to bypass high-frequency noise.

### 2.4.1 Analog Voltage Regulators

Linear voltage regulators create the positive and negative analog power supply voltages to the analog components on CDB5376. These regulate the EXT\_VA+ and EXT\_VA- power supply inputs to create the VA+ and VA- analog power supplies.

| Specification                                | Value                     |
|--|---------------------------|
| Positive Analog Power Supply                 | +2.5 V, +5 V              |
| Low Noise Micropower Regulator - Linear Tech | LT1763CS8                 |
| Surface Mount Package Type                   | SO-8                      |
| Load Regulation, -40 C to +85 C              | +/- 25 mV                 |
| Quiescent Current, Current @ 100 mA Load     | 40 $\mu$ A, 2 mA          |
| Output Voltage Noise, 10 Hz - 100 kHz        | 20 $\mu$ V <sub>RMS</sub> |
| Ripple Rejection, DC - 200 Hz                | > 50 dB                   |



| <b>Specification</b>                         | <b>Value</b>              |
|--|---------------------------|
| Negative Analog Supply, -2.5VA               | -2.5 V                    |
| Low Noise Micropower Regulator - Linear Tech | LT1964ES5-BYP             |
| Surface Mount Package Type                   | SOT-23                    |
| Load Regulation, -40 C to +85 C              | +/- 30 mV                 |
| Quiescent Current, Current @ 100 mA Load     | 30 $\mu$ A, 1.3 mA        |
| Output Voltage Noise, 10 Hz - 100 kHz        | 20 $\mu$ V <sub>RMS</sub> |
| Ripple Rejection, DC - 200 Hz                | > 45 dB                   |

The VA+ and VA- power supplies to the analog components on CDB5376 can be jumpered to use regulated bipolar power supplies (+2.5 V, -2.5 V), regulated unipolar power supplies (+5 V, GND), or unregulated direct connections (EXT\_VA+, EXT\_VA-). When using direct connections to EXT\_VA+ and EXT\_VA-, extreme care must be taken not to exceed the maximum specified power supply voltages of the analog components on CDB5376.

Characterization testing has shown the analog components on CDB5376 work best using bipolar analog power supplies (+2.5 V, -2.5 V) instead of unipolar analog power supplies (+5 V, GND). It is recommended to always use the regulated bipolar analog power supplies for optimal performance.

The VA+ and VA- power supply nets to the analog components on CDB5376 include reverse-biased Schottkey diodes to ground to protect against reverse voltages that could latch-up the CMOS analog components. Also included on VA+ and VA- are 100 uF bulk capacitors for bypassing and to help settle transients plus individual 0.1 uF bypass capacitors local to the analog power supply pins of each device.

### **2.4.2 Digital Voltage Regulators**

Linear voltage regulators create the positive digital power supply voltages on CDB5376. Jumper options select which external power supply input voltage, EXT\_VD or EXT\_VA+, is supplied to the digital voltage regulators to create the VD and V<sub>CORE</sub> power supplies.

| <b>Specification</b>                         | <b>Value</b>              |
|--|---------------------------|
| Positive Digital Power Supply                | +2.5 V, +3.3 V            |
| Low Noise Micropower Regulator - Linear Tech | LT1763CS8                 |
| Surface Mount Package Type                   | SO-8                      |
| Load Regulation, -40 C to +85 C              | +/- 25 mV                 |
| Quiescent Current, Current @ 100 mA Load     | 40 $\mu$ A, 2 mA          |
| Output Voltage Noise, 10 Hz - 100 kHz        | 20 $\mu$ V <sub>RMS</sub> |
| Ripple Rejection, DC - 200 Hz                | > 50 dB                   |

The VD and V<sub>CORE</sub> power supplies on CDB5376 can be jumpered to use regulated +3.3 V or +2.5 V power supplies or an unregulated direct connection to EXT\_VD. Extreme care must be taken when using a direct connection to EXT\_VD not to exceed the maximum specified power supply voltages of the digital components on CDB5376. Even though the Cirrus Logic components on CDB5376 will tolerate up to 5 V from the direct EXT\_VD power supply, other components are specified for +3.3 V operation only and so



it is recommended to use only the regulated +3.3 V jumper setting for VD. Characterization testing has shown the VCORE power supply to the digital filter device requires +3 V or higher to operate at the maximum 16.384 MHz internal clock rate, so it is recommended to always use the regulated +3.3 V jumper setting for VCORE.

The VD and VCORE power supplies on CDB5376 include reverse-biased Schottky diodes to ground to protect against reverse voltages that could latch-up the CMOS components. Also included on VD and VCORE are 100 uF bulk capacitors for bypassing and to help settle transients plus individual 0.1 uF bypass capacitors local to the digital power supply pins of each device.

## 2.5 PCB Layout

### 2.5.1 Layer Stack

**CDB5376 layers 1 and 2** are dedicated as analog routing layers. All critical analog signal routes are on these two layers. Some CPLD and microcontroller digital routes are also included on these layers away from the analog signal routes.

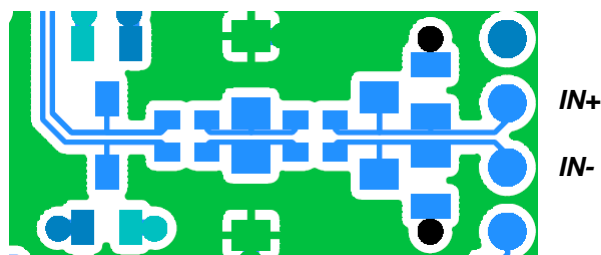
**CDB5376 layer 3** is dedicated for power supply routing. Each power supply net includes at least 100  $\mu$ F bulk capacitance as a charge well for settling transient current loads.

**CDB5376 layer 4** is a solid ground plane without splits or routing. A solid ground plane provides the best return path for bypassed noise to leave the system. No separate analog ground is required since analog signals on CDB5376 are differentially routed.

**CDB5376 layers 5 and 6** are dedicated as digital routing layers.

### 2.5.2 Differential Pairs

Analog signal routes on CDB5376 are differential with dedicated + and - traces. All source and return analog signal currents are constrained to the differential pair route and do not return through the ground plane. Differential traces are routed together with a minimal gap between them so that noise events affect them equally and are rejected as common mode noise.



**Figure 4. Differential Pair Routing**

Analog signal connections into the CS3301/02 amplifiers are 2-wire IN+ and IN- differential pairs, and are routed as such. Analog signal connections out of the CS3301/02 amplifiers and into the CS5372 modu-

lators are 4-wire INR+, INF+, INF-, INR- quad groups, and are routed with INF+ and INF- as a traditional differential pair and INR+ and INR- as guard traces outside the respective INF+ and INF- traces.

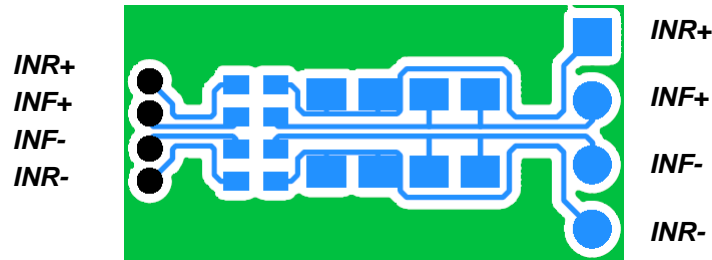


Figure 5. Quad Group Routing

### 2.5.3 Bypass Capacitors

Each device power supply pin includes 0.1  $\mu\text{F}$  bypass capacitors placed as close as possible to the pin on the back side of the PCB. Each power supply net includes at least 100  $\mu\text{F}$  bulk capacitance as a charge well for transient current loads.

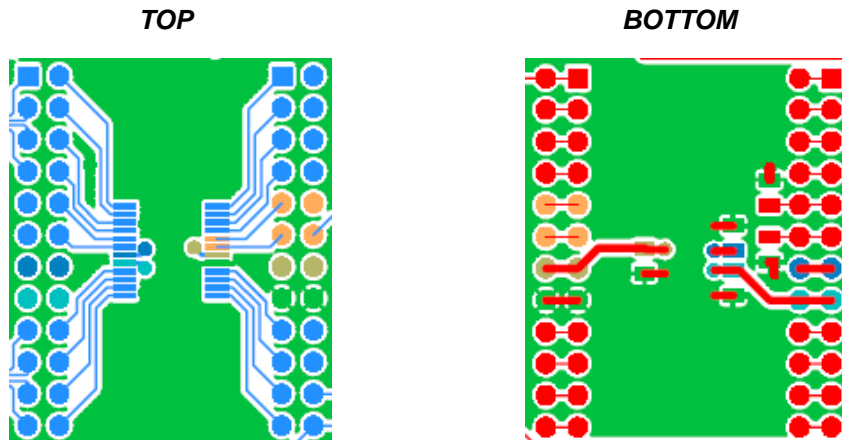
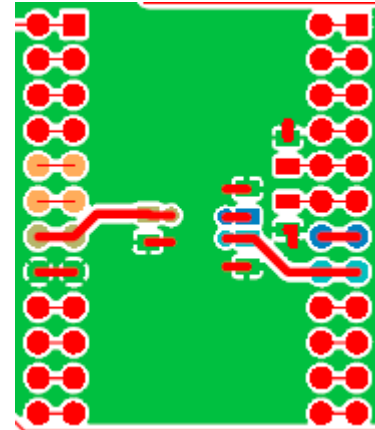
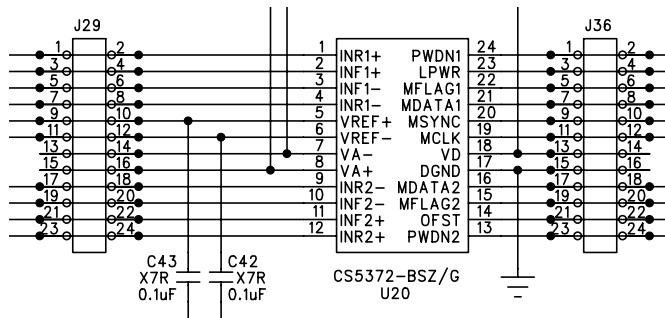


Figure 6. Bypass Capacitor Placement

### 2.5.4 Dual Row Headers

To simplify signal tracing on CDB5376, all device pins connect to dual-row headers. These dual-row headers are not populated during board manufacture, but the empty PCB footprint exists on the boards and can be used as test points.



**Figure 7. Dual-row Headers with Shorts**

The dual-row header pins are shorted on the bottom side of the PCB to pass signals through to the rest of the board. These shorted traces between the dual-row pins can be carefully cut to isolate the device signals from the rest of the PCB to permit wiring changes to the existing route. To restore the previous connection, install a jumper to short across the dual-row pins.

Signals taken off the PCB should not be wired directly from the dual-row header pins, as there is no clean path for the signal return current. Instead, install a connector into the prototyping area and wire the signal and a ground connection to it. Pairing the signal with a ground return before taking it off the PCB will improve signal integrity.

### 3. SOFTWARE DESCRIPTION

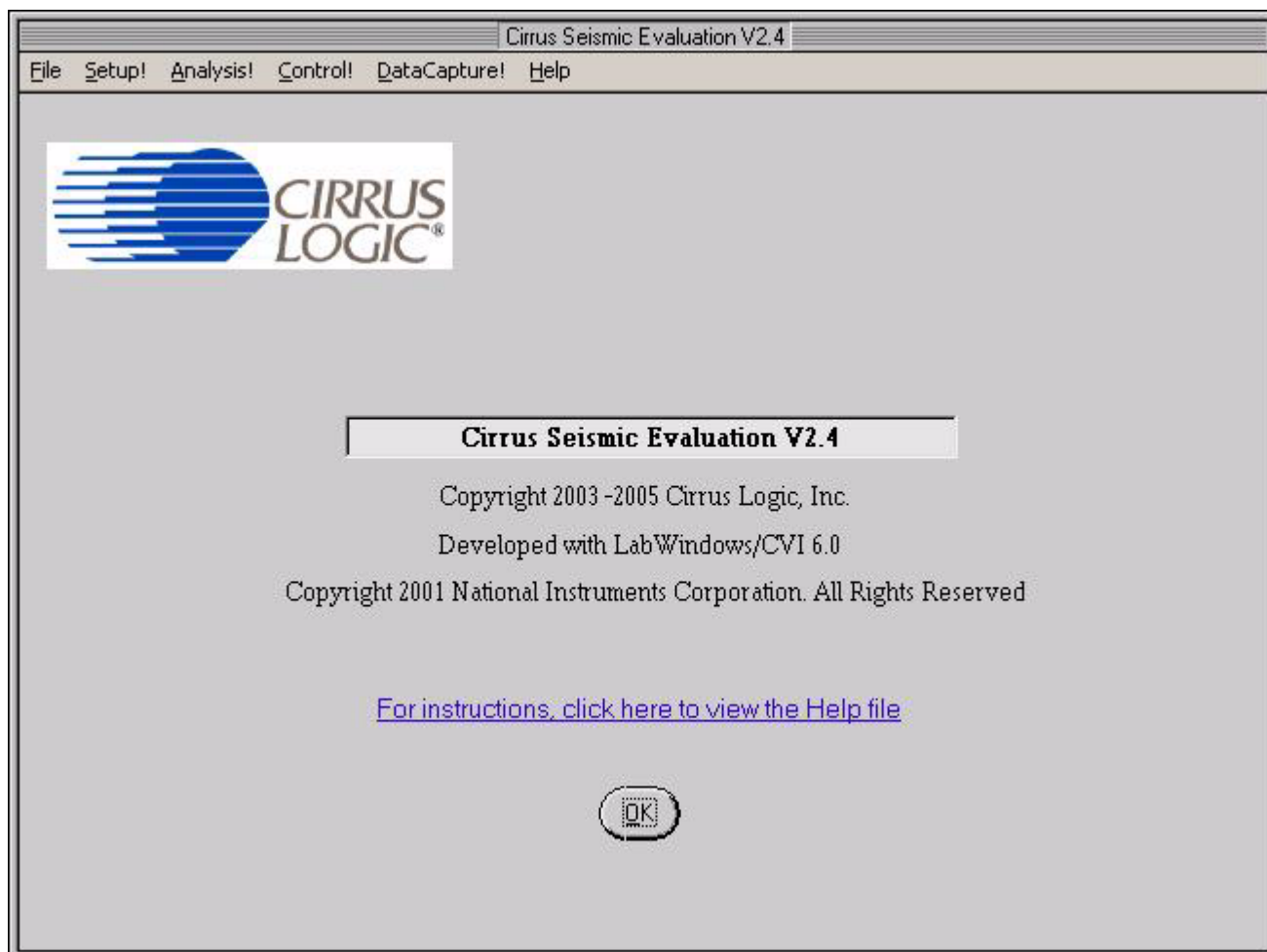
#### 3.1 Menu Bar



The menu bar is always present at the top of the software panels and provides typical *File* and *Help* pull-down menus. The menu bar also selects the currently displayed panel.

| Control                         | Description  |
|---------------------------------|--|
| <b>File</b>                     |  |
| <b>Load Data Set</b>            | Loads a data set from disk.                                  |
| <b>Save Data Set</b>            | Saves the current data set to disk.                          |
| <b>Copy Panel to Clipboard</b>  | Copies a bitmap of the current panel to the clipboard.       |
| <b>Print Analysis Screen</b>    | Prints the full Analysis panel, including statistics fields. |
| <b>Print Analysis Graph</b>     | Prints only the graph from the Analysis panel.               |
| <b>High Resolution Printing</b> | Prints using the higher resolution of the printer.           |
| <b>Low Resolution Printing</b>  | Prints using the standard resolution of the screen.          |
| <b>Quit</b>                     | Exits the application software.                              |
| <b>Setup!</b>                   |  |
|                                 | Displays the Setup Panel.                                    |
| <b>Analysis!</b>                |  |
|                                 | Displays the Analysis Panel.                                 |
| <b>Control!</b>                 |  |
|                                 | Displays the Control Panel.                                  |
| <b>DataCapture!</b>             |  |
|                                 | Displays the Setup Panel and starts Data Capture.            |
| <b>Help</b>                     |  |
| <b>Contents</b>                 | Find help by topic.  |
| <b>Search for help on</b>       | Find help by keywords.                                       |
| <b>About</b>                    | Displays the About Panel.                                    |

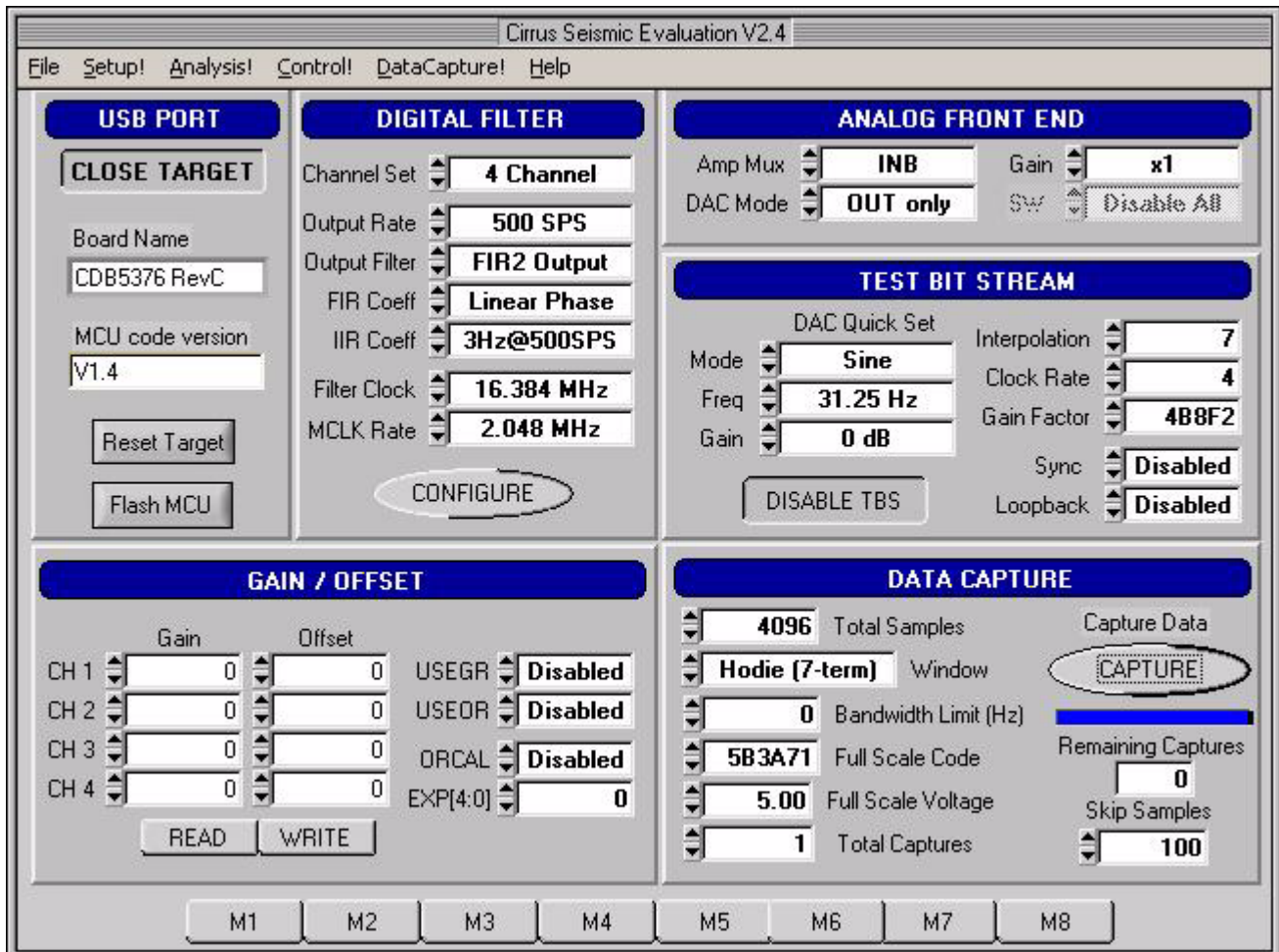
### 3.2 About Panel



The **About** panel displays copyright information for the Cirrus Seismic Evaluation software.

Click **OK** to exit this panel. Select **Help** ⇒ **About** from the menu bar to display this panel.

### 3.3 Setup Panel



The **Setup** panel initializes the evaluation system to perform data acquisition. It consists of the following sub-panels and controls.

- **USB Port**
- **Digital Filter**
- **Analog Front End**
- **Test Bit Stream**
- **Gain/Offset**
- **Data Capture**
- **External Macros**

### 3.3.1 USB Port

The **USB Port** sub-panel sets up the USB communication interface between the PC and the target board.

| Control                 | Description   |
|-------------------------|---|
| <b>Open Target</b>      | Open USB communication to the target board and read the board name and microcontroller firmware version. When communication is established, the name of this control changes to 'Close Target' and <b>Setup, Analysis</b> and <b>Control</b> panel access becomes available in the menu bar.  |
| <b>Close Target</b>     | Disconnects the previously established USB connection. On disconnection, this control changes to 'Open Target' and the <b>Setup, Analysis</b> and <b>Control</b> panel access becomes unavailable in the menu bar. The evaluation software constantly monitors the USB connection status and automatically disconnects if the target board is turned off or the USB cable is unplugged. |
| <b>Board Name</b>       | Displays the type of target board currently connected.  |
| <b>MCU code version</b> | Displays the version number of the microcontroller code on the connected target board.  |
| <b>Reset Target</b>     | Sends a software reset command to the target board.   |
| <b>Flash MCU</b>        | Programs the microcontroller code on the target board using the .thx file found in the "C:\Program Files\Cirrus Seismic Evaluation" directory. This feature permits reprogramming of the microcontroller (without using a hardware programmer) when a new version of the MCU code becomes available.  |

### 3.3.2 Digital Filter

The **Digital Filter** sub-panel sets up the digital filter configuration options.

By default the **Digital Filter** sub-panel configures the system to use on-chip coefficients and test bit stream data. The on-chip data can be overwritten by loading custom coefficients and test bit stream data from the **Customize** sub-panel on the **Control** panel.

Any changes made under this sub-panel will not be applied to the target board until the **Configure** button is pushed. The **Configure** button writes the new configuration to the target board and then enables the data **Capture** button.

| Control              | Description  |
|----------------------|--|
| <b>Channel Set</b>   | Selects the number of channels that are enabled in the digital filter. For the CS5376A digital filter, from 1 to 4 channels can be enabled.  |
| <b>Output Rate</b>   | Selects the output word rate of the digital filter. Output word rates from 4000 SPS to 1 SPS (0.25 mS to 1 S) are available.   |
| <b>Output Filter</b> | Selects the output filter stage from the digital filter. Sinc output, FIR1 output, FIR2 output, IIR 1st order output, IIR 2nd order output, or IIR 3rd order output can be selected. FIR2 output provides full decimation of the modulator data. |
| <b>FIR Coeff</b>     | Selects the on-chip FIR coefficient set to use in the digital filter. Linear phase or minimum phase FIR coefficients can be selected.  |
| <b>IIR Coeff</b>     | Selects the on-chip IIR coefficient set to use in the digital filter. Coefficient sets producing a 3 Hz high-pass corner at 2000 SPS, 1000 SPS, 500 SPS, 333 SPS, and 250 SPS can be selected.   |
| <b>Filter Clock</b>  | Sets the digital filter internal clock rate. Lower internal clock rates can save power when using slow output word rates.  |
| <b>MCLK Rate</b>     | Sets the analog sample clock rate. The CS5372 modulators and CS4373A test DAC typically run with MCLK set to 2.048 MHz.  |
| <b>Configure</b>     | Writes all information from the <b>Setup</b> panel to the digital filter. The data <b>Capture</b> button becomes available once the configuration information is written to the target board.  |



### 3.3.3 Analog Front End

The **Analog Front End** sub-panel configures the amplifier, modulator, and test DAC pin options. Pin options are controlled through the GPIO outputs of the digital filter.

Any changes made under this sub-panel will not be applied to the target board until the *Configure* button is pushed. The *Configure* button writes the new configuration to the target board and then enables the data *Capture* button.

| Control         | Description  |
|-----------------|--|
| <b>Amp Mux</b>  | Selects the input source for the CS3301/02 amplifiers. An internal termination, external INA inputs or external INB inputs can be selected.  |
| <b>DAC Mode</b> | Selects the operational mode of the CS4373A test DAC. The test DAC operational modes are AC dual output (OUT&BUF), AC precision output (OUT only), AC buffered output (BUF only), DC common mode output (DC Common), DC differential output (DC Diff), or AC common mode output (AC Common). The test DAC can also be powered down (PWDN) when not in use to save power. |
| <b>Gain</b>     | Sets the amplifier gain range and test DAC attenuation. Amplifier gain and DAC attenuation settings of 1x, 2x, 4x, 8x, 16x, 32x, or 64x can be selected and are controlled together.   |
| <b>Sw</b>       | Disabled for CDB5376.  |

### 3.3.4 Test Bit Stream

The **Test Bit Stream** sub-panel configures test bit stream (TBS) generator parameters. The digital filter data sheet describes TBS operation and options.

The *DAC Quick Set* controls automatically set the *Interpolation*, *Clock Rate*, and *Gain Factor* controls based on the selected *Mode*, *Freq*, and *Gain*. Additional configurations can be programmed by writing the *Interpolation*, *Clock Rate*, and *Gain Factor* controls manually.

Any changes made under this sub-panel will not be applied to the target board until the *Configure* button is pushed. The *Configure* button writes the new configuration to the target board and then enables the data *Capture* button.

| Control              | Description  |
|----------------------|--|
| <b>DAC Quick Set</b> | Automatically sets test bit stream options. <i>Mode</i> selects sine or impulse output mode, <i>Freq</i> selects the test signal frequency for sine mode, and <i>Gain</i> selects the test signal amplitude in dB. |
| <b>Interpolation</b> | Manual control for the data interpolation factor of the test bit stream generator.   |
| <b>Clock Rate</b>    | Manual control for the output clock and data rate of the test bit stream generator.  |
| <b>Gain Factor</b>   | Manual control to set the test bit stream signal amplitude.  |
| <b>Sync</b>          | Enables test bit stream synchronization by the MSYNC signal.   |
| <b>Loopback</b>      | Enables digital loopback from the test bit stream generator output to the digital filter input.  |

### 3.3.5 Gain/Offset

The **Gain / Offset** sub-panel controls the digital filter GAIN and OFFSET registers for each channel.

The OFFSET and GAIN registers can be manually written with any 24-bit 2's complement value from 0x800000 to 0x7FFFFFFF. The USEGR, USEOR, ORCAL, and EXP[4:0] values enable gain correction, offset correction, and offset calibration in the digital filter.

The offset calibration routine built into the digital filter is enabled by writing the ORCAL and EXP[4:0] bits. The EXP[4:0] value can range from 0x00 to 0x18 and represents an exponential shift of the calibration feedback, as described in the digital filter data sheet. Offset calibration results are automatically written to the OFFSET registers and remain there, even after offset calibration is disabled.

| Control         | Description  |
|-----------------|--|
| <b>Gain</b>     | Displays the digital filter GAIN1 to GAIN4 registers.  |
| <b>Offset</b>   | Displays the digital filter OFFSET1 to OFFSET4 registers.  |
| <b>Read</b>     | Reads values from the GAIN and OFFSET registers.   |
| <b>Write</b>    | Writes values to the GAIN and OFFSET registers.  |
| <b>USEGR</b>    | Enables gain correction. When enabled, output samples are gained down by the value in the GAIN register. (Output = GAIN / 0x7FFFFFFF).                           |
| <b>USEOR</b>    | Enables offset correction. When enabled, output samples are offset by the value in the OFFSET register. (Output = Sample - OFFSET).                              |
| <b>ORCAL</b>    | Enables offset calibration using the exponent value from the EXP[4:0] control. Results are automatically written to the OFFSET registers as they are calculated. |
| <b>EXP[4:0]</b> | Sets the exponential value used by offset calibration.   |

### 3.3.6 Data Capture

The **Data Capture** sub-panel collects samples from the target board and sets analysis parameters.

When the *Capture* button is pressed, the requested number of samples are collected from the target board through the USB port and are split among the enabled channels. A four-channel system, for example, will collect (Total Samples / 4) samples per channel. The maximum number of samples that can be collected is 1,048,576 (1M). The number of samples per channel should be a power of two for the analysis FFT routines to work properly.

After data is collected, analysis is performed using the selected parameters and the results are displayed on the **Analysis** panel. The selected analysis *window*, *bandwidth limit*, *full scale code*, and *full scale voltage* parameters can be modified for the data set currently in memory and the analysis re-run by pressing the *REFRESH* button on the **Analysis** Panel.

| Control                     | Description   |
|-----------------------------|---|
| <b>Total Samples</b>        | Sets the total number of samples to be collected. Multichannel acquisitions split the requested number of samples among the channels. A maximum of 1,048,576 (1M) samples can be collected. |
| <b>Window</b>               | Selects the type of analysis windowing function to be applied to the collected data set. Used to ensure proper analysis of discontinuous data sets.   |
| <b>Bandwidth Limit (Hz)</b> | Sets the frequency range over which to perform analysis, used to exclude higher-frequency components. Default value of zero performs analysis for the full Nyquist frequency range.         |
| <b>Full Scale Code</b>      | Defines the maximum positive full-scale 24-bit code from the digital filter. Used during FFT noise analysis to set the 0 dB reference level.  |
| <b>Full Scale Voltage</b>   | Defines the maximum peak-to-peak input voltage for the nV/rtHz Spot Noise analysis.   |
| <b>Total Captures</b>       | Sets the number of data sets to be collected and averaged together in the FFT magnitude domain. The maximum number of data sets that can be averaged is 100.                                |
| <b>Capture</b>              | Starts data collection from the target board through the USB port. After data collection, analysis is run using parameters from this sub-panel.   |
| <b>Remaining Captures</b>   | Indicates how many more data captures are remaining to complete the requested number of <i>Total Captures</i> . A zero value means that the current data capture is the last one.           |
| <b>Skip Samples</b>         | Sets the total number of samples to be skipped prior to data collection. A maximum of 64K samples can be skipped  |

### 3.3.7 External Macros

Macros are generated within the **Macros** sub-panel on the **Control** panel. Once a macro has been built it can either be saved with a unique macro name to be run within the **Macros** sub-panel, or saved as an external macro and be associated with one of the *External Macro* buttons.

A macro is saved as an *External Macro* by saving it in the `./macros/` subdirectory using the name `'m1.mac'`, `'m2.mac'`, etc. Depending on the selected name the macro will be associated with the corresponding *External Macro* button *M1*, *M2*, etc.

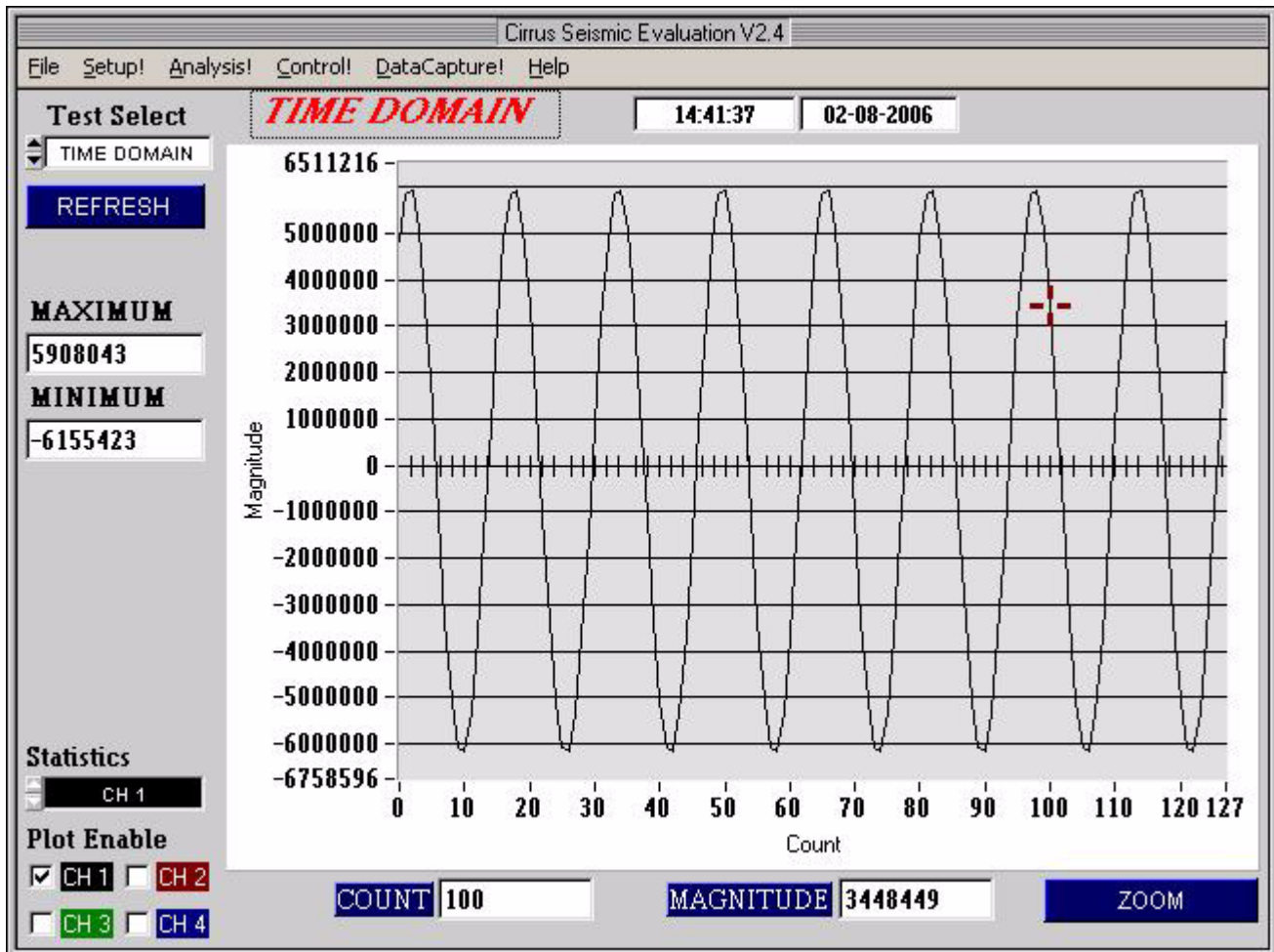
- M1 = `./macros/m1.mac`
- M2 = `./macros/m2.mac`
- etc.

*External Macro* buttons can be re-named on the panel by right clicking on them. The button name will change, but the macro associated with that button is always saved as `'m1.mac'`, `'m2.mac'`, etc., in the `./macros/` subdirectory. The *External Macro* button names are stored in the file `'Mnames.txt'`, also in the `./macros/` subdirectory.

*External Macros* allow up to eight macros to be accessed quickly without having to load them into the **Macros** sub-panel on the **Control** panel. These *External Macros* operate independently of the **Macros** sub-panel and are not affected by operations within it, except when a macro is saved to the `./macros/` subdirectory to replace a currently existing *External Macro*.

| Control        | Description   |
|----------------|---|
| <b>M1 - M8</b> | Runs the <i>External Macro</i> associated with that button. |

### 3.4 Analysis Panel



The **Analysis** panel is used to display the analysis results on collected data. It consists of the following controls.

- **Test Select**
- **Statistics**
- **Plot Enable**
- **Cursor**
- **Zoom**
- **Refresh**
- **Harmonics**
- **Spot Noise**
- **Plot Error**

### 3.4.1 Test Select

The *Test Select* control sets the type of analysis to be run on the collected data set.

| Control            | Description   |
|--------------------|---|
| <i>Time Domain</i> | Runs a min / max calculation on the collected data set and then plots sample data value vs. sample number.  |
| <i>Histogram</i>   | Runs a histogram calculation on the collected data set and then plots sample occurrence vs. sample value. Only valid for noise data since sine wave data varies over too many codes to plot as a histogram. |
| <i>Signal FFT</i>  | Runs an FFT on the collected data set and then plots frequency magnitude vs. frequency. Statistics are calculated using the largest frequency bin as a full-scale signal reference.                         |
| <i>Noise FFT</i>   | Runs an FFT on the collected data set and then plots frequency magnitude vs. frequency. Statistics are calculated using a simulated full-scale signal as a full-scale signal reference.                     |
| <i>Phase</i>       | Runs an FFT on the collected data set and then plots phase vs. frequency. Limited usefulness for real collected data since noise has random phase.  |

### 3.4.2 Statistics

The *Statistics* control displays calculated statistics for the selected analysis channel. For multichannel data captures, only one channel of calculated statistics are displayed at a time and is selected using the *Statistics* channel control.

Errors that affect statistical calculations will cause the *Plot Error* control to appear. Information about errors on specific channels can be accessed by enabling the plot of the channel using the *Plot Enable* control and then accessing the *Plot Error* controls.

| Control              | Description  |
|----------------------|--|
| <b>Time Domain</b>   |  |
| <i>Max</i>           | Maximum code of collected data set.                |
| <i>Min</i>           | Minimum code of collected data set.                |
| <b>Histogram</b>     |  |
| <i>Max</i>           | Maximum code of collected data set.                |
| <i>Min</i>           | Minimum code of collected data set.                |
| <i>Mean</i>          | Mean of collected data set.                        |
| <i>Std Dev</i>       | Standard Deviation of collected data set.          |
| <i>Variance</i>      | Variance of collected data set.                    |
| <b>Signal FFT</b>    |  |
| <i>S/N</i>           | Signal to Noise of calculated FFT.                 |
| <i>S/PN</i>          | Signal to Peak Noise of calculated FFT.            |
| <i>S/D</i>           | Signal to Distortion of calculated FFT.            |
| <i>S/N+D</i>         | Signal to Noise plus Distortion of calculated FFT. |
| <i># of bins</i>     | Number of Bins covering the Nyquist frequency.     |
| <b>Noise FFT</b>     |  |
| <i>S/N</i>           | Signal to Noise of calculated FFT.                 |
| <i>S/PN</i>          | Signal to Peak Noise of calculated FFT.            |
| <i>Spot Noise dB</i> | Spot Noise in dB/Hz of calculated FFT.             |
| <i>Spot Noise nV</i> | Spot Noise in nV/rtHz of calculated FFT.           |
| <i># of bins</i>     | Number of Bins covering the Nyquist frequency.     |
| <b>Phase</b>         |  |
|                      | No statistics are calculated.                      |

### 3.4.3 Plot Enable

The *Plot Enable* control selects which channels are plotted for the current analysis. Multichannel plots are overlay plots with the highest number channel displayed as the top most plot. Only channels enabled by the *Plot Enable* control will report analysis error codes. Information about error codes can be accessed through the *Plot Error* controls.



### 3.4.4 *Cursor*

The *Cursor* control is used to identify a point on the graph using the mouse and then display its plot values. When any point within the plot area of the graph is clicked, the *Cursor* will snap to the closest plotted point and the plot values for that point display below the graph.

When using the *Zoom* function, the *Cursor* is used to select the corners of the area to zoom.

### 3.4.5 *Zoom*

The *ZOOM* function allows an area on the graph to be expanded. To use the zoom function, click the *ZOOM* button and select the box corners of the area on the graph to expand. The graph will then expand to show the details of this area, and the plot axes will be re-scaled. While zoomed, you can zoom in farther by repeating the process.

To restore the graph to its original scale, click the *RESTORE* button that appears while zoomed. If multiple zooms have been initiated, the *RESTORE* button will return to the previously viewed plot scale. Repeated *RESTORE* will eventually return to the original plot scale. From within multiple zooms the original scale can be directly restored by clicking the *REFRESH* button.

### 3.4.6 *Refresh*

The *REFRESH* button will clear and re-plot the current data set. *Refresh* can be used to apply new analysis parameters from the **Data Capture** sub-panel, or to restore a *ZOOM* graph to its default plot scale.

### 3.4.7 *Harmonics*

The *HARMONICS* control is only visible during a Signal FFT analysis and highlights the fundamental and harmonic bins used to calculate the Signal FFT statistics. *HARMONICS* highlighting helps to understand the source of any Signal FFT plot errors.

### 3.4.8 *Spot Noise*

The *Spot Noise* control (labeled *dB* or *nV*) is only visible during a Noise FFT analysis and selects the units used for plotting the graph, either dB/Hz or nV/rHz. The dB/Hz plot applies the *Full Scale Code* value from the **Data Capture** sub-panel on the **Setup** panel to determine the 0 dB point of the dB axis. The nV/rHz plot applies the *Full Scale Voltage* value from the **Data Capture** sub-panel on the **Setup** panel to determine the absolute scaling of the nV axis.

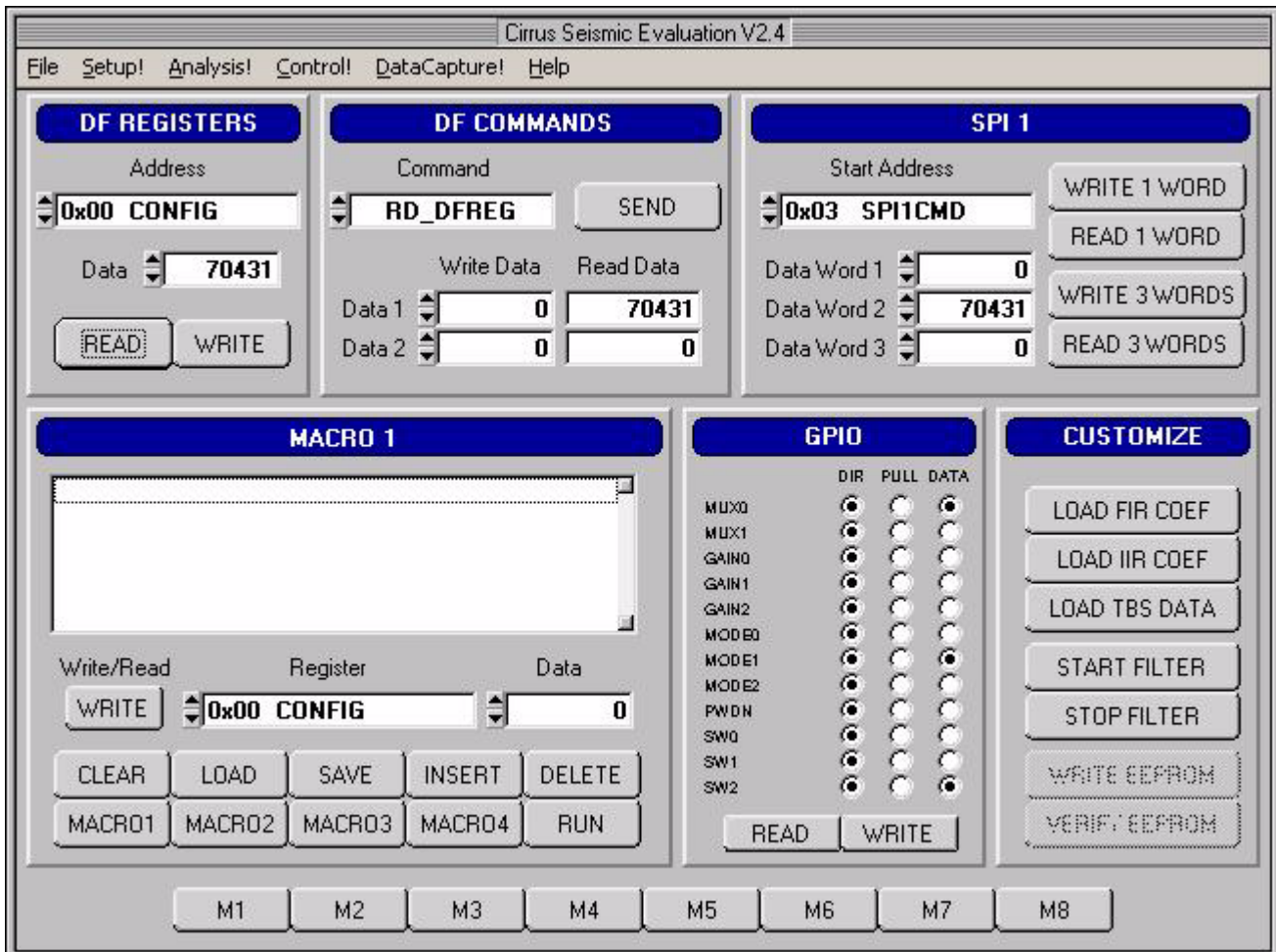
### 3.4.9 *Plot Error*

The *PLOT ERROR* control provides information about errors that occurred during an analysis. Analysis errors are only reported if the channel that has the error is currently plotted.

An analysis error stores an error code in the numerical display box of the *PLOT ERROR* control. If more than one error occurs, all error codes are stored and the last error code is displayed. Any of the accumulated error codes can be displayed by clicking on the numerical box and selecting it.

Once an error code is displayed in the numerical box, a description can be displayed by clicking the *PLOT ERROR* button. This causes a dialog box to display showing the error number, the error channel, and a text error message.

### 3.5 Control Panel



The **Control** panel is used to write and read register settings and to send commands to the digital filter. It consists of the following sub-panels and controls.

- **DF Registers**
- **DF Commands**
- **SPI1**
- **Macros**
- **GPIO**
- **Customize**
- **External Macros**

### 3.5.1 DF Registers

The **DF Registers** sub-panel writes and reads registers within the digital filter. Digital filter registers control operation of the digital filter and the included hardware peripherals, as described in the digital filter data sheet.

| Control        | Description   |
|----------------|---|
| <b>Address</b> | Selects a digital filter register.                      |
| <b>Data</b>    | Contains the data written to or read from the register. |
| <b>Read</b>    | Initiates a register read.                              |
| <b>Write</b>   | Initiates a register write.                             |

### 3.5.2 DF Commands

The **DF Commands** sub-panel sends commands to the digital filter. The digital filter commands and their required parameters are described in the digital filter data sheet.

Not all commands require write data values, and not all commands will return read data values. Some commands require formatted data files for uploading custom coefficients or test bit stream data. Example formatted data files are included in the SPI sub-directory of the software installation.

| Control             | Description   |
|---------------------|---|
| <b>Command</b>      | Selects the command to be written to the digital filter.        |
| <b>Write Data 1</b> | Contains the SPI1DAT1 data to be written to the digital filter. |
| <b>Write Data 2</b> | Contains the SPI1DAT2 data to be written to the digital filter. |
| <b>Read Data 1</b>  | Contains the SPI1DAT1 data read from the digital filter.        |
| <b>Read Data 2</b>  | Contains the SPI1DAT2 data read from the digital filter.        |
| <b>Send</b>         | Initiates the digital filter command.                           |

### 3.5.3 SPI

The **SPI** sub-panel writes and reads registers in the digital filter SPI register space. They can be used to check the SPI serial port status bits or to manually write commands to the digital filter.

| Control              | Description  |
|----------------------|--|
| <b>Start Address</b> | Selects the address to begin the SPI transaction.                        |
| <b>Data Word 1</b>   | Contains the first data word written to or read from the SPI registers.  |
| <b>Data Word 2</b>   | Contains the second data word written to or read from the SPI registers. |
| <b>Data Word 3</b>   | Contains the third data word written to or read from the SPI registers.  |
| <b>Read 1 Word</b>   | Initiates a 1 word SPI read transaction.                                 |
| <b>Read 3 Words</b>  | Initiates a 3 word SPI read transaction.                                 |
| <b>Write 1 Word</b>  | Initiates a 1 word SPI write transaction.                                |
| <b>Write 3 Words</b> | Initiates a 3 word SPI write transaction.                                |

### 3.5.4 Macros

The **Macros** sub-panel is designed to write a large number of registers with a single command. This allows the target evaluation system to be quickly set into a specific state for testing.

The **Register** control gives access to both digital filter registers and SPI1 registers. These registers can be written with data from the **Data** control, or data can be read and output to a text window. The **Register** control can also select special commands to be executed, with the **Data** control used to define a parameter value for the special command, if necessary.

| Control                | Description   |
|------------------------|---|
| <b>Write / Read</b>    | Selects the type of operation to be performed by the inserted macro command.  |
| <b>Register</b>        | Selects the target register for the inserted macro command. Also selects special commands that can be performed.  |
| <b>Data</b>            | Sets the register data value for the inserted macro command. Also sets the parameter value for special commands.  |
| <b>Clear</b>           | Clears the currently displayed macro.   |
| <b>Load</b>            | Loads a previously saved macro.   |
| <b>Save</b>            | Saves the currently displayed macro. Macros can be saved with unique names or can be saved as <i>External Macros</i> .                                  |
| <b>Insert</b>          | Inserts a macro command at the selected macro line. The macro command is built from the <i>Write/Read</i> , <i>Register</i> , and <i>Data</i> controls. |
| <b>Delete</b>          | Deletes the macro command at the selected macro line.   |
| <b>Macro1 - Macro4</b> | Selects which of the four working macros is displayed.  |
| <b>Run</b>             | Runs the currently displayed working macro.   |

### 3.5.5 GPIO

The **GPIO** sub-panel controls the digital filter GPIO pin configurations. GPIO pins have dedicated functions on the target board, but can be used in any manner for custom designs.

| Control          | Description  |
|------------------|--|
| <b>Direction</b> | Sets the selected GPIO pin as an output (*) or input ( ).  |
| <b>Pull Up</b>   | Turns the pull up resistor for the selected GPIO pin on (*) or off ( ).  |
| <b>Data</b>      | Sets the selected output GPIO pin to a high (*) or low ( ) level.  |
| <b>Write</b>     | Initiates a write to GPIO registers. The <i>Direction</i> , <i>Pull Up</i> and <i>Data</i> controls are read to determine the register values to be written. |
| <b>Read</b>      | Initiates a read from GPIO registers. The <i>Direction</i> , <i>Pull Up</i> and <i>Data</i> controls are updated based on the register values that are read. |

### 3.5.6 *Customize*

The **Customize** sub-panel sends commands to upload custom FIR and IIR filter coefficients, upload custom test bit stream data, start the digital filter, stop the digital filter, and write/read custom EEPROM configuration files to the on-board boot EEPROM. Example data files are included in a sub-directory of the software installation.

| Control              | Description  |
|----------------------|--|
| <b>Load FIR Coef</b> | Write a set of FIR coefficients into the digital filter from a file.     |
| <b>Load IIR Coef</b> | Write a set of IIR coefficients into the digital filter from a file.     |
| <b>Load TBS Data</b> | Write a set of test bit stream data into the digital filter from a file. |
| <b>Start Filter</b>  | Enables the digital filter by sending the <i>Start Filter</i> command.   |
| <b>Stop Filter</b>   | Disables the digital filter by sending the <i>Stop Filter</i> command.   |
| <b>Write EEPROM</b>  | Writes an EEPROM boot configuration file to the EEPROM memory.           |
| <b>Verify EEPROM</b> | Verifies EEPROM memory against an EEPROM boot configuration file.        |

### 3.5.7 *External Macros*

Macros are generated within the **Macros** sub-panel on the **Control** panel. Once a macro has been built it can either be saved with a unique macro name to be run within the **Macros** sub-panel, or saved as an external macro and be associated with one of the *External Macro* buttons.

A macro is saved as an *External Macro* by saving it in the `./macros/` subdirectory using the name `'m1.mac'`, `'m2.mac'`, etc. Depending on the selected name the macro will be associated with the corresponding *External Macro* button *M1*, *M2*, etc.

- *M1* = `./macros/m1.mac`
- *M2* = `./macros/m2.mac`
- etc.

*External Macro* buttons can be re-named on the panel by right clicking on them. The button name will change, but the macro associated with that button is always saved as `'m1.mac'`, `'m2.mac'`, etc., in the `./macros/` subdirectory. The *External Macro* button names are stored in the file `'Mnames.txt'`, also in the `./macros/` subdirectory.

*External Macros* allow up to eight macros to be accessed quickly without having to load them into the **Macros** sub-panel on the **Control** panel. These *External Macros* operate independently of the **Macros** sub-panel and are not affected by operations within it, except when a macro is saved to the `./macros/` subdirectory to replace a currently existing *External Macro*.

| Control        | Description   |
|----------------|---|
| <b>M1 - M8</b> | Runs the <i>External Macro</i> associated with that button. |

**4. BILL OF MATERIALS**

| Line Item | Part | Cirrus PN     | Rev | Description                         | Rev | BOM Desc: PWA CDB5376 | Rev | D | Status | Qty   | UM | Ref Desg  | Manf                           | Manf PN  | ECO | Effective Date | Notes           |
|-----------|------|---------------|-----|-------------------------------------|-----|-----------------------|-----|---|--------|-------|----|---|--------------------------------|--|-----|----------------|-----------------|
| 0001      | P    | 001-0345-01   | A   | CAP 0.1uF ±10% 50V X7R 0805         |     |                       |     |   | A      | 69 EA |    | C1 C2 C11 C12 C13 C15 C16 C17 C24 C25 C26 C27 C30 C31 C32 C33 C34 C42 C43 C44 C45 C48 C49 C51 C52 C54 C55 C57 C60 C61 C62 C63 C64 C65 C66 C67 C68 C69 C70 C71 C72 C73 C74 C75 C76 C77 C78 C79 C80 C81 C261 C262 C268 C361 C362 C368 C461 C462 C468 C506 C509 C513 C516 C542 C543 C563 C564 C569 | KEMET KOA PANASONIC MURATA VDK | C0805C103K5RAC<br>0805X7RHT103K<br>EC02YBHL04K<br>C0805X7R500-103KRE                       |     |                |                 |
| 0002      | P    | 001-04076-01  | A   | CAP 0.01uF ±10% 50V X7R 0805        |     |                       |     |   | A      | 8 EA  |    | C3 C4 C5 C9 C10 C14 C22 C23   | KEMET KOA PANASONIC MURATA VDK | C0805C103K5RAC<br>0805X7RHT103K<br>EC02YBHL04K<br>GRM216R7JH103KA01D<br>C0805X7R500-103KRE |     |                |                 |
| 0003      | P    | 004-00102-01  | A   | CAP 100uF ±10% 16V TANT CASE D      |     |                       |     |   | A      | 11 EA |    | C6 C7 C8 C18 C19 C20 C21 C28 C29 C35 C520   | KEMET VDK                      | T491D107K016AS<br>TA016TCM107KD  |     |                |                 |
| 0004      | P    | 001-06603-01  | A   | CAP 0.01uF ±5% 25V C0G 1206         |     |                       |     |   | A      | 27 EA |    | C37 C38 C39 C40 C41 C46 C47 C50 C237 C238 C239 C240 C246 C247 C250 C337 C338 C339 C340 C347 C437 C438 C439 C440 C447 C507 C510  | KEMET KOA                      | C1206C103J3GAC<br>12.06NPOET103J   |     |                |                 |
| 0005      | P    | 000-00000-09  | A   | NO POP CAP 1206                     |     |                       |     |   | A      | 0 EA  |    | C53 C56 C58 C253 C256 C258 C346 C350 C353 C356 C358 C446 C450 C453 C456 C458  | NO POP                         | NP-CAP-1206  |     |                | DO NOT POPULATE |
| 0006      | P    | 004-00068-01  | A   | CAP 4.7uF ±10% 10V TANT CASE A      |     |                       |     |   | A      | 1 EA  |    | C59   | KEMET VDK                      | T491A475K010AS<br>TA010TCM475KAR<br>TAJ4475K010R   |     |                |                 |
| 0007      | P    | 070-00004-01  | A   | DIODE SCHOTTKY BARRIER 30V 0.2A AXL |     |                       |     |   | A      | 4 EA  |    | D1 D2 D3 D4   | PHILIPS                        | BA785  |     |                |                 |
| 0008      | P    | 070-00024-01  | A   | DIODE SWT 70V 215mA SOT-23          |     |                       |     |   | A      | 16 EA |    | D5 D6 D7 D8 D205 D206 D207 D208 D305 D306 D307 D308 D405 D406 D407 D408   | SEMICONDUCTOR                  | BAV991J71  |     |                |                 |
| 0009      | P    | 070-00055-01  | A   | DIODE ARRAY 5V (TVS) ESD SOT143     |     |                       |     |   | A      | 1 EA  |    | D9  | LITTELFUSE                     | SP9503BART   |     |                |                 |
| 0010      | P    | 165-00004-01  | A   | LED CLR SUP RED 1.7V 1mA 1.6MCD SMD |     |                       |     |   | A      | 1 EA  |    | D10   | CHICAGO MINIATURE LAMP         | MDZ8-21SRC/TR8/T1  |     |                |                 |
| 0011      | P    | 110-00028-01  | A   | CON BLCR-PCB RCPT RA                |     |                       |     |   | A      | 1 EA  |    | J4  | POMONA KINGS                   | Model 4788<br>KC-79-237 M06  |     |                |                 |
| 0012      | P    | 130-00007-01  | A   | JACK BAN SOLDER TERM, NYLON INS GRN |     |                       |     |   | A      | 1 EA  |    | J6  | JOHNSON COMPONENTS             | 108-0904-001   |     |                | SEE COMMENTS    |
| 0013      | P    | 130-00009-01  | A   | JACK BAN SOLDER TERM, NYLON INS YLW |     |                       |     |   | A      | 1 EA  |    | J7  | JOHNSON COMPONENTS             | 108-0907-001   |     |                | SEE COMMENTS    |
| 0014      | P    | 130-00014-01  | A   | JACK BAN SOLDER TERM NYLON INS RED  |     |                       |     |   | A      | 1 EA  |    | J8  | JOHNSON COMPONENTS             | 108-0903-001   |     |                | SEE COMMENTS    |
| 0015      | P    | 130-00006-01  | A   | JACK BAN SOLDER TERM, NYLON INS RED |     |                       |     |   | A      | 1 EA  |    | J9  | JOHNSON COMPONENTS             | 108-0902-001   |     |                | SEE COMMENTS    |
| 0016      | P    | 115-00016-01  | A   | HDR 3x2 MLE .1"CTR S GLD            |     |                       |     |   | A      | 3 EA  |    | J10 J11 J21   | SAMTEC                         | TSM-103-07-G-D   |     |                |                 |
| 0017      | P    | 115-00013-01  | A   | HDR 2x2 MLE .1"CTR S GLD            |     |                       |     |   | A      | 11 EA |    | J12 J13 J19 J20 J22 J23 J33 J34 J43 J58 J519  | SAMTEC                         | TSM-103-07-G-D   |     |                |                 |
| 0018      | P    | 115-00012-01  | A   | HDR 4x2 MLE .1"CTR S GLD            |     |                       |     |   | A      | 4 EA  |    | J14 J15 J24 J25   | SAMTEC                         | TSM-104-07-G-D   |     |                |                 |
| 0019      | P    | 115-00030-01  | A   | HDR 6x2 MLE .1"CTR S GLD            |     |                       |     |   | A      | 1 EA  |    | J16   | SAMTEC                         | TSM-106-07-G-D   |     |                |                 |
| 0020      | P    | 115-00029-01  | A   | HDR 8x2 MLE .1" CTR 062BD ST GLD TH |     |                       |     |   | A      | 2 EA  |    | J17 J18   | SAMTEC                         | TSM-108-07-G-D   |     |                |                 |
| 0021      | P    | 115-00011-01  | A   | HDR 10x2 MLE .1"CTR 062BD ST GLD TH |     |                       |     |   | A      | 1 EA  |    | J26   | SAMTEC FCI                     | TSM-110-07-G-D<br>67996-220  |     |                |                 |
| 0022      | P    | 115-00081-01  | A   | HDR 12x2 MLE .1" CTR D GLD          |     |                       |     |   | A      | 4 EA  |    | J27 J27 J327 J427   | SAMTEC                         | TSM-112-07-G-D   |     |                | DO NOT POPULATE |
| 0023      | P    | 115-00023-01  | A   | HDR 14x2 MLE .1"CTR S GLD           |     |                       |     |   | A      | 0 EA  |    | J30 J37   | SAMTEC                         | TSM-114-07-G-D   |     |                | SEE COMMENTS    |
| 0024      | P    | 110-00085-01  | A   | CON TERM BLOCK 4 POS 5mm C/C BLUE   |     |                       |     |   | A      | 8 EA  |    | J32 J41 J232 J241 J332 J341 J432 J441   | ON-SHORE TECHNOLOGY            | ED 100/4DS   |     |                |                 |
| 0025      | P    | 115-000176-01 | A   | HDR 7x2 ML 2MM CTR 062BD S GLD TH   |     |                       |     |   | A      | 1 EA  |    | J39   | MOLEX                          | 87758-1416   |     |                |                 |
| 0026      | P    | 110-00041-01  | A   | CON RA USB BLK                      |     |                       |     |   | A      | 1 EA  |    | J47   | AMP                            | 787780-1   |     |                |                 |
| 0027      | P    | 110-00056-01  | A   | CON TERM BLOCK 2 POS 5mm C/C BLUE   |     |                       |     |   | A      | 3 EA  |    | J50 J59 J63   | ON-SHORE TECHNOLOGY            | ED 100/2DS   |     |                |                 |
| 0028      | P    | 115-00014-01  | A   | HDR 2x1 ML .1"CTR 062BD ST GLD TH   |     |                       |     |   | A      | 1 EA  |    | J56   | SAMTEC FCI                     | TSM-102-07-G-S<br>68000-202<br>103741-2  |     |                |                 |
| 0029      | P    | 115-00003-01  | A   | HDR 5x2 MLE .1"CTR S GLD            |     |                       |     |   | A      | 1 EA  |    | J60   | SAMTEC                         | TSM-105-07-G-D   |     |                |                 |

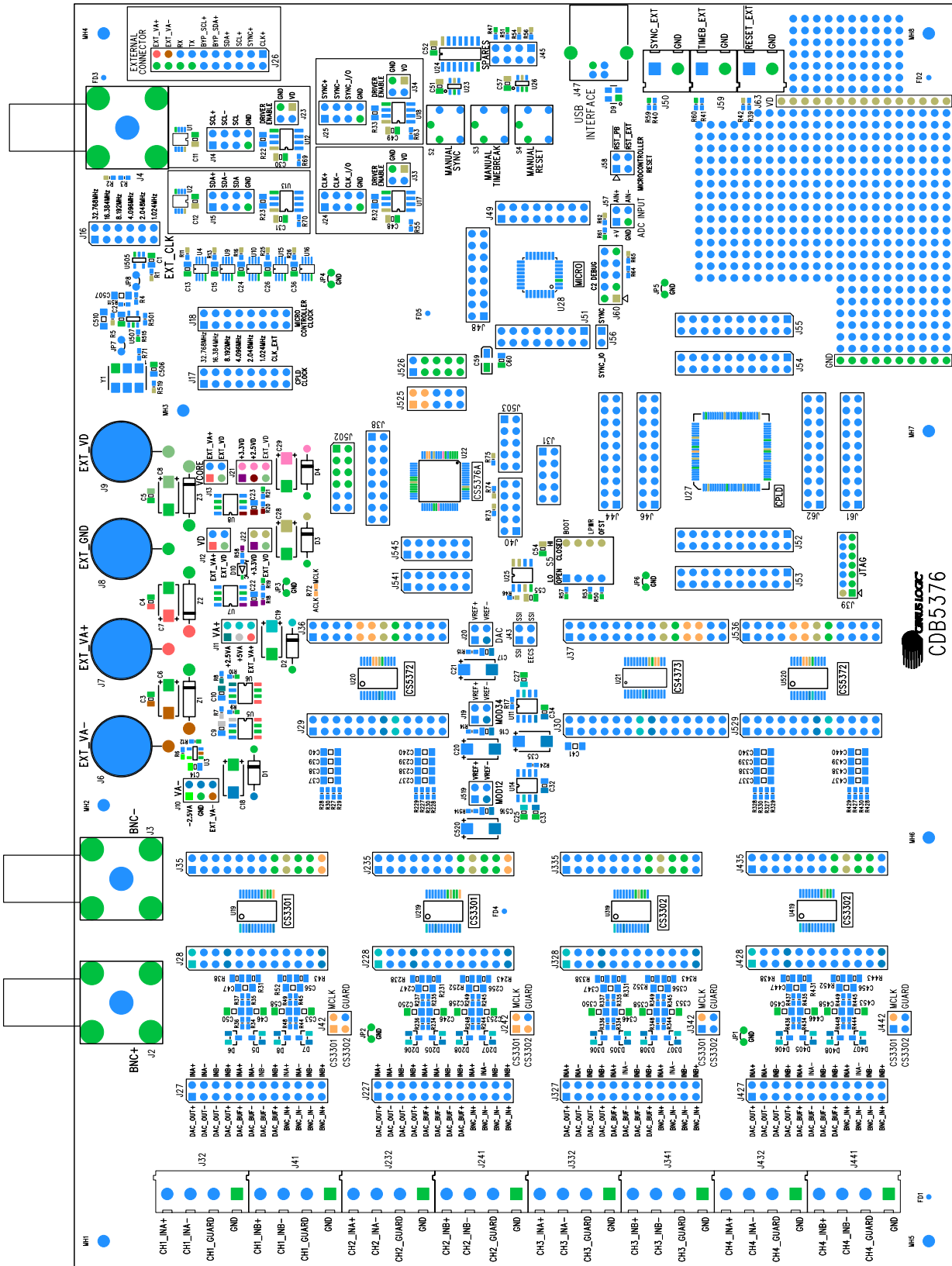
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|-----------|------|--------------|-----|---------------------------------------|--------|------|---|---|------------------------------|---------|-----|----------------|-----------------|
| 0030      | P    | 060-00004-01 | A   | WIRE, JUMPER 2P, 0.1"CTR, BRASS       | A      | 8EA  | JP1 JP2 JP3 JP4 JP5 JP6 JP7 JP8   | COMPONENTS CORPORATION                        | TP-101-10                    |         |     |                |                 |
| 0031      | P    | 304-00001-01 | A   | SPCR, STANDOFF 4-40 THR, 0.875"L      | A      | 8EA  | MHT MH2 MH3 MH4 MH5 MH6 MH7 MH8   | KEystone                                      | 1809                         |         |     |                | SEE COMMENTS    |
| 0032      | P    | 020-00788-01 | A   | RES 10 OHM 1/10W ±1% 0603 FILM        | A      | 13EA | R1 R5 R11 R13 R14 R15 R16 R24 R25 R26 R68 R514 R519   | DALE KOA PANASONIC                            |                              |         |     |                |                 |
| 0033      | P    | 020-01244-01 | A   | RES 100K OHM 1/10W ±1% 0603 FILM      | A      | 8EA  | R2 R42 R46 R50 R53 R57 R59 R60  | DALE KOA PANASONIC                            |                              |         |     |                |                 |
| 0034      | P    | 020-00934-01 | A   | RES 200 OHM 1/10W ±1% 0603 FILM       | A      | 23EA | R3 R17 R34 R35 R36 R37 R39 R40 R41 R55 R63 R69 R70 R71 R72 R234 R235 R236 R237 R335 R337 R435 R437  | DALE KOA PANASONIC                            |                              |         |     |                |                 |
| 0035      | P    | 020-01130-01 | A   | RES 10K OHM 1/10W ±1% 0603 FILM       | A      | 16EA | R4 R6 R7 R8 R18 R20 R47 R51 R54 R56 R73 R74 R75 R601 R511 R515  | DALE KOA PANASONIC VENKEL                     |                              |         |     |                |                 |
| 0036      | P    | 020-01074-01 | A   | RES 3.32K OHM 1/10W ±1% 0603 FILM     | A      | 2EA  | R9 R58  | DALE KOA PANASONIC                            |                              |         |     |                |                 |
| 0037      | P    | 020-01128-01 | A   | RES 9.53K OHM 1/10W ±1% 0603 FILM     | A      | 3EA  | R10 R12 R21   | DALE KOA PANASONIC                            |                              |         |     |                |                 |
| 0038      | P    | 020-01104-01 | A   | RES 5.9K OHM 1/10W ±1% 0603 FILM      | A      | 1EA  | R19   | DALE KOA PANASONIC                            |                              |         |     |                |                 |
| 0039      | P    | 000-00000-01 | A   | NO POP RES 0605                       | A      | 0EA  | R22 R23 R32 R33 R43 R52 R243 R252 R343 R352 R443 R452   | NO POP  | NP-RES-0805                  |         |     |                | DO NOT POPULATE |
| 0040      | P    | 020-00673-01 | A   | RES 0 OHM 1/10W ±5% 0603 FILM         | A      | 37EA | R27 R28 R29 R30 R44 R45 R48 R49 R62 R227 R228 R229 R230 R244 R245 R248 R249 R327 R328 R329 R330 R334 R336 R344 R348 R348 R349 R427 R428 R429 R430 R434 R436 R444 R445 R448 R449 | DALE NRC0603000Z NRC0606Z0TR PANASONIC VENKEL |                              |         |     |                |                 |
| 0041      | P    | 020-01962-01 | A   | RES 20K OHM 1/8W ±1% 0805 FILM        | A      | 4EA  | R31 R38 R231 R238   | DALE KOA PANASONIC                            |                              |         |     |                |                 |
| 0042      | P    | 000-00000-02 | A   | NO POP RES 0603                       | A      | 0EA  | R61   | NO POP  | NP-RES-0603                  |         |     |                | DO NOT POPULATE |
| 0043      | P    | 020-01016-01 | A   | RES 1K OHM 1/10W ±1% 0603 FILM        | A      | 4EA  | R64 R65 R66 R67   | DALE KOA PANASONIC                            |                              |         |     |                |                 |
| 0044      | P    | 021-01391-01 | A   | RES 18M OHM 1/8W ±5% 0805             | A      | 4EA  | R331 R338 R431 R438   | PANASONIC                                     | ERJ6GEYK185V                 |         |     |                |                 |
| 0045      | P    | 120-00002-01 | A   | SWITCH 01T TACT W/ESD                 | A      | 3EA  | S2 S3 S4  | C&K   | WTS645TUS0 EVO-P2KC20        |         |     |                | SEE COMMENTS    |
| 0046      | P    | 120-00011-01 | A   | SWITCH, 4 POS, DIP, RAISED, SPST      | A      | 1EA  | S5  | GRAYHILL                                      | 765B04                       |         |     |                |                 |
| 0047      | P    | 060-00195-01 | A   | IC LOW V DUAL SPST ANA SWITCH MSOP8   | A      | 2EA  | U1 U2   | VISHAY  | DG2003DQ                     |         |     |                |                 |
| 0048      | P    | 060-00063-01 | A   | IC LNR, V REG 200mA NEG ADJ SOT23-5   | A      | 1EA  | U3  | LINEAR TECH                                   | LT11964ES5-BYP               |         |     |                |                 |
| 0049      | P    | 061-00062-01 | A   | IC LOG, LITTLE LOG SINGLE D-FF SSOP8  | A      | 5EA  | U4 U9 U10 U15 U16   | TEXAS INSTRUMENTS                             | SN74LVC2974DCTR              |         |     |                |                 |
| 0050      | P    | 060-00062-01 | A   | IC LNR, V REG, LNOISE 500mA SO8-150   | A      | 4EA  | U5 U6 U7 U8   | LINEAR TECH                                   | LT11763CS8                   |         |     |                |                 |
| 0051      | P    | 065-00039-03 | D   | IC CRUS LOW V AMP DC-1KHZ SOIC8       | A      | 1EA  | U11   | CIRRUS LOGIC                                  | CS3011-IS/D                  |         |     |                |                 |
| 0052      | P    | 060-00162-01 | A   | IC 3.3V U LOW PWR RS485 XCVR SOIC8    | A      | 4EA  | U12 U13 U17 U18   | LINEAR TECH                                   | LTC1480IS8                   |         |     |                |                 |
| 0053      | P    | 060-00236-01 | A   | IC LNR, PRCV, REF 2.5V, TC10, SO8-150 | A      | 1EA  | U14   | LINEAR TECH                                   | LT1019A1848-2.5              |         |     |                |                 |
| 0054      | P    | 065-00051-01 | C   | IC CRUS 24 SSOP DIDO AMP              | A      | 2EA  | U19 U219  | CIRRUS LOGIC                                  | CS3301-IS/G                  |         |     |                |                 |
| 0055      | P    | 065-00174-Z1 | G   | IC CRUS DUAL MODULATOR SSOP24 NPb     | A      | 2EA  | U20 U20   | CIRRUS LOGIC                                  | CS3322-B2Z/G                 |         |     |                |                 |
| 0056      | P    | 065-00173-Z1 | D   | IC CRUS TEST DAC SSOP28 NPb           | A      | 1EA  | U21   | CIRRUS LOGIC                                  | CS4373A-18Z/D                |         |     |                |                 |
| 0057      | P    | 065-00056-01 | A   | IC CRUS QUAD DIG FILTER TOPP64        | A      | 1EA  | U22   | CIRRUS LOGIC                                  | CS5376A-10/A                 |         |     |                |                 |
| 0058      | P    | 060-00067-01 | A   | IC LNR DUAL CMOS SW DEBNCR SOT223-6   | A      | 2EA  | U23 U26   | MAXIM   | MAX6617EUT-T                 |         |     |                |                 |
| 0059      | P    | 061-00084-01 | A   | IC LOG, HEX INVERTER S014-150         | A      | 1EA  | U24   | TEXAS INSTRUMENTS                             | SN74LVC04D                   |         |     |                | SEE COMMENTS    |
| 0060      | P    | 062-00022-01 | A   | IC PGM EEPROM 8KX8 SPT SRL SOIC8      | A      | 1EA  | U25   | ATMEL   | AT25640N-10S1-2.7 CAT25C6481 |         |     |                | SEE COMMENTS    |
| 0061      | P    | 062-00055-01 | A   | IC PGM 128 MACROCELL CPLD VQFP100     | A      | 1EA  | U27   | CATALYST SEMICONDUCTOR                        | XCR3128XL-10VQ1001           |         |     |                | SEE COMMENTS    |
| 0062      | P    | 062-00079-01 | A   | IC PGM USB 16KB FLASH MCU LQFP32      | A      | 1EA  | U28   | SILICON LABORATORIES                          | C8051F320                    |         |     |                | SEE COMMENTS    |
| 0063      | P    | 065-00052-01 | C   | IC CRUS 24 SSOP DIDO AMP              | A      | 2EA  | U319 U419   | CIRRUS LOGIC                                  | CS3302-IS/C                  |         |     |                | SEE COMMENTS    |



| Line Item  | Part | Cirrus PN    | Rev | Description                         | Status | Qty  | UM  | Ref Desc | Manf               | Manf PN                  | ECO    | Effective Date | Notes           |
|--|------|--------------|-----|-------------------------------------|--------|------|---|----------|--------------------|--------------------------|--------|----------------|-----------------|
| <b>BOM#: 505-00018-01 Rev: D BOM Desc: PWA CDB5376</b> |      |              |     |                                     |        |      |   |          |                    |                          |        |                |                 |
| 0064   | P    | 061-00061-01 | A   | IC LOG. LITTLE LOG 2IN XOR SOT-23-5 | A      | 1EA  | U605  |          | TEXAS INSTRUMENTS  | SN74VCLG86DBVR           |        |                |                 |
| 0065   | P    | 060-00075-01 | A   | IC 1.29MHZ R-TX-R OP AMP SOT-23     | A      | 1EA  | U507  |          | LINERAR TECH       | LTT7831S5                |        |                |                 |
| 0066   | P    | 070-00017-02 | A   | OSC 33.768MHz 100ppm 3.3V V CNTL SM | A      | 1EA  | Y1  |          | CITIZEN            | CSK750VBEL32-7.68MTR     | ECO286 |                |                 |
| 0067   | P    | 070-00005-01 | A   | DIODE TR 13V 600W AXL               | A      | 3EA  | Z1 Z2 Z3  |          | LITTELFUSE         | P6KE13A                  |        |                |                 |
| 0068   | P    | 080-00003-01 | A   | WIRE BPOST 1.5X.25" 24/19 GA BLU    | A      | 4EA  | XJ6 XJ7 XJ8 XJ9   |          | SQUIRES            | L-                       |        |                | SEE COMMENTS    |
| 0069   | P    | 300-00001-01 | A   | SCREW 4-40X5/16" PH STEEL           | A      | 8EA  | XMH1 XMH2 XMH3 XMH4 XMH5 XMH6 XMH7 XMH8                 |          | BUILDING FASTENERS | PMS 440 0031 PH          |        |                | SEE COMMENTS    |
| 0070   | P    | 110-00013-01 | D   | CON SHUNT 2P .1"CTR BLK             | A      | 45EA |   |          | MOLEX              | 15-29-1025               |        |                |                 |
| 0071   | A    | 422-00013-01 | B   | LBL SUBASSY PRODUCT ID AND REV      | A      | 1EA  |   |          | AMP                | 382811-6                 |        |                |                 |
| 0072   | P    | 240-00018-21 | D   | PCB SUBASSY                         | A      | 1EA  |   |          | 3M                 | 929950-00                |        |                |                 |
| 0073   | P    | 603-00018-01 | D   | ASSY DMG PWA CDB5376                | A      | 1REF |   |          | CIRRUS LOGIC       | 422-00013-01             | ECO286 |                |                 |
| 0074   | P    | 600-00018-01 | D   | SCHEM CDB5376                       | A      | 1REF |   |          | CIRRUS LOGIC       | 240-00018-01             | ECO286 |                |                 |
| 0075   | P    | 602-00018-01 | C   | TST PROC CDB5376                    | A      | 1REF |   |          | CIRRUS LOGIC       | 603-00018-01             | ECO286 |                |                 |
| 0076   | P    | 110-00028-01 | A   | CON BNC-PCB RCPT RA                 | A      | 0EA  | J2 J3   |          | POMONA KINGS       | 600-00018-01             |        |                | DO NOT POPULATE |
| 0077   | P    | 115-00061-01 | A   | HDR 12x2 MLE .1" CTR D GLD          | A      | 0EA  | J28 J29 J35 J36 J228 J235 J328 J335 J428 J435 J529 J536 |          | SAMTEC             | Model 4788 KC-79-237 M06 |        |                | DO NOT POPULATE |
| 0078   | P    | 115-00003-01 | A   | HDR 5x2 MLE .1"CTR S GLD            | A      | 0EA  | J31 J40 J503 J525 J526                                  |          | SAMTEC             | TSW-112-07-G-D           |        |                | DO NOT POPULATE |
| 0079   | P    | 115-00029-01 | A   | HDR 8x2 ML .1" CTR 062BD ST GLD TH  | A      | 0EA  | J38 J48 J49 J51   |          | SAMTEC             | TSW-105-07-G-D           |        |                | DO NOT POPULATE |
| 0080   | P    | 115-00013-01 | A   | HDR 2x2 MLE .1"CTR S GLD            | A      | 0EA  | J42 J57 J242 J342 J442                                  |          | SAMTEC             | TSW-108-07-G-D           |        |                | DO NOT POPULATE |
| 0081   | P    | 115-00011-01 | A   | HDR 10x2 ML .1"CTR 062BD ST GLD TH  | A      | 0EA  | J44 J46 J52 J53 J54 J55 J61 J62                         |          | SAMTEC             | TSW-102-07-G-D           |        |                | DO NOT POPULATE |
| 0082   | P    | 115-00012-01 | A   | HDR 4x2 MLE .1"CTR S GLD            | A      | 0EA  | J45   |          | PCI                | 67996-220                |        |                | DO NOT POPULATE |
| 0083   | P    | 115-00030-01 | A   | HDR 6x2 MLE .1"CTR S GLD            | A      | 0EA  | J502 J541 J545  |          | SAMTEC             | TSW-104-07-G-D           |        |                | DO NOT POPULATE |

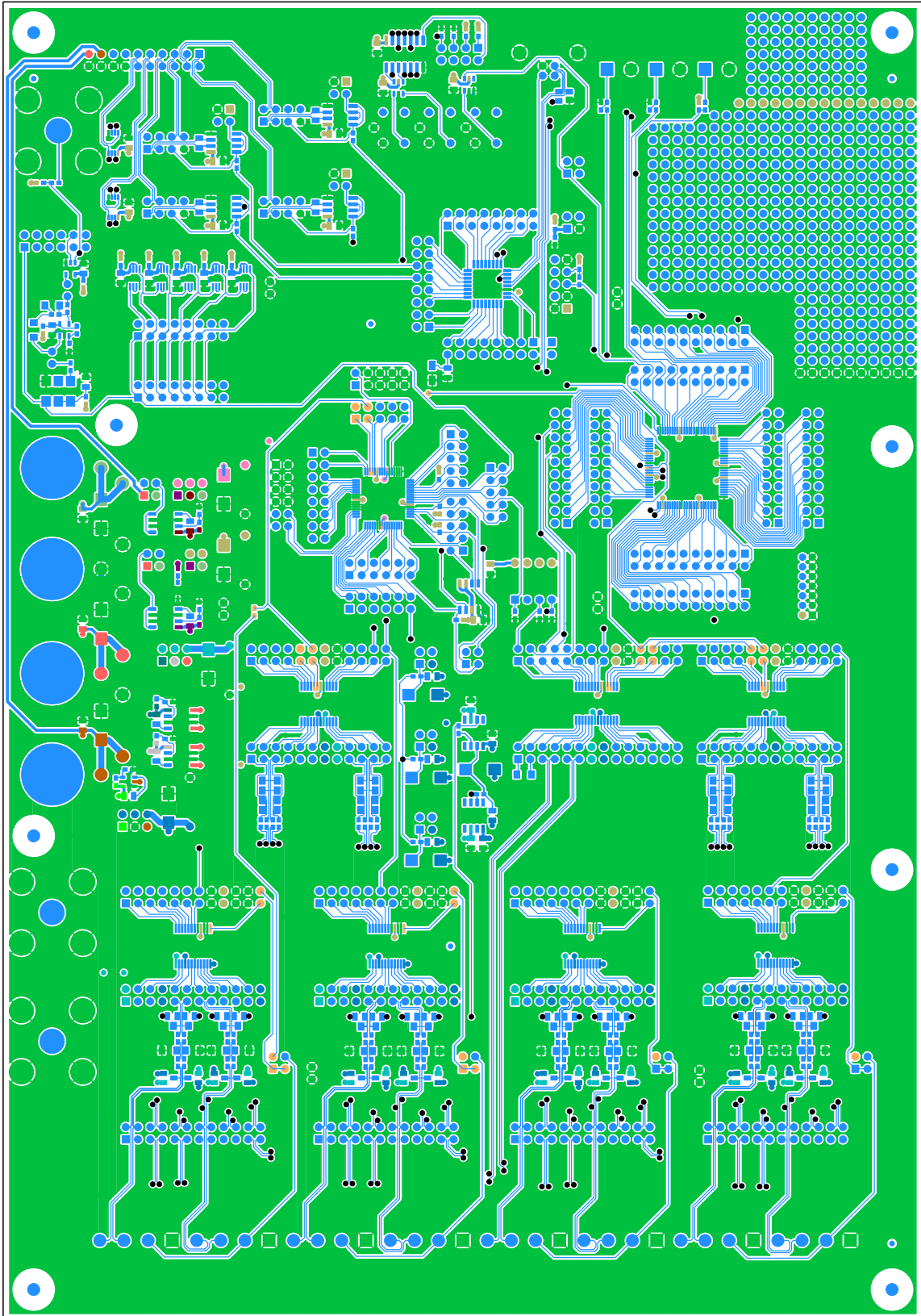
**BOM Comments**  
 LINE 12-15: REQUIRES BINDING POST HOOK UP WIRE. CIRRUS PN: 080-00003-01  
 LINE 24: ASSEMBLE CONNECTORS TOGETHER BEFORE INSERTING INTO PCB  
 LINE 31: REQUIRES 4-40 PAN HEAD SCREW. CIRRUS PN: 300-00001-01  
 LINE 45: INSTALL AFTER WASH PROCESS.  
 LINE 60: PROGRAMMED AT TEST.  
 LINE 61: PROGRAMMED AT TEST.  
 LINE 62: PROGRAMMED AT TEST.  
 LINE 68: WIRES FOR BINDING POST  
 LINE 69: SCREWS FOR STANDOFFS  
 LINE 70: SHUNTS USED DURING TEST.

### 5. LAYER PLOTS



CIRRUS LOGIC PCB 240-00018-Z1 Rev D

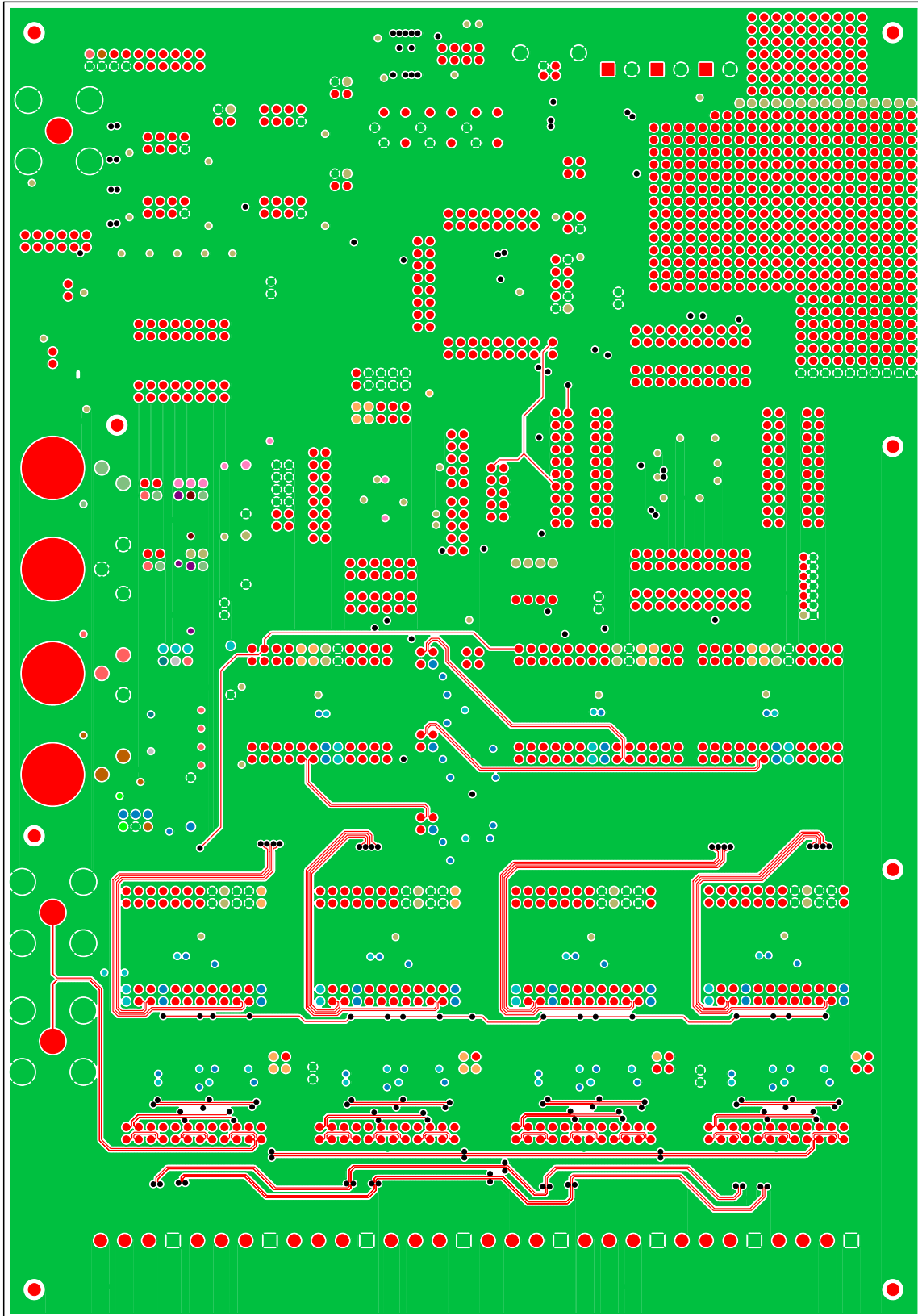
SILKSCREEN TOP



PCB 240-00018-Z1 Rev D

CIRRUS LOGIC

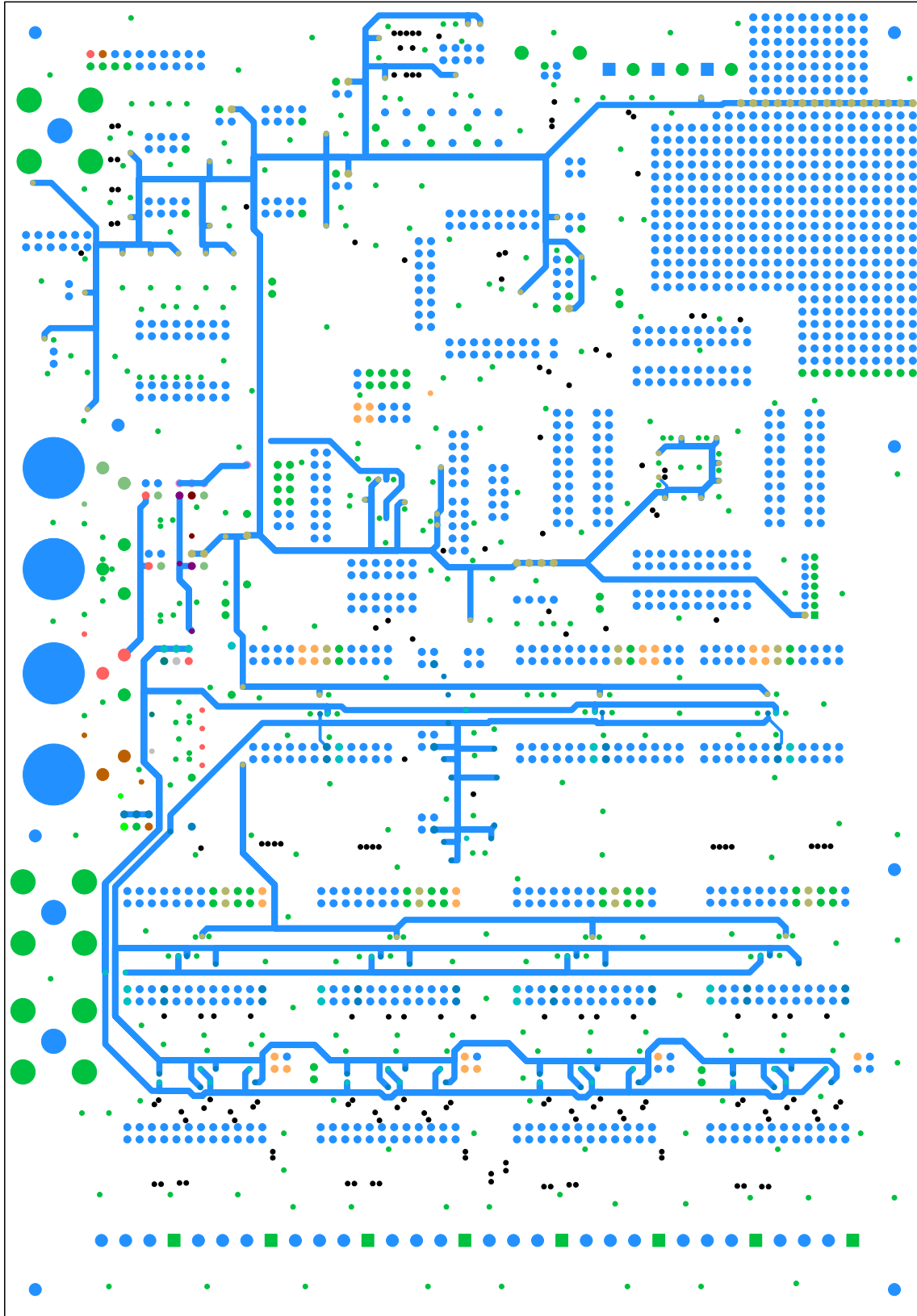
TOP SIDE ANALOG



PCB 240-00018-Z1 Rev D

CIRRUS LOGIC

LAYER2 ANALOG

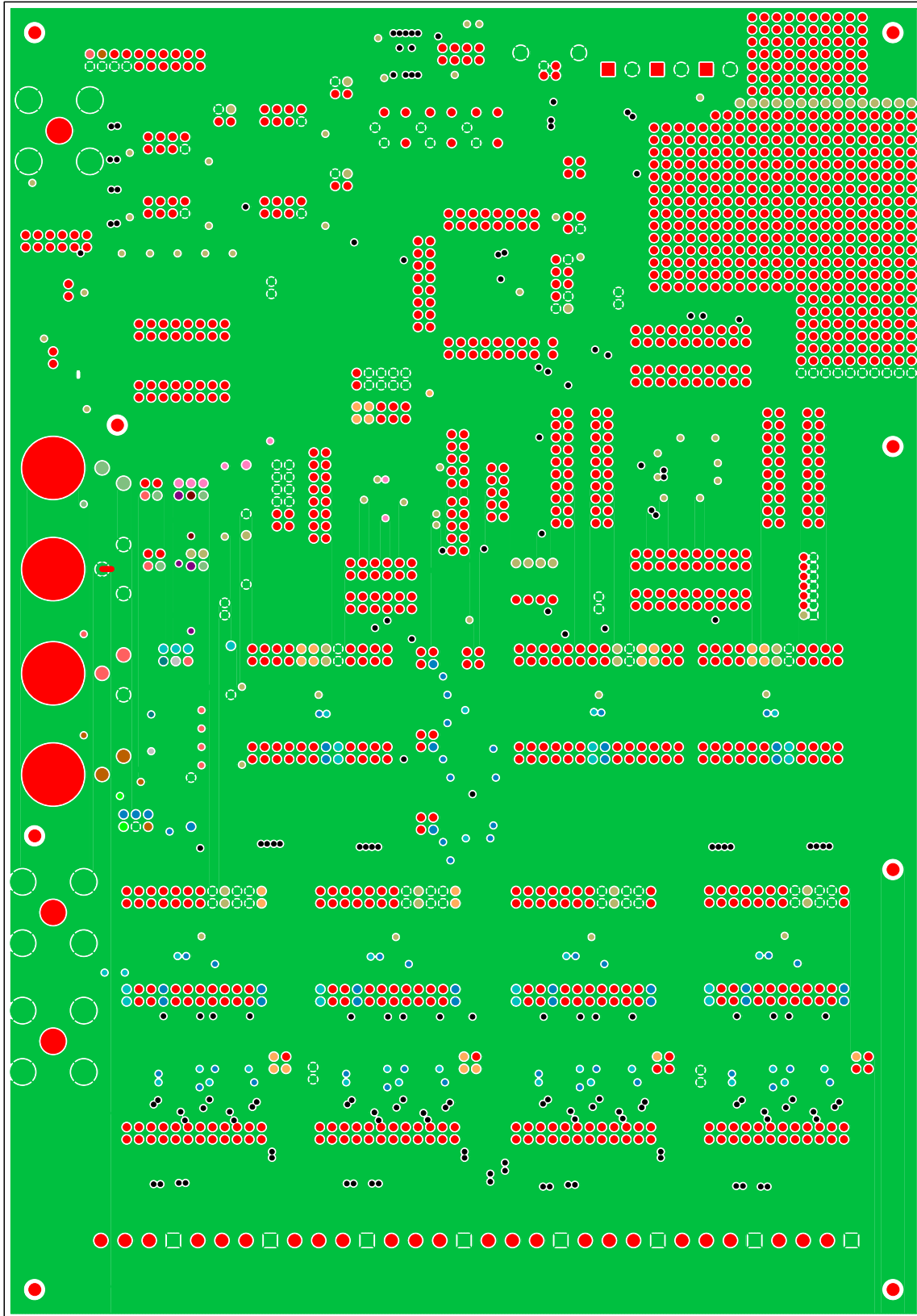


PCB 240-00018-Z1 Rev D

CIRRUS LOGIC

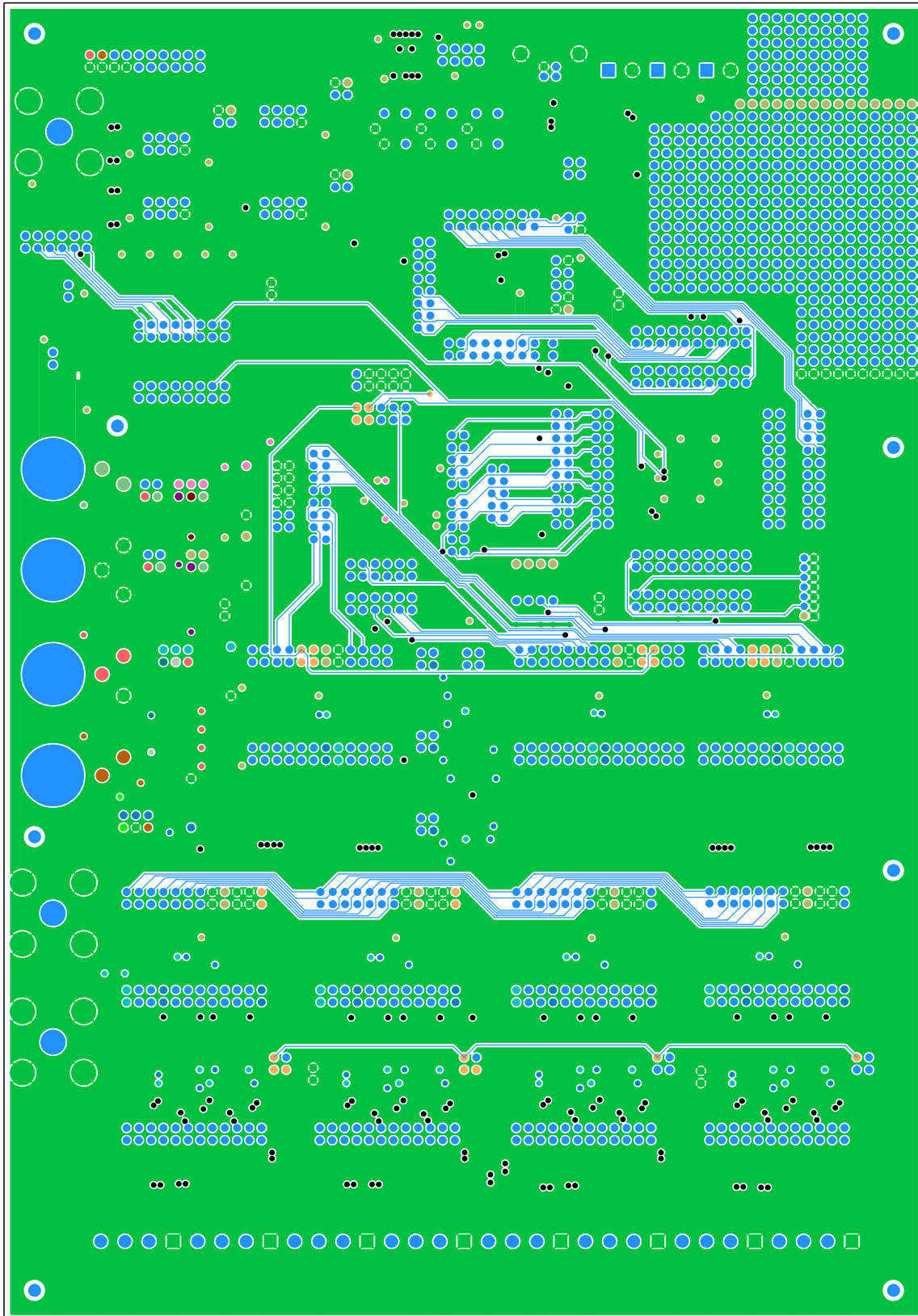
LAYER3 POWER





CIRRUS LOGIC PCB 240-00018-Z1 Rev D

LAYER4 GND



CIRRUS LOGIC PCB 240-00018-Z1 Rev D

LAYERS DIGITAL

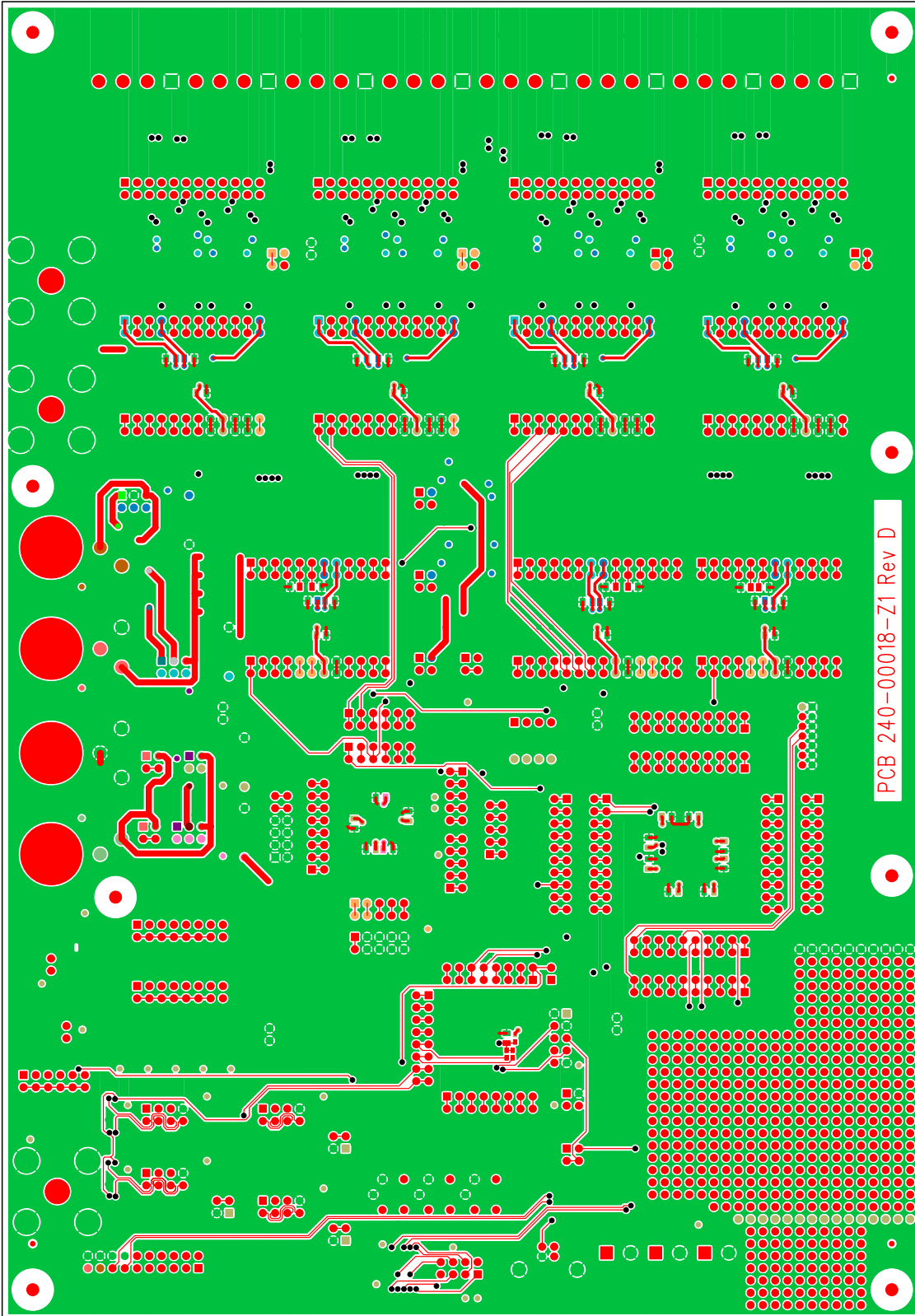


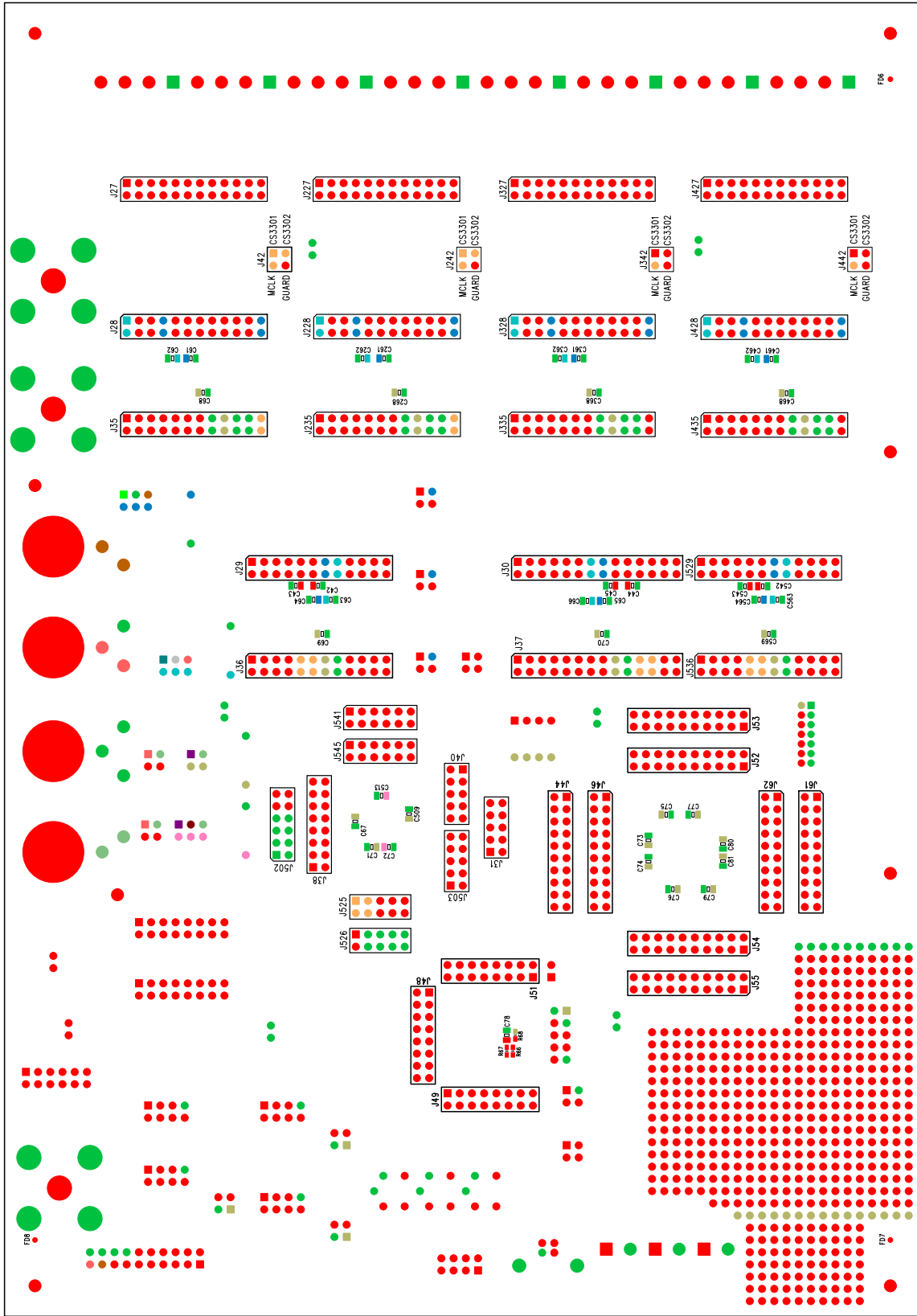
BOTTOM SIDE

CIRRUS LOGIC

PCB 240-00018-Z1 Rev D

PCB 540-00018-S1 Rev D

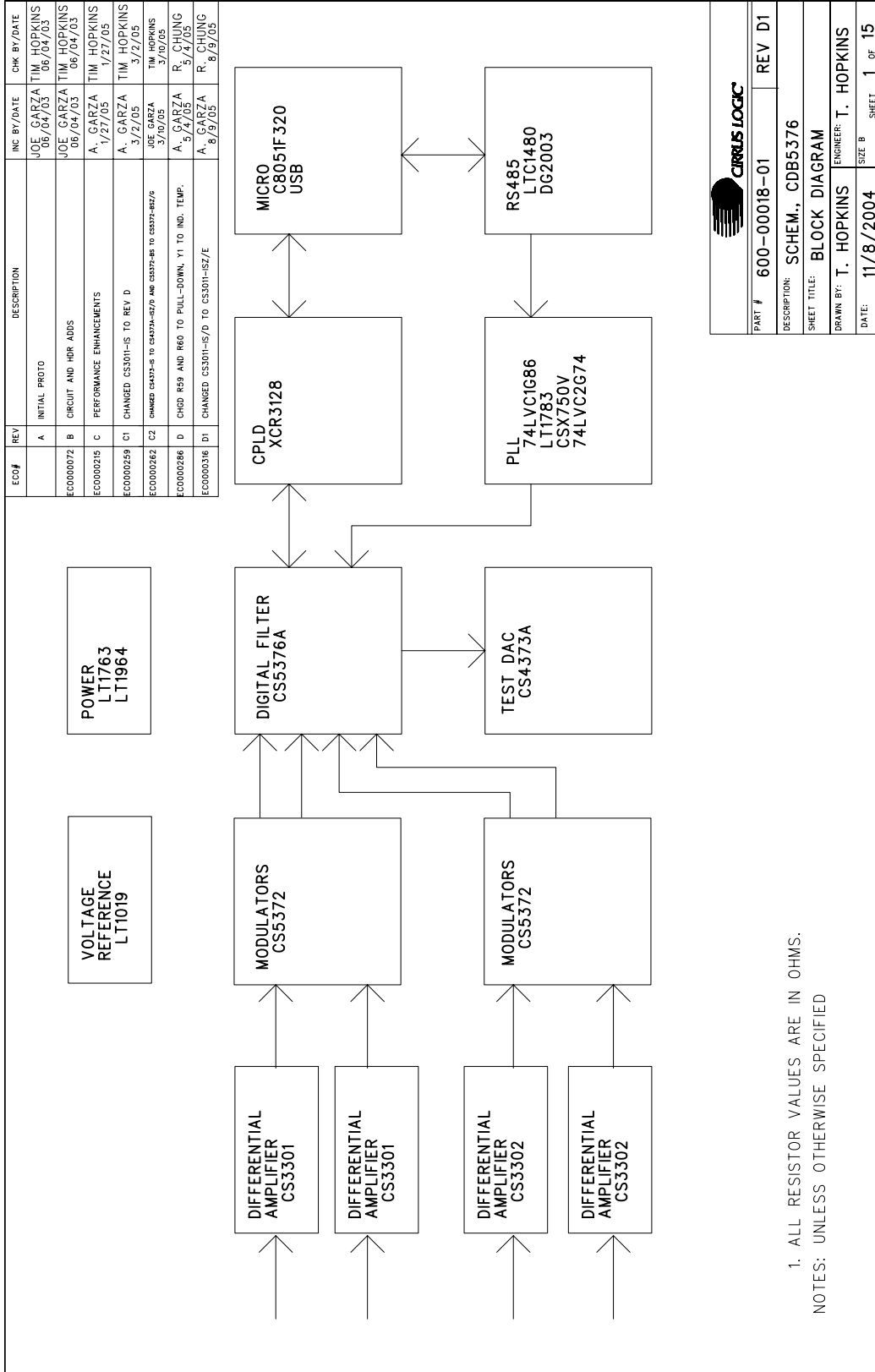


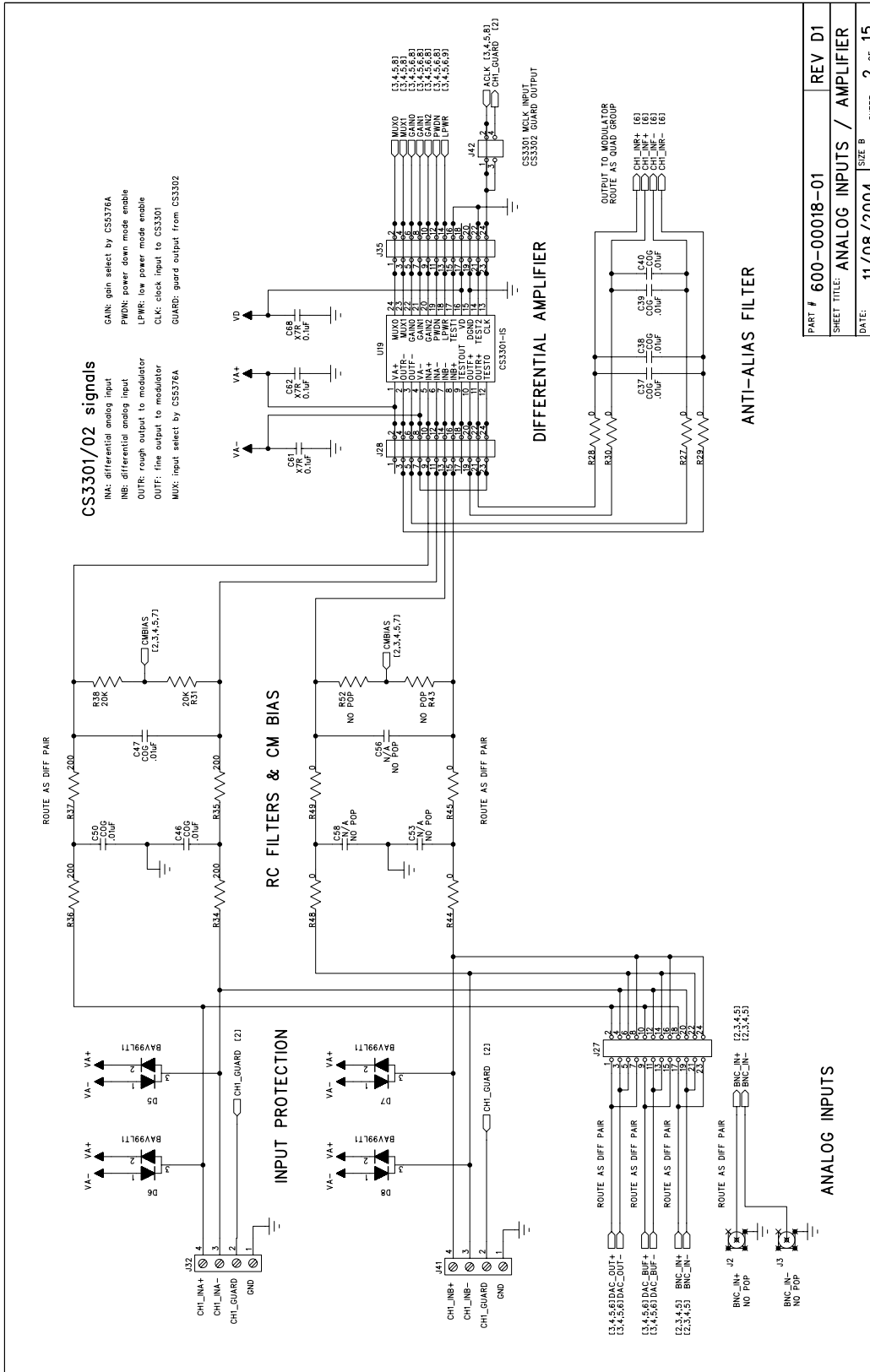


CIRRUS LOGIC

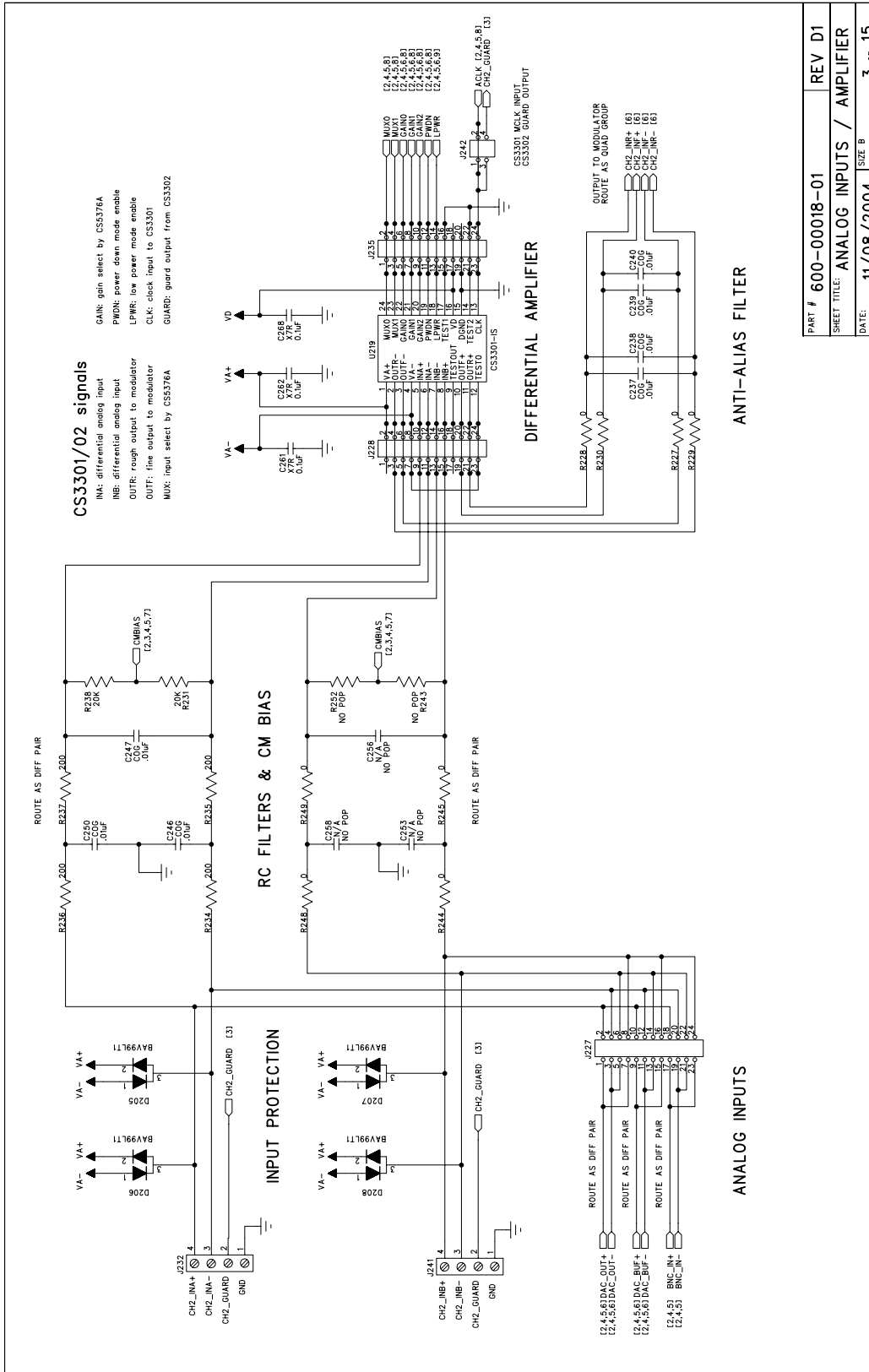
BCB 540-00018-S1 Rev D

21K2SCREEN BOTTOM

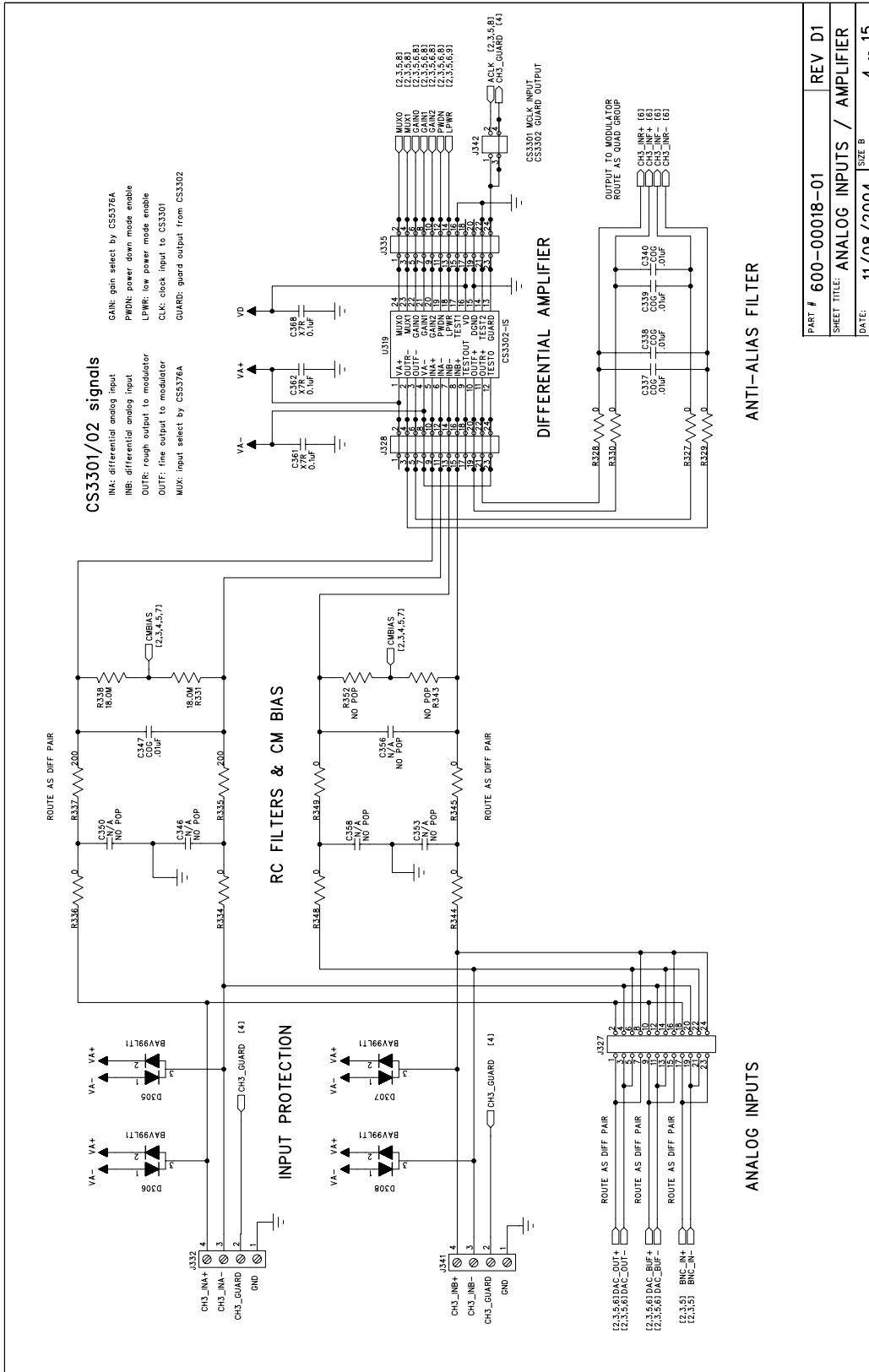
**6. SCHEMATICS**




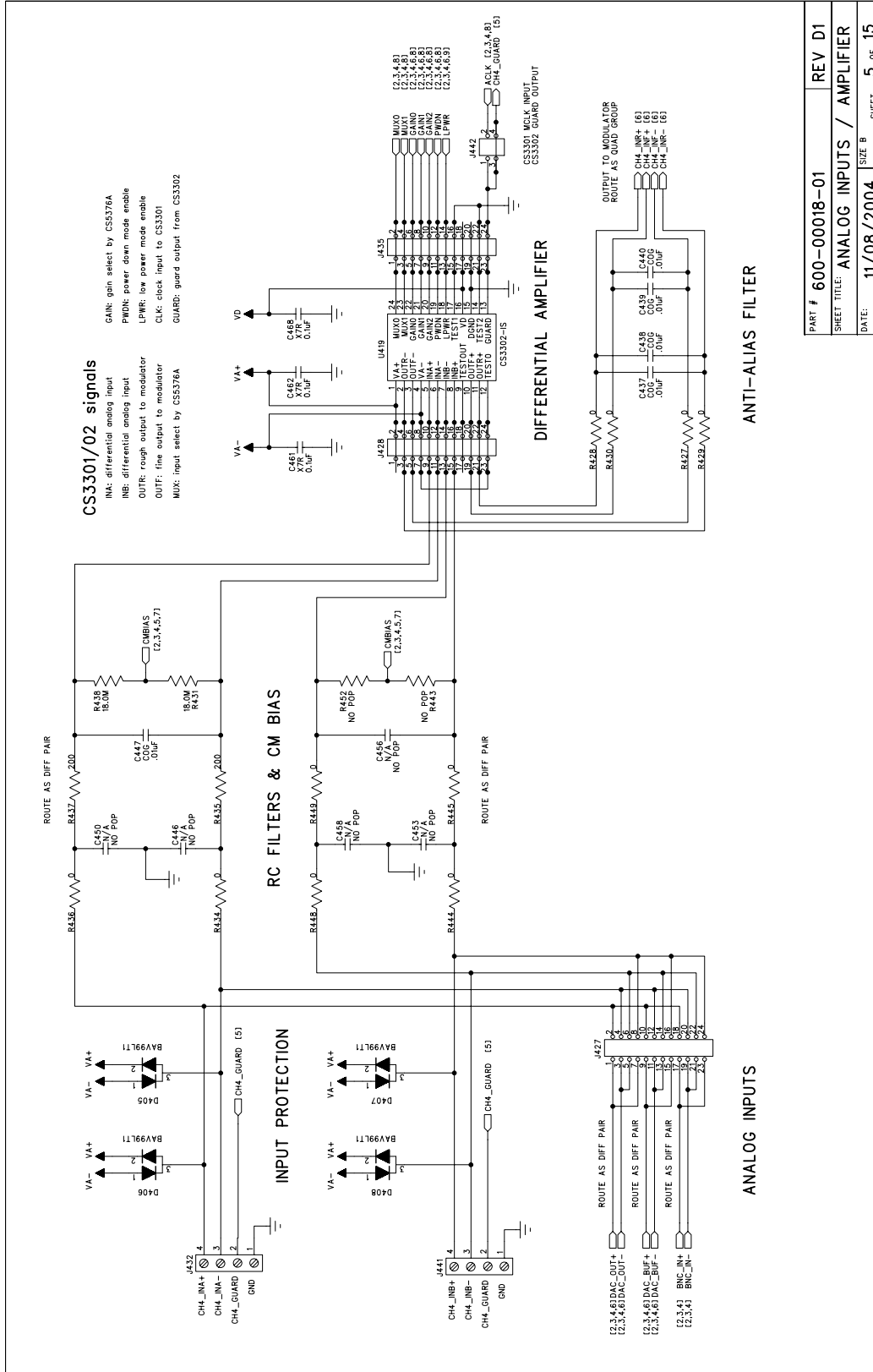
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| SHEET TITLE: | ANALOG INPUTS / AMPLIFIER |        |               |
| DATE:        | 11/08/2004                | SIZE B | SHEET 2 OF 15 |



|              |                           |       |         |
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| DATE:        | 11/08/2004                | SHEET | 3 OF 15 |

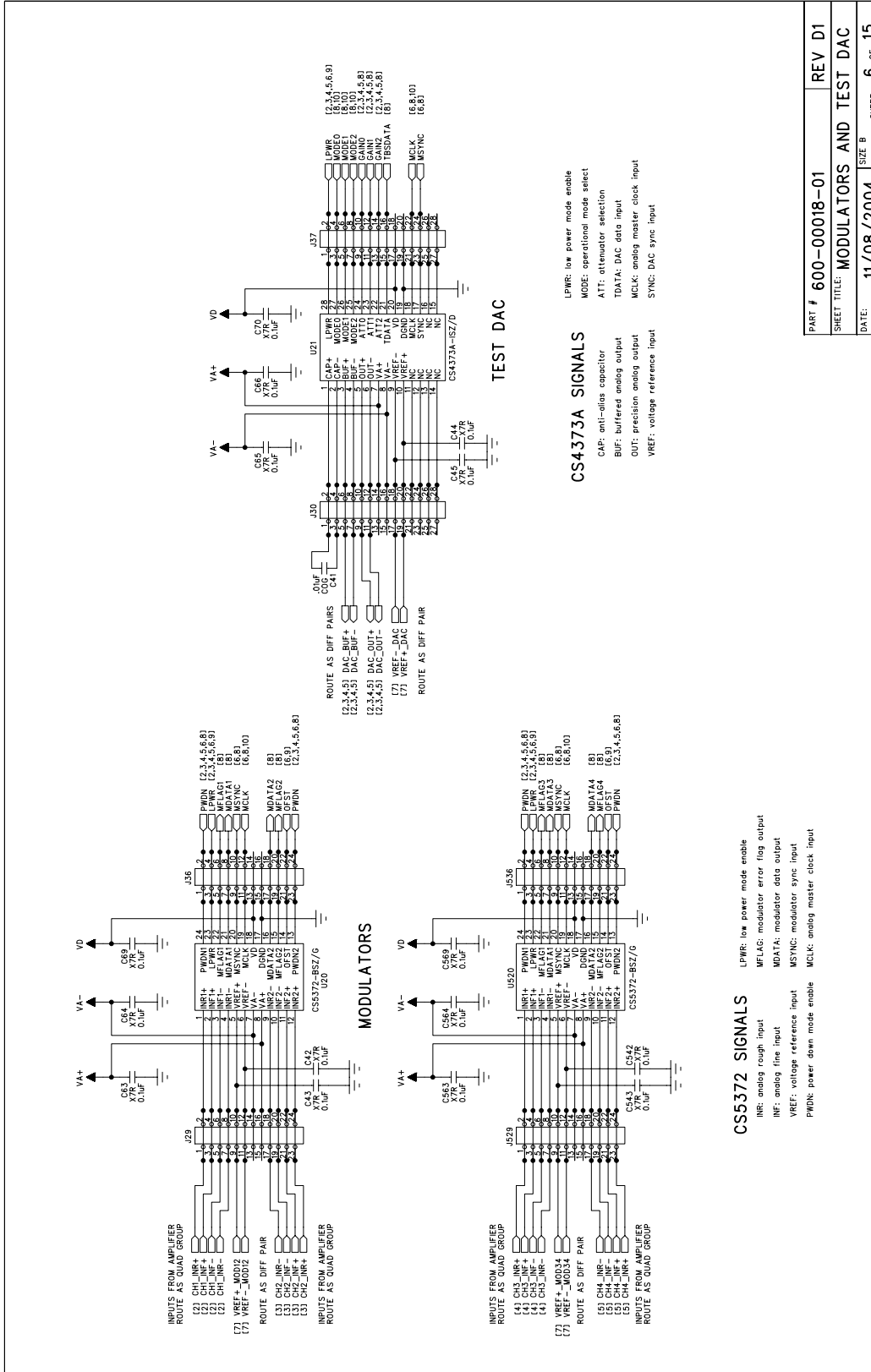


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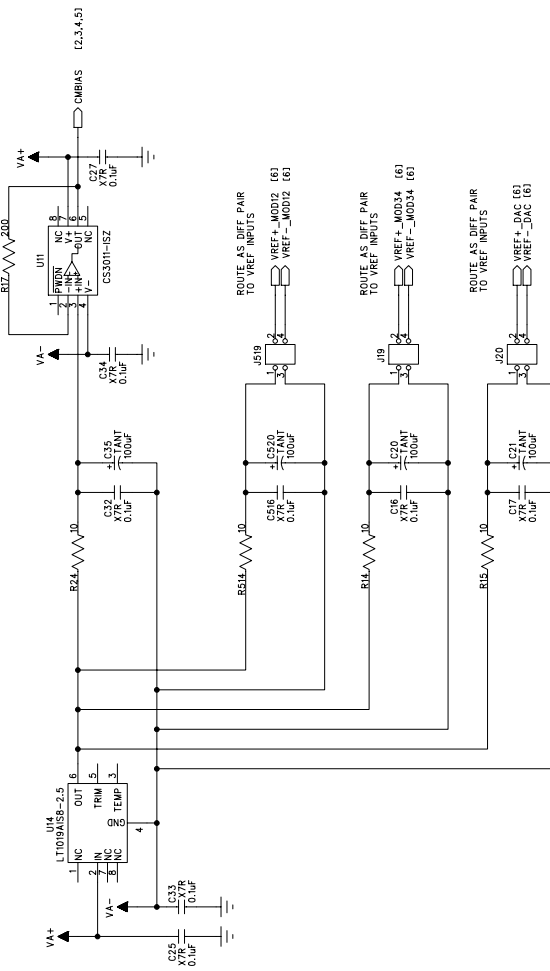


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| DATE:        | 11/08/2004                | SIZE  | B       |
|              |                           | SHEET | 5 OF 15 |

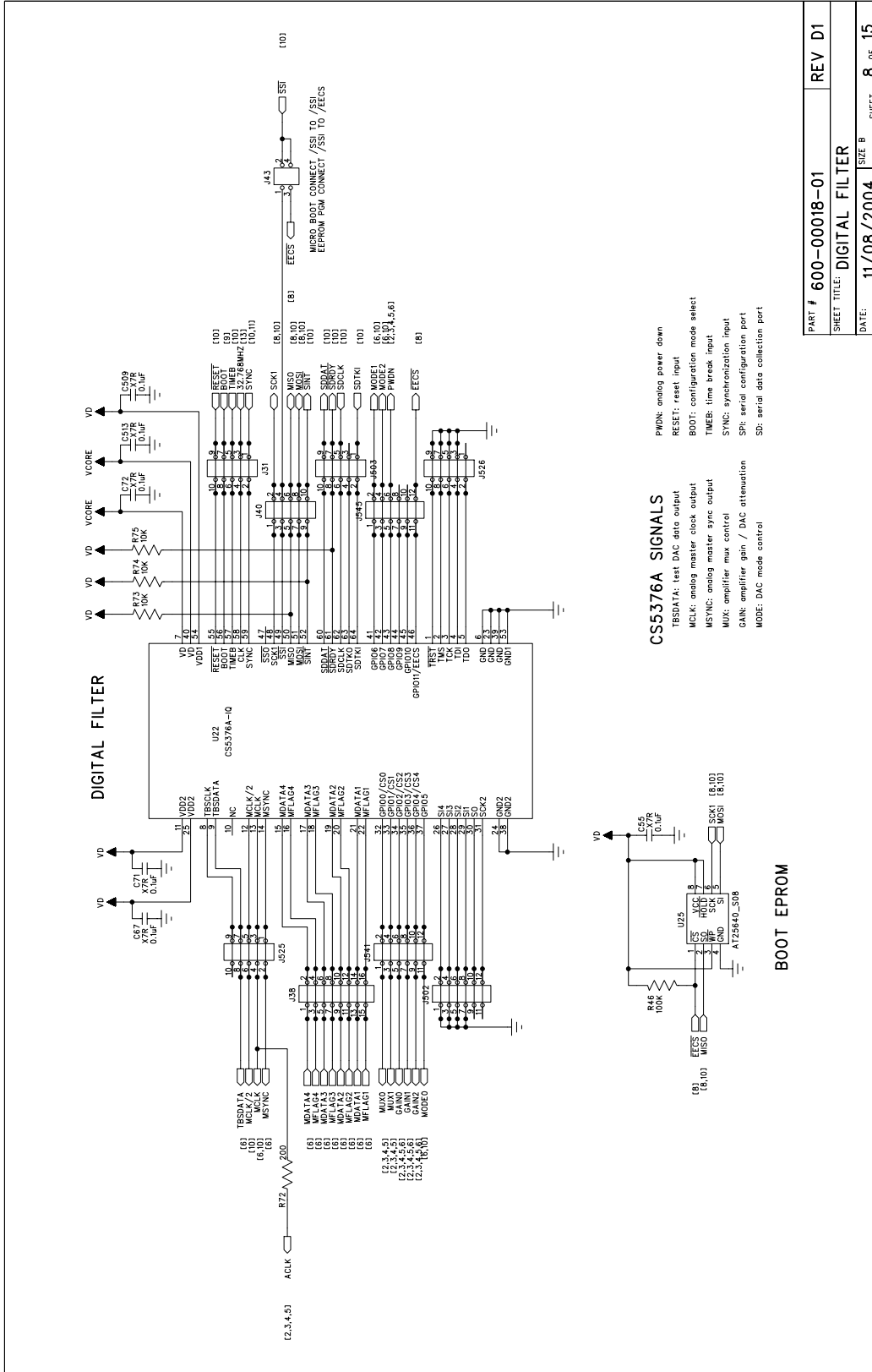


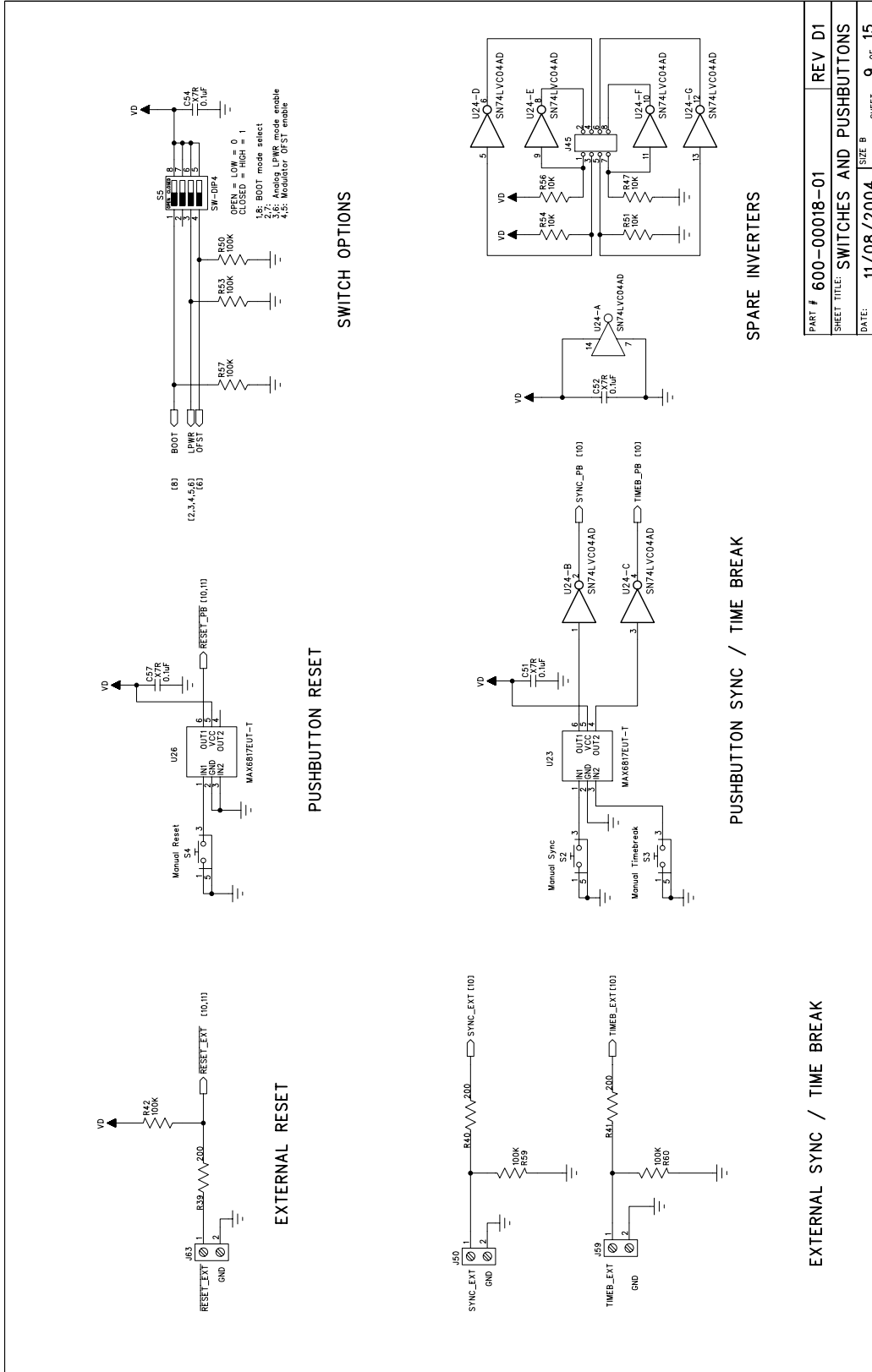


|              |                         |       |         |
|--------------|-------------------------|-------|---------|
| PART #       | 600-00018-01            | REV   | D1      |
| SHEET TITLE: | MODULATORS AND TEST DAC |       |         |
| DATE:        | 11/08/2004              | SIZE  | B       |
|              |                         | SHEET | 6 of 15 |

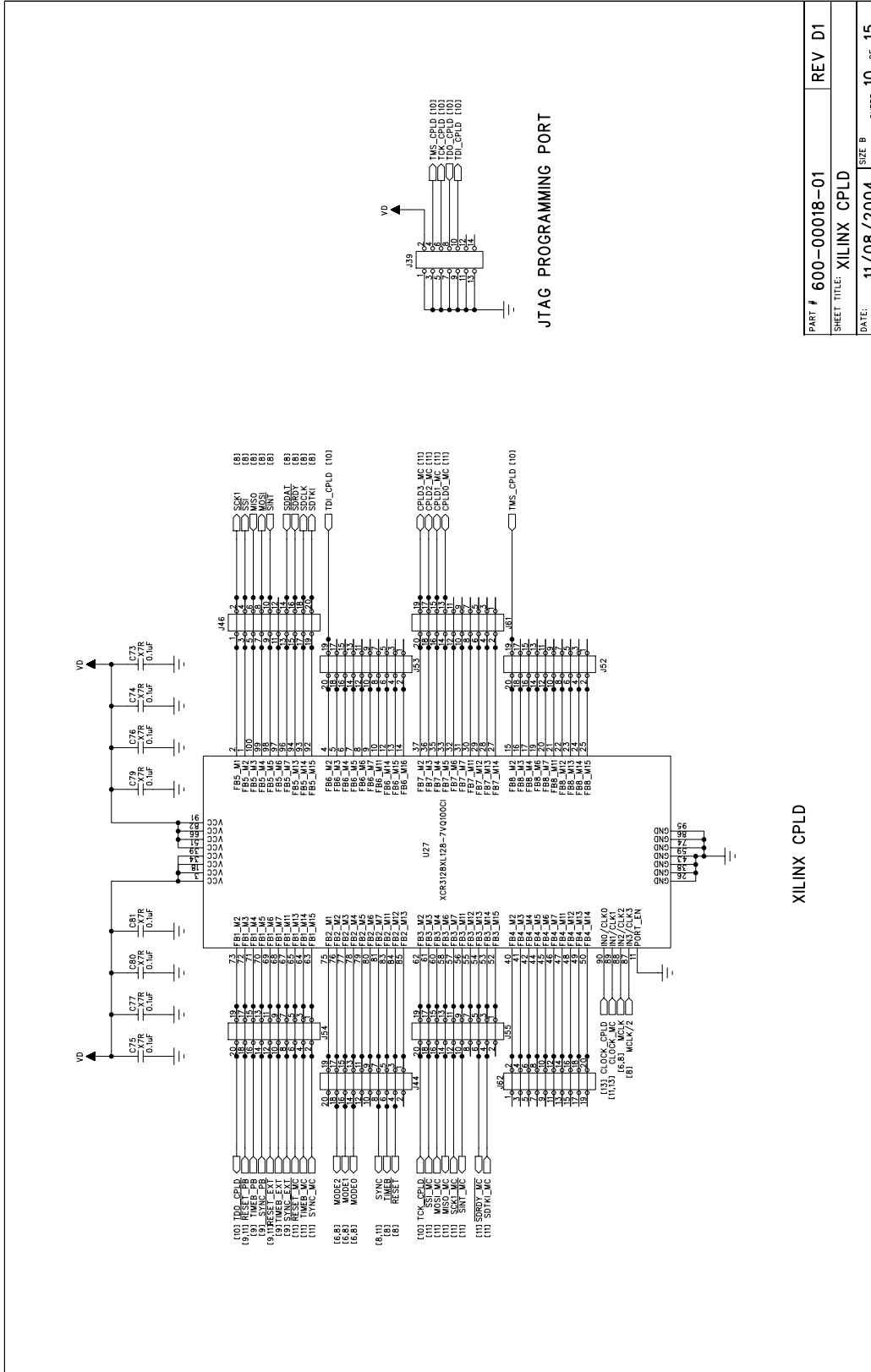
**VOLTAGE REFERENCE**


|              |                   |       |         |
|--------------|-------------------|-------|---------|
| PART #       | 600-00018-01      | REV   | D1      |
| SHEET TITLE: | VOLTAGE REFERENCE |       |         |
| DATE:        | 11/08/2004        | SHEET | 7 OF 15 |





|              |                          |        |               |
|--------------|--------------------------|--------|---------------|
| PART #       | 600-00018-01             | REV    | D1            |
| SHEET TITLE: | SWITCHES AND PUSHBUTTONS |        |               |
| DATE:        | 11/08/2004               | SIZE B | SHEET 9 OF 15 |



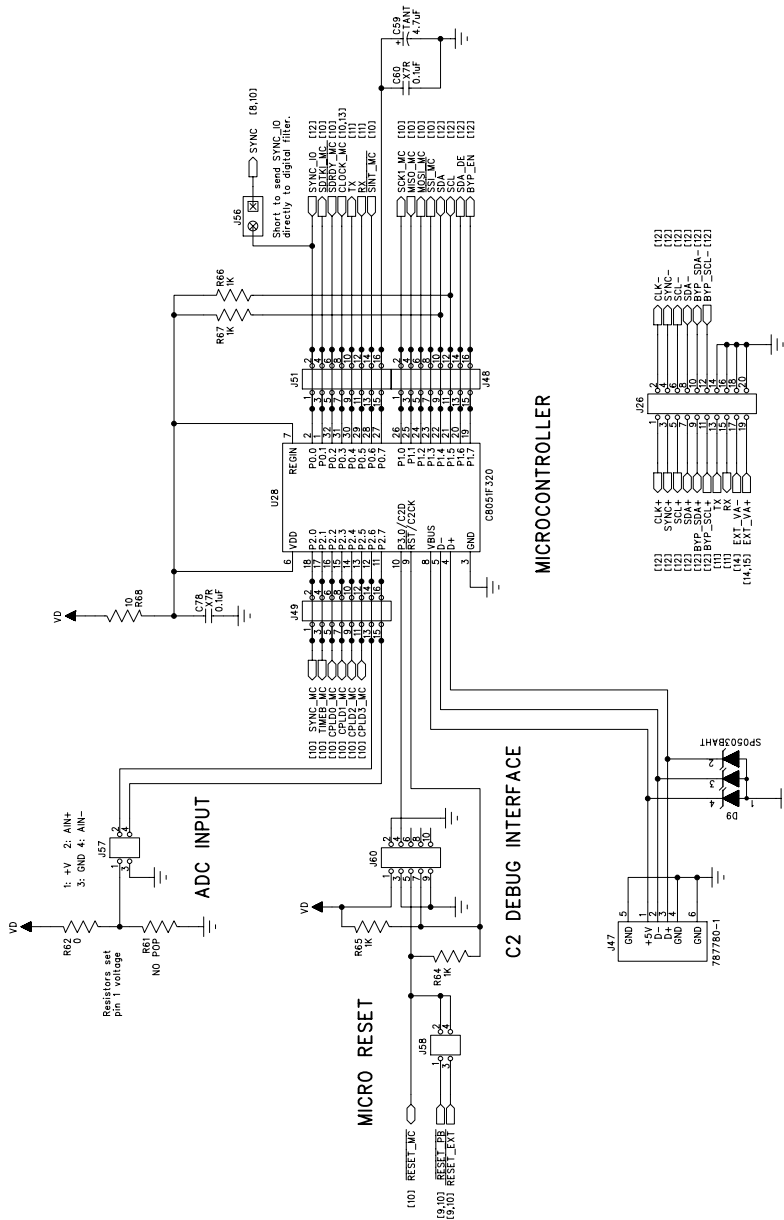
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|--------------|--------------|--------|----------------|
| PART #       | 600-00018-01 | REV    | D1             |
| SHEET TITLE: | XILINX CPLD  |        |                |
| DATE:        | 11/08/2004   | SIZE B | SHEET 10 OF 15 |

XILINX CPLD

JTAG PROGRAMMING PORT

**MICROCONTROLLER SIGNALS**

- SYNC\_MC: synchronization output
- TIMEB\_MC: time break output
- CPLO\_MC: General purpose digital to CPLD
- AIN: analog input to microcontroller ADC
- CZB: debugger data input / output
- CZCK: debugger clock input
- RESET\_MC: microcontroller reset output / input
- VBUS: USB power connection
- D: USB differential data transceiver
- SYNC: raw synchronization output to CS5376A
- SYNC\_ID: synchronization input from RS485
- SDTRD\_MC: serial data taken output
- SDRDY\_MC: serial data ready input
- CLOCK\_MC: microcontroller clock input
- TX: UART transmit
- RX: UART receive
- SINT\_MC: serial acknowledge input
- SKL\_MC: serial clock
- MISO\_MC: serial data
- MOSI\_MC: serial data
- SSL\_MC: serial chip select output
- SDA: I2C data to/from RS485
- SCL: I2C clock from RS485
- SDA\_DE: I2C data driver enable
- BYP\_EN: I2C clock / data bypass



**EXTERNAL CONNECTOR**

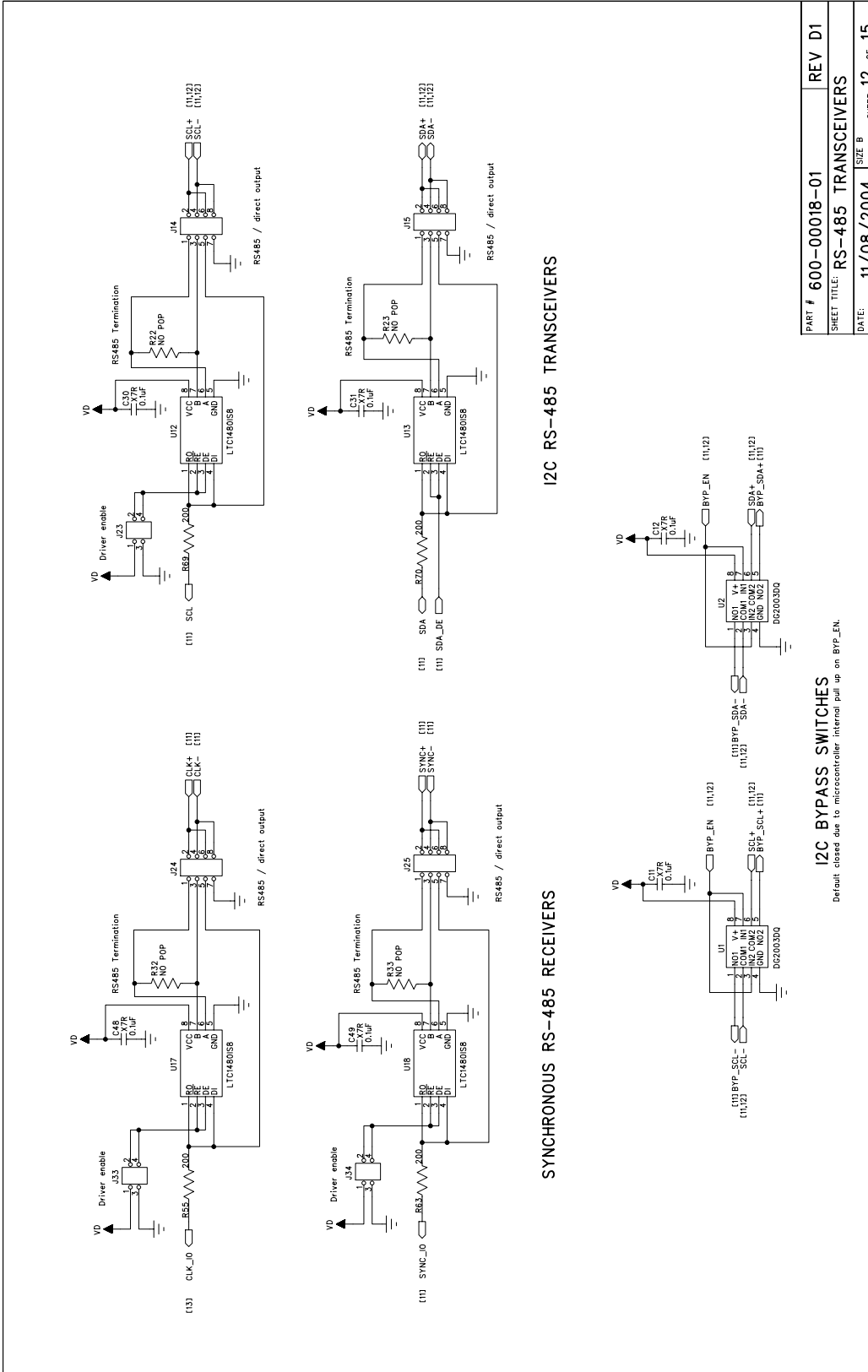
- CLK: synchronous master clock input
- SYNC: synchronous sync signal input
- SCL: I2C clock input / output
- SDA: I2C data input / output
- BYP\_SDA: I2C clock pass through
- BYP\_SCL: I2C data pass through
- TX: UART transmit direct connection
- RX: UART receive direct connection
- EXT\_VA-: negative power supply input
- EXT\_VA+: positive power supply input

**MICROCONTROLLER**

**EXTERNAL CONNECTOR**

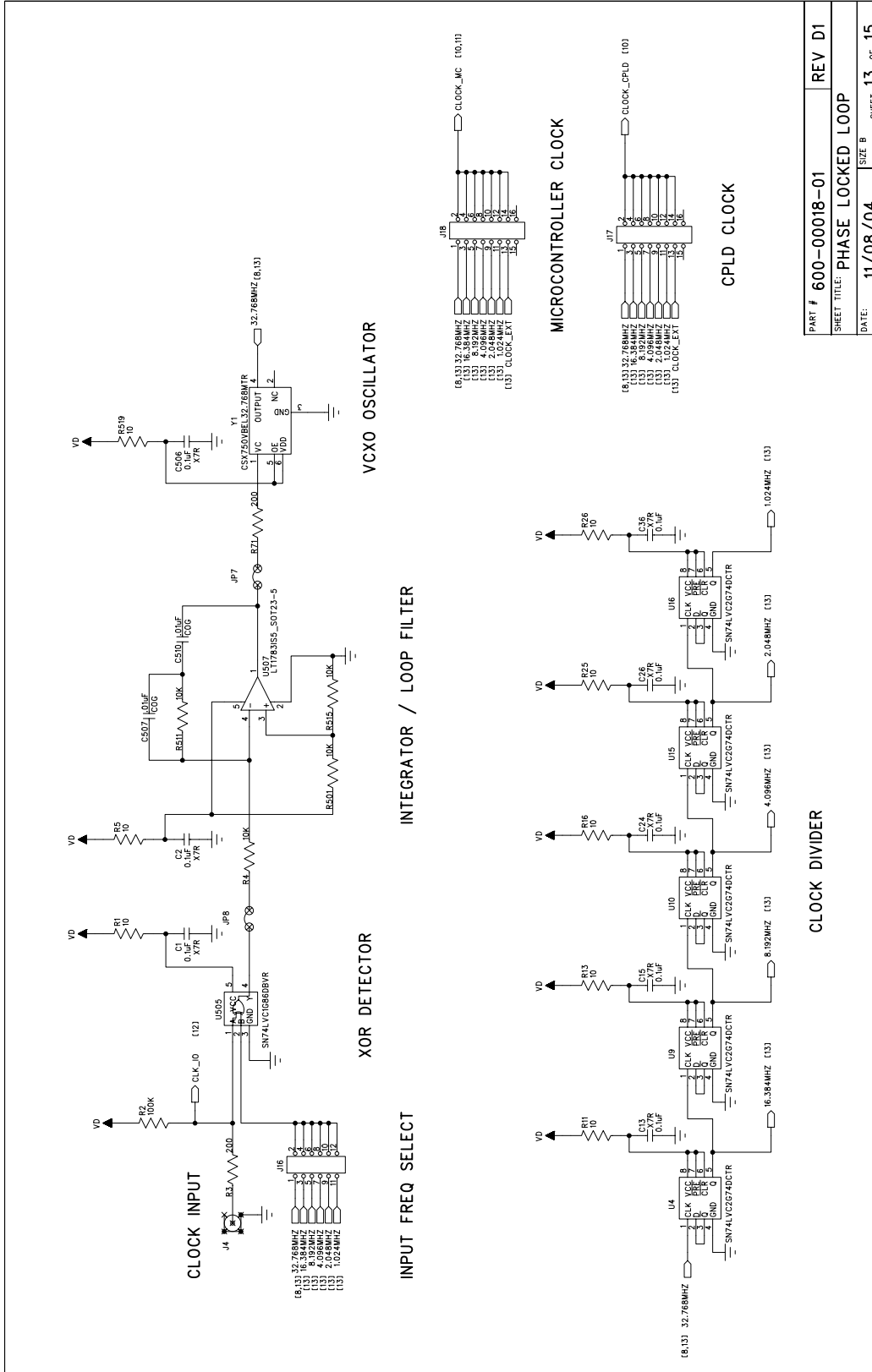
**USB INTERFACE**

|              |                 |       |          |
|--------------|-----------------|-------|----------|
| PART #       | 600-00018-01    | REV   | D1       |
| SHEET TITLE: | MICROCONTROLLER |       |          |
| DATE:        | 11/08/2004      | SHEET | 11 OF 15 |

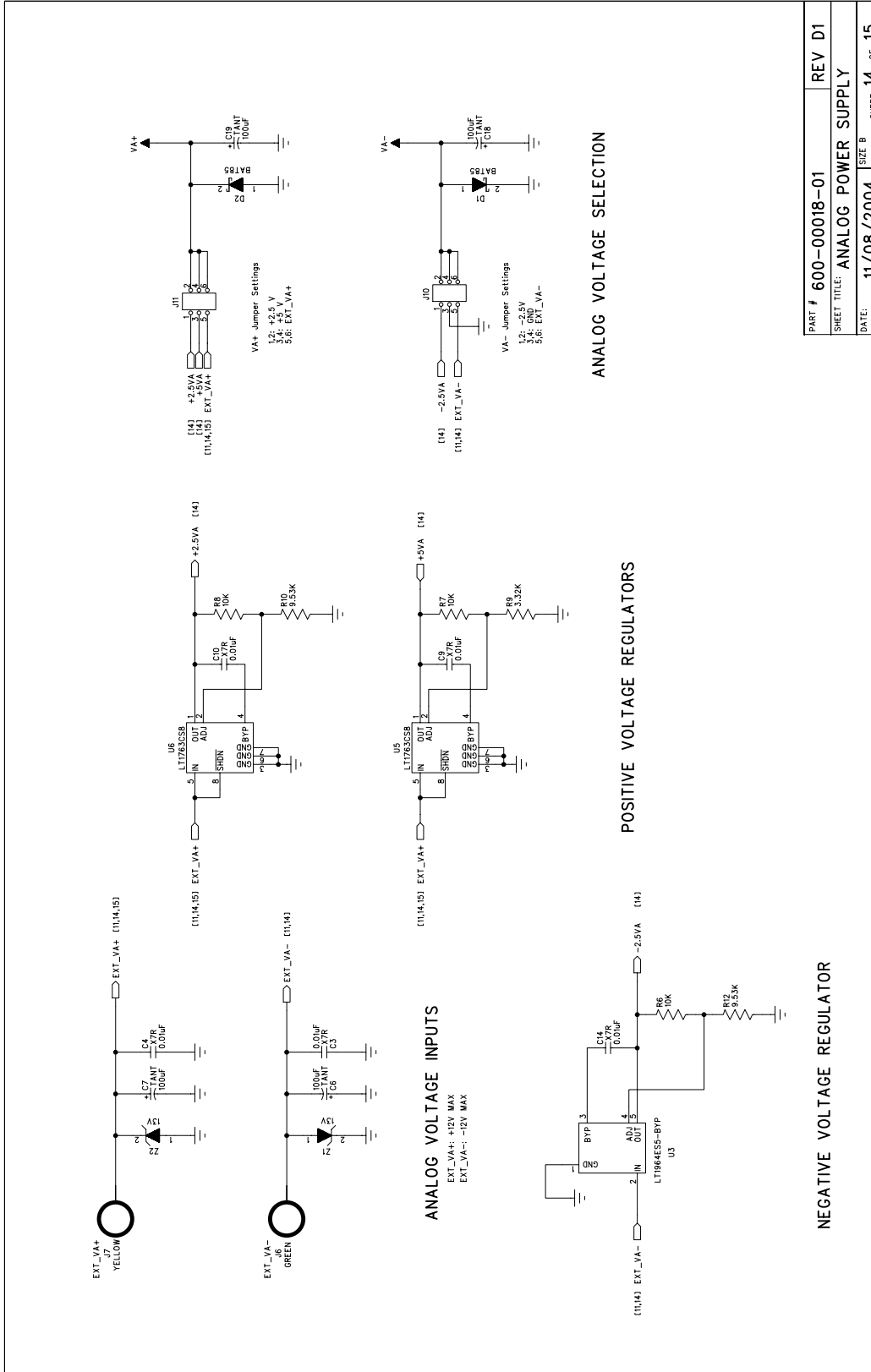


|              |                     |       |          |
|--------------|---------------------|-------|----------|
| PART #       | 600-00018-01        | REV   | D1       |
| SHEET TITLE: | RS-485 TRANSCEIVERS |       |          |
| DATE:        | 11/08/2004          | SIZE  | B        |
|              |                     | SHEET | 12 OF 15 |





|              |                   |       |          |
|--------------|-------------------|-------|----------|
| PART #       | 600-00018-01      | REV   | D1       |
| SHEET TITLE: | PHASE LOCKED LOOP |       |          |
| DATE:        | 11/08/04          | SIZE  | B        |
|              |                   | SHEET | 13 OF 15 |



|              |                     |       |          |
|--------------|---------------------|-------|----------|
| PART #       | 600-00018-01        | REV   | D1       |
| SHEET TITLE: | ANALOG POWER SUPPLY |       |          |
| DATE:        | 11/08/2004          | SIZE  | B        |
|              |                     | SHEET | 14 OF 15 |

