

# 2N4921, 2N4922, 2N4923

2N4923 is a Preferred Device

## Medium-Power Plastic NPN Silicon Transistors

These high-performance plastic devices are designed for driver circuits, switching, and amplifier applications.

### Features

- Low Saturation Voltage –  $V_{CE(sat)} = 0.6 \text{ Vdc (Max) @ } I_C = 1.0 \text{ A}$
- Excellent Power Dissipation Due to Thermopad Construction –  $P_D = 30 \text{ W @ } T_C = 25^\circ\text{C}$
- Excellent Safe Operating Area
- Gain Specified to  $I_C = 1.0 \text{ A}$
- Complement to PNP 2N4918, 2N4919, 2N4920
- Pb-Free Packages are Available\*

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	2N4921 2N4922 2N4923	$V_{CEO}$ 40 60 80	Vdc
Collector-Emitter Voltage	2N4921 2N4922 2N4923	$V_{CB}$ 40 60 80	Vdc
Emitter Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current – Continuous (Note 1)	$I_C$	1.0 3.0	Adc
Base Current – Continuous	$I_B$	1.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	30 0.24	W mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS (Note 2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$\theta_{JC}$	4.16	$^\circ\text{C/W}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. The 1.0 A maximum  $I_C$  value is based upon JEDEC current gain requirements. The 3.0 A maximum value is based upon actual current handling capability of the device (see Figures 5 and 6).
2. Recommend use of thermal compound for lowest thermal resistance.

\*Indicates JEDEC Registered Data.

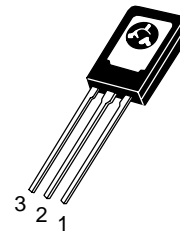
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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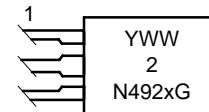
<http://onsemi.com>

**1.0 AMPERE  
GENERAL PURPOSE  
POWER TRANSISTORS  
40–80 VOLTS, 30 WATTS**



**TO-225  
CASE 77  
STYLE 1**

### MARKING DIAGRAM



Y = Year  
WW = Work Week  
2N492x = Device Code  
x = 1, 2, or 3  
G = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping
2N4921	TO-225	500 Units / Box
2N4921G	TO-225 (Pb-Free)	500 Units / Box
2N4922	TO-225	500 Units / Box
2N4922G	TO-225 (Pb-Free)	500 Units / Box
2N4923	TO-225	500 Units / Box
2N4923G	TO-225 (Pb-Free)	500 Units / Box

**Preferred** devices are recommended choices for future use and best overall value.

## 2N4921, 2N4922, 2N4923

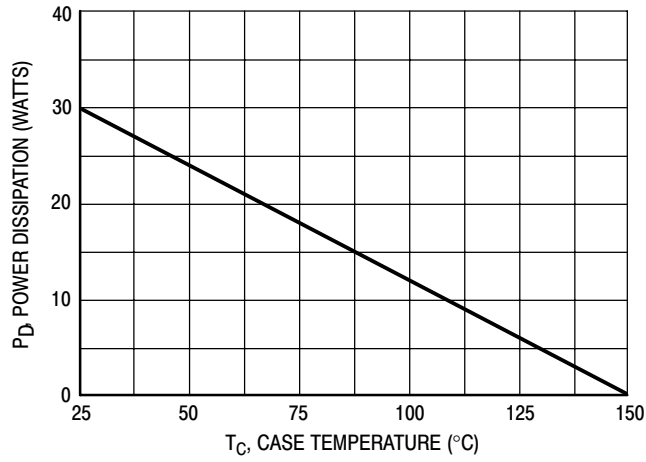
### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Sustaining Voltage (Note 3) ( $I_C = 0.1 \text{ Adc}$ , $I_B = 0$ )	$V_{CE(sus)}$	40 60 80	– – –	Vdc
Collector Cutoff Current ( $V_{CE} = 20 \text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 30 \text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 40 \text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	– – –	0.5 0.5 0.5	mAdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{EB(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{EB(off)} = 1.5 \text{ Vdc}$ , $T_C = 125^\circ\text{C}$ )	$I_{CEX}$	– –	0.1 0.5	mAdc
Collector Cutoff Current ( $V_{CB} = \text{Rated } V_{CB}$ , $I_E = 0$ )	$I_{CBO}$	–	0.1	mAdc
Emitter Cutoff Current ( $V_{EB} = 5.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	1.0	mAdc
<b>ON CHARACTERISTICS</b>				
DC Current Gain (Note 3) ( $I_C = 50 \text{ mAdc}$ , $V_{CE} = 1.0 \text{ Vdc}$ ) ( $I_C = 500 \text{ mAdc}$ , $V_{CE} = 1.0 \text{ Vdc}$ ) ( $I_C = 1.0 \text{ Adc}$ , $V_{CE} = 1.0 \text{ Vdc}$ )	$h_{FE}$	40 30 10	– 150 –	–
Collector-Emitter Saturation Voltage (Note 3) ( $I_C = 1.0 \text{ Adc}$ , $I_B = 0.1 \text{ Adc}$ )	$V_{CE(sat)}$	–	0.6	Vdc
Base-Emitter Saturation Voltage (Note 3) ( $I_C = 1.0 \text{ Adc}$ , $I_B = 0.1 \text{ Adc}$ )	$V_{BE(sat)}$	–	1.3	Vdc
Base-Emitter On Voltage (Note 3) ( $I_C = 1.0 \text{ Adc}$ , $V_{CE} = 1.0 \text{ Vdc}$ )	$V_{BE(on)}$	–	1.3	Vdc
<b>SMALL-SIGNAL CHARACTERISTICS</b>				
Current-Gain – Bandwidth Product ( $I_C = 250 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ MHz}$ )	$f_T$	3.0	–	MHz
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f = 100 \text{ kHz}$ )	$C_{ob}$	–	100	pF
Small-Signal Current Gain ( $I_C = 250 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ kHz}$ )	$h_{fe}$	25	–	–

3. Pulse Test:  $PW \approx 300 \mu\text{s}$ , Duty Cycle  $\approx 2.0\%$ .

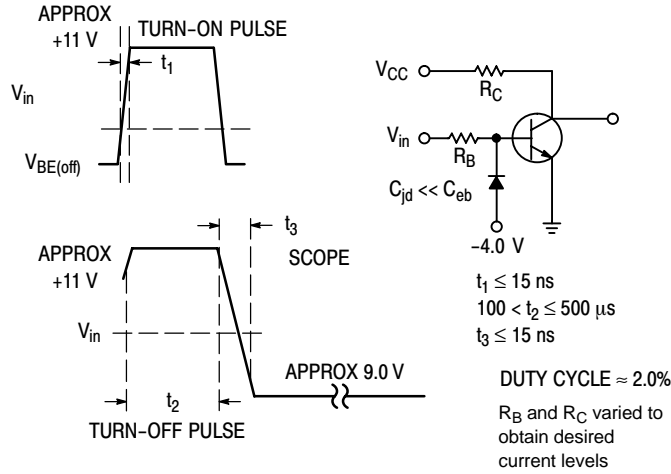
\*Indicates JEDEC Registered Data.

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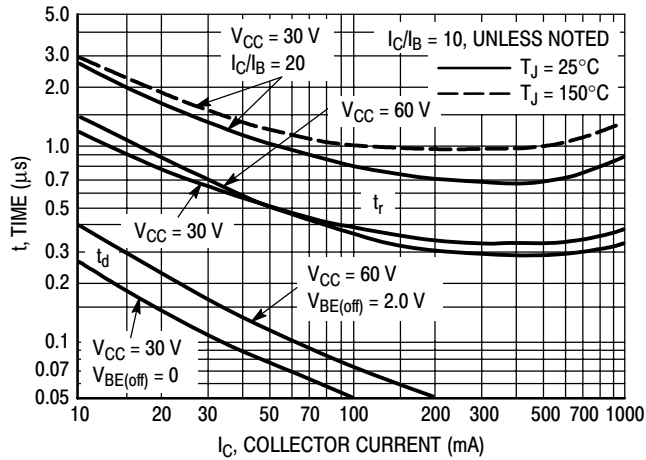


**Figure 1. Power Derating**

Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



**Figure 2. Switching Time Equivalent Circuit**



**Figure 3. Turn-On Time**

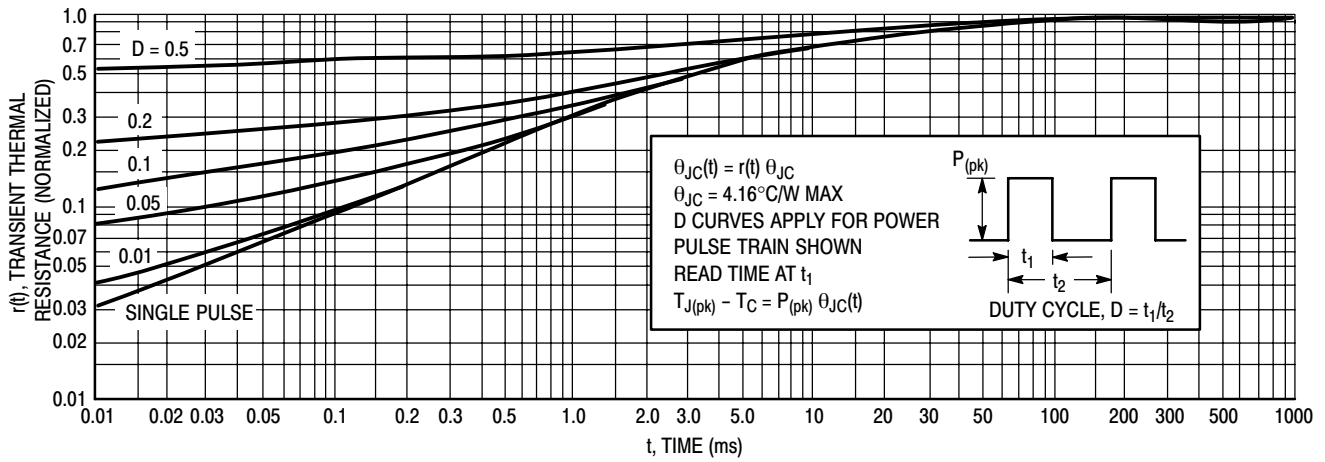


Figure 4. Thermal Response

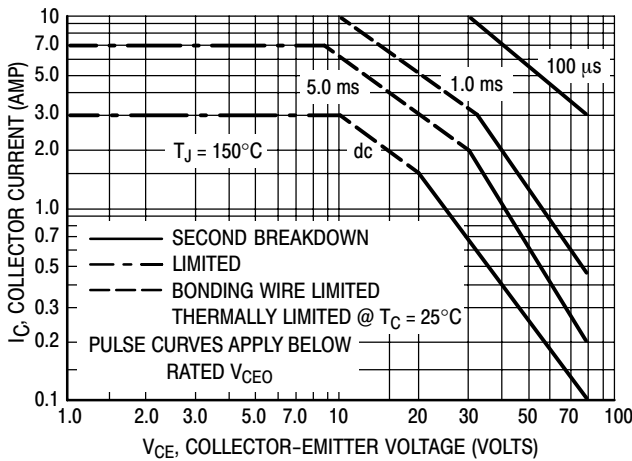


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

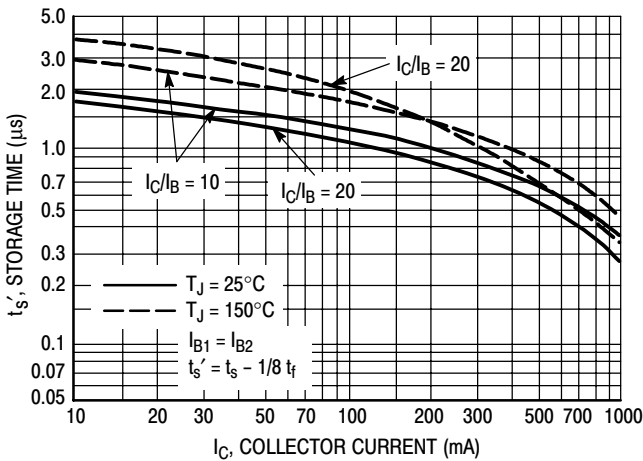


Figure 6. Storage Time

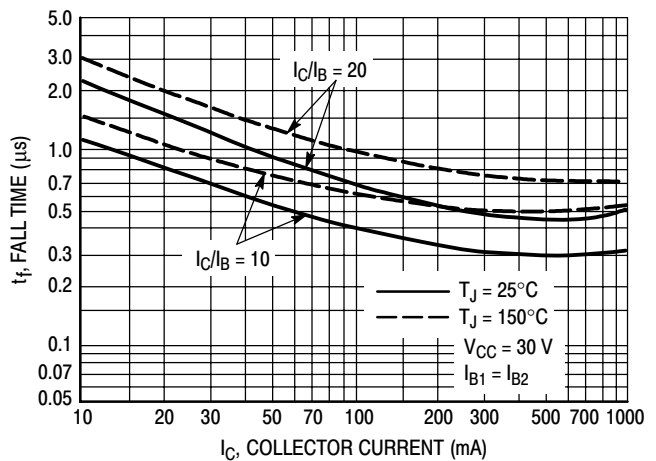


Figure 7. Fall Time

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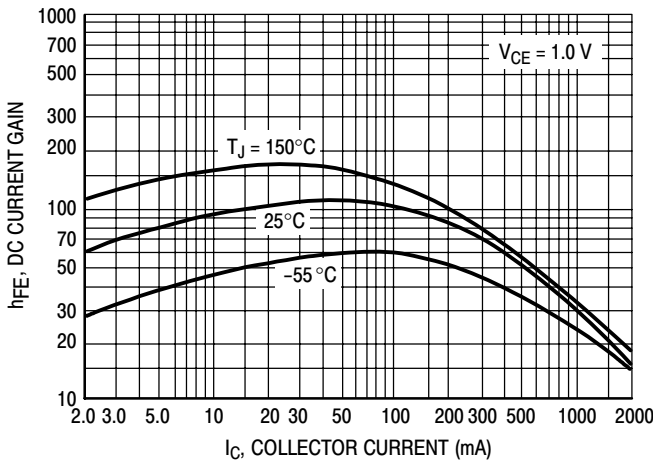


Figure 8. Current Gain

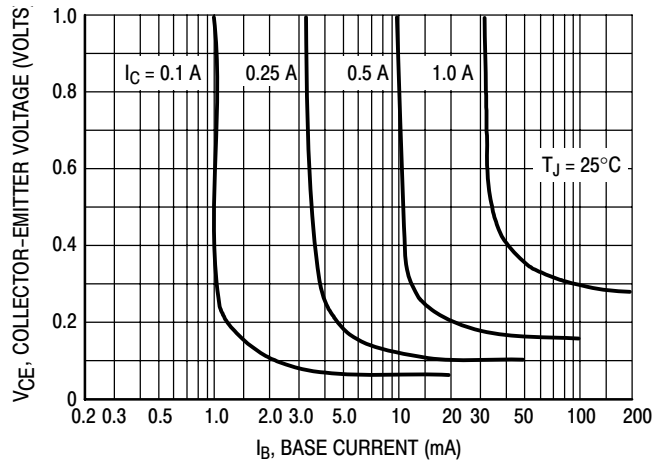


Figure 9. Collector Saturation Region

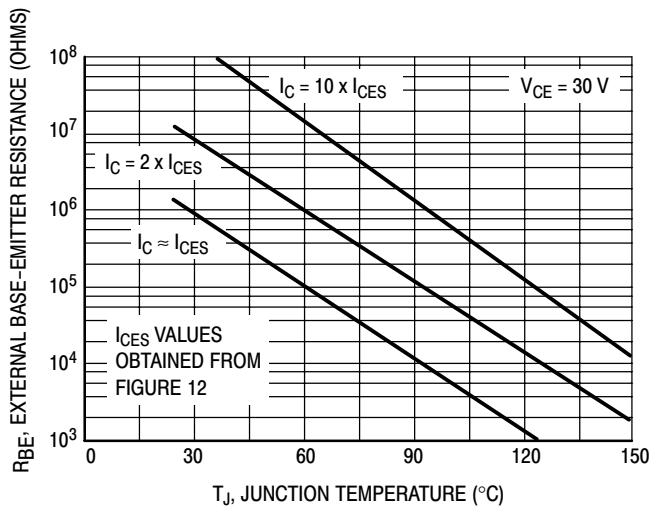


Figure 10. Effects of Base-Emitter Resistance

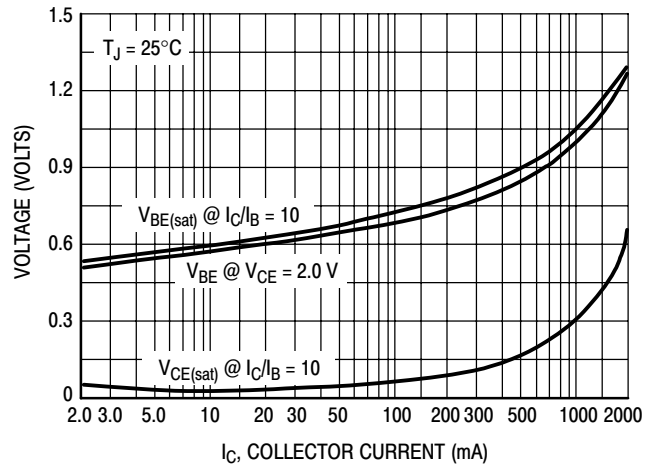


Figure 11. "On" Voltage

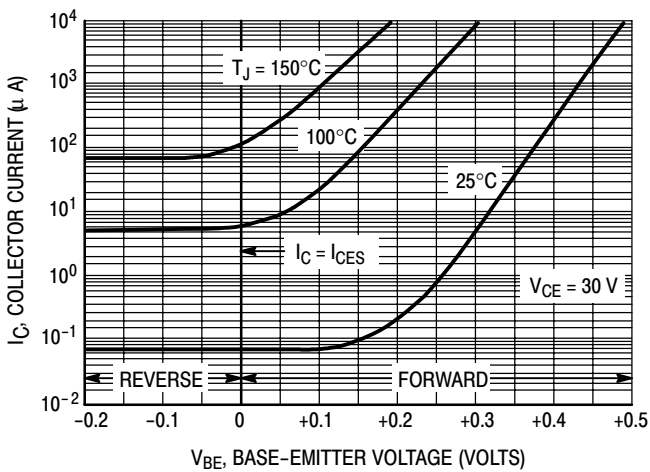


Figure 12. Collector Cut-Off Region

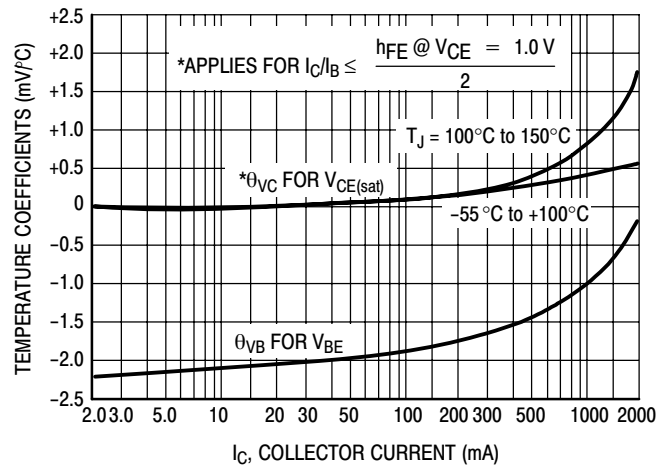
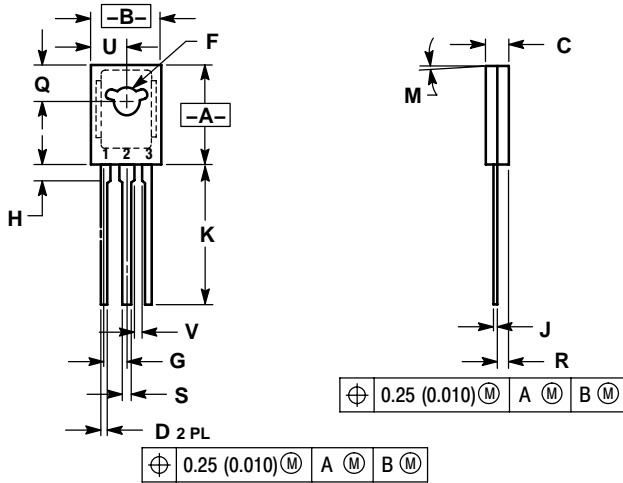


Figure 13. Temperature Coefficients

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## PACKAGE DIMENSIONS

TO-225  
CASE 77-09  
ISSUE Z



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 077-01 THRU -08 OBSOLETE, NEW STANDARD 077-09.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	---	1.02	---

### STYLE 1:

1. EMITTER
2. COLLECTOR
3. BASE

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