

Features

- Programmable AVR® 8-bit Flash Microcontroller Transmitter IC
- Frequency: 315 MHz (ATA6285) and 433 MHz (ATA6286)
- Support ASK/FSK Modulation with Integrated FSK Switch
- 6 dBm Output Power with Typically 8.5 mA Active Current Consumption in Transmission Mode
- Low-power Microcontroller Requires Typically 0.6 µA Sleep Current with Active Interval Timer
- Interfaces for Simple Capacitive Sensors (2 pF to 6 pF)
- One Interface Can Be Configured for Motion Wake-up (3 pF to 5 pF)
- Typically 25 mbar ADC Resolution for Pressure Measurement with Dedicated Sensor Type
- Low-power Measurement Mode for Directly Connected Capacitive Sensors Typically 200 µA at 1 MHz System Clock
- Programmable 125 kHz Wake-up Receiver Channel with Typically 1.7 µA Current Consumption in Listening Mode
- 2V to 3.6V Operation Voltage for Single Li-cell Power Supply
- -40°C to +125°C Operation Temperature and -40°C to +150°C Storage Temperature
- Less than 10 External Passive Components
- QFN32 (5 mm × 5 mm) Package

1. Description

ATA6285 and ATA6286 are highly integrated smart RF micro transmitter ICs for 315 MHz and 433 MHz, suited for ASK and FSK with typically 20 Kbits/s data rate in Manchester mode. The devices combine the functionality of the RF transmitter ICs ATA5756/ATA5757 with the programmable low-power AVR 8-bit Flash microcontroller in a single QFN32 package (5 mm × 5 mm). The ATA6285 and ATA6286 include a dedicated ADC interface for simple capacitive sensors as well as an on-chip temperature sensor. Three sensor interfaces are available for a capacitive range of 2 pF to 16 pF, where one channel can be configured as motion wake-up in the range of 3 pF to 5 pF. The ICs are suited for use in tire pressure monitoring (TPMS) sensor gauges in combination with external sensor devices.

The programmable AVR 8-bit Flash microcontroller includes 8 Kbytes of in-system self-programmable Flash memory and an 320-Bytes EEPROM, thus allowing the system integrator to install field-programmable firmware to enable system flexibility on different platforms. ATA6285 and ATA6286 can be configured to guarantee extremely low power consumption in sleep mode and measurement mode. They also include a programmable 125 kHz wake-up receiver channel for extremely low current consumption in listening mode. The ICs are designed for use in applications with typically less than 10 passive components: one external crystal for the sensor gauge, several capacitors, a single LiMnO₂ battery coin cell, a single-ended antenna for the data transmission and an LF ferrite coil for the wake-up channel. ATA6285 and ATA6286 support TPMS-specific low-current modes even with an active brown-out detection and an interval timer.



TPMS Control and Transmitter IC

ATA6285
ATA6286

Summary

Preliminary

NOTE: This is a summary document. The complete document is available under NDA. For more information, please contact your local Atmel sales office.

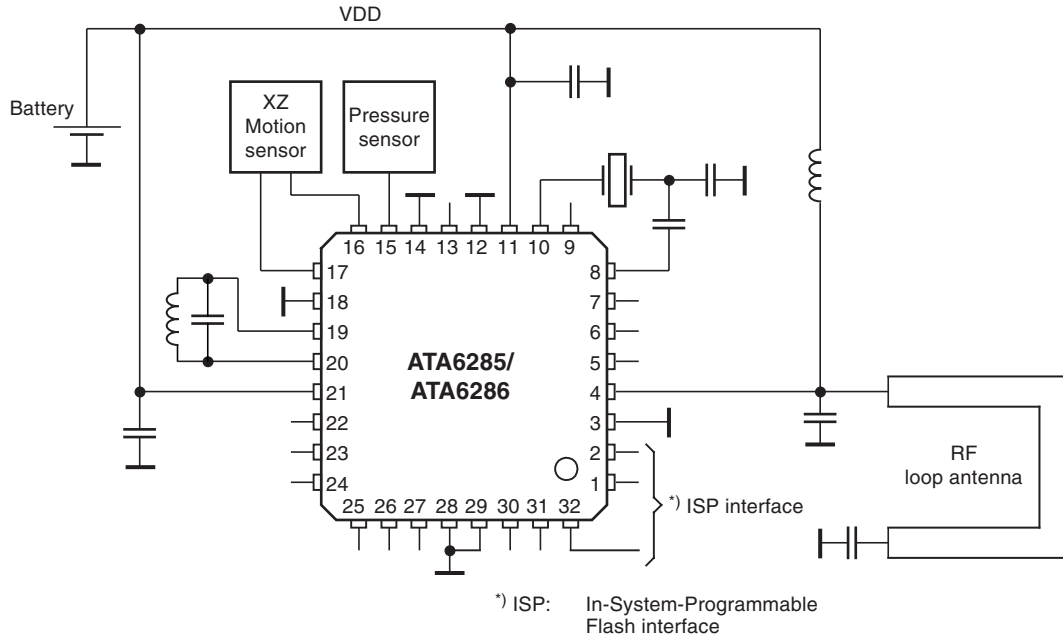
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2. Overview

2.1 Application

Figure 2-1. Tire Pressure Monitoring System (TPMS)



Crystal Frequency 13.56 MHz for 433 MHz application

Crystal Frequency 13.125 MHz for 315 MHz application

2.4 Pin Configuration

Figure 2-3. Pinning QFN32

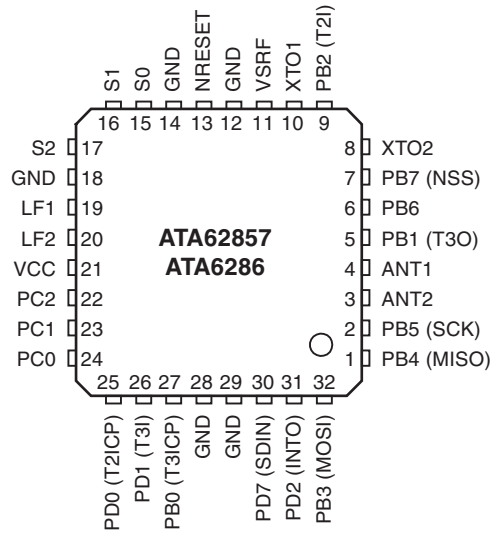


Table 2-2. Pin Description

| Pin Number | Pin Name | Alternate Function 1 | Alternate Function 2 | Function | Comment |
|------------|----------|----------------------|----------------------|---|---------|
| 1 | PB4 | MISO | PCINT4 | SPI | Port B4 |
| 2 | PB5 | SCK | PCINT5 | SPI | Port B5 |
| 3 | ANT2 | – | – | RF-antenna 2. Emitter of antenna output stage | RF pin |
| 4 | ANT1 | – | – | RF-antenna 1. Open collector antenna output | RF pin |
| 5 | PB1 | T3O | PCINT1 | Timer3 output | Port B1 |
| 6 | PB6 | – | PCINT6 | | Port B6 |
| 7 | PB7 | NSS | PCINT7 | SPI | Port B7 |
| 8 | XT02 | – | – | Switch for FSK modulation | RF pin |
| 9 | PB2 | T2I | PCINT2 | Timer2 external input clock | Port B2 |
| 10 | XT01 | – | – | Connection for crystal | RF pin |
| 11 | VS_RF | – | – | Power supply voltage for RF | RF pin |
| 12 | GND | – | – | Power supply ground for RF | RF pin |
| 13 | NRESET | debugWIRE | – | Reset input/debugWIRE interface | |
| 14 | GND | – | – | Power supply ground | |
| 15 | S0 | – | – | Sensor input 0 – Pressure Sensor (Cap.) | |
| 16 | S1 | – | – | Sensor input 1 – X – Motion Sensor (Cap.) | |
| 17 | S2 | – | – | Sensor input 2 – Z – Motion Sensor (Cap.) | |
| 18 | GND | – | – | Power supply ground | |

Note: 1. Internal inter-die connection of the MCP

Table 2-2. Pin Description (Continued)

| Pin Number | Pin Name | Alternate Function 1 | Alternate Function 2 | Function | Comment |
|--------------------------|-----------------|----------------------|----------------------|--|---------|
| 19 | LF1 | – | – | LF-receiver input 1 | |
| 20 | LF2 | – | – | LF-receiver input 2 | |
| 21 | V _{CC} | – | – | Power supply voltage (V _{CC} + AV _{CC}) | |
| 22 | PC2 | – | PCINT10 | - | Port C2 |
| 23 | PC1 | CLKO | PCINT9 | System clock output | Port C1 |
| 24 | PC0 | ECIN0 | PCINT8 | External Clock input 0 | Port C1 |
| 25 | PD0 | T2ICP | PCINT16 | Timer2 external input capture | Port D0 |
| 26 | PD1 | T3I | PCINT17 | Timer3 external input clock | Port D1 |
| 27 | PB0 | T3ICP | PCINT0 | Timer3 external input capture | Port B0 |
| 28 | GND | – | – | Power supply ground | |
| 29 | GND | – | – | Power supply ground | |
| Inter-die ⁽¹⁾ | PD3 | INT1 | PCINT19 | External Interrupt 1 → Inter-die connection | Port D2 |
| Inter-die ⁽¹⁾ | PD4 | ECIN1 | PCINT20 | External Clock input 1 → Inter-die connection | Port D4 |
| Inter-die ⁽¹⁾ | PD5 | T2O1 | PCINT21 | Timer2 Modulator output 1 → Inter-die connection | Port D5 |
| Inter-die ⁽¹⁾ | PD6 | T2O2 | PCINT22 | Timer2 Modulator output 2 → Inter-die connection | Port D6 |
| 30 | PD7 | SDIN | PCINT23 | SSI –Serial Data Input | Port D7 |
| 31 | PD2 | INT0 | PCINT18 | External interrupt input 0 | Port D2 |
| 32 | PB3 | MOSI | PCINT3 | SPI | Port B3 |

Note: 1. Internal inter-die connection of the MCP

2.5 Pin Names

2.5.1 VCC

Supply voltage

2.5.2 GND

Ground

2.5.3 Port B (PB7..0)

Port B is a 5(8)-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The PB7, PB6 and PB2 ports are only used as internal I/O ports for inter-die connections. The Port B output buffers have symmetrical drive characteristics with both high sink and source current capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmegaT.

2.5.4 Port C (PC2..0)

Port C is a 3-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source current capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

2.5.5 Port D (PD7..0)

Port D is a 7(1)-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The PD(6..3) pins are used as internal inter-die connection I/O ports. The Port D output buffers have symmetrical drive characteristics with both high sink and source current capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmegaT.

2.5.6 NRESET

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. Shorter pulses than defined minimum pulse length are not guaranteed to generate a reset.

2.5.7 LF (2..1)

Input coil pins for the LF-Receiver.

2.5.8 S (2..0)

Measuring input pins for external capacitance sensor elements.

2.5.9 ANT(2, 1)

RF-Antenna pins.

2.5.10 XTO(0, 1)

External crystal for the internal RF transmitter IC.

3. Low Power AVR 8-bit Microcontroller

3.1 Features

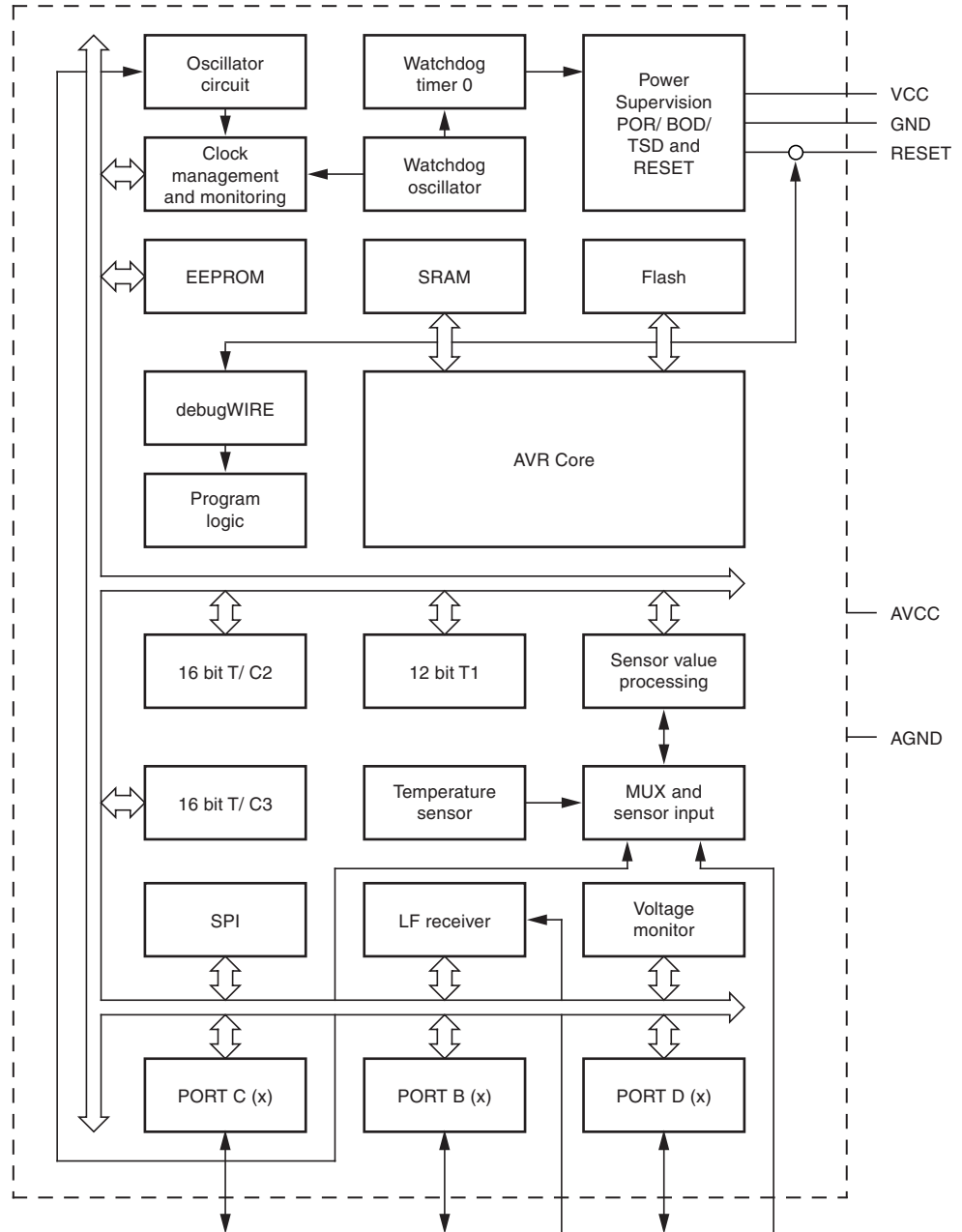
- **High Performance, Extremely Low Power AVR 8-bit Microcontroller**
- **Advanced RISC Architecture**
 - 131 Powerful Instructions
 - 32 × 8 General Purpose Working Registers
 - Fully Static Operation
 - On-chip 2-cycle Multiplier
- **Non-volatile Program and Data Memories**
 - 8 Kbytes of In-system Self-programmable Flash
 - Optional Boot Code Section with Independent Lock Bits
 - 320 (256 + 64) Bytes EEPROM
 - 512 Bytes Internal SRAM
 - Programming Lock for Software Security
- **Peripheral Features**
 - Programmable Watchdog/Interval Timer with Separate, Internally Calibrated and Extremely Low-power Oscillator
 - Two 16-bit Timer/Counter with Compare Mode, Capture Mode, and On-chip Digital Data Modulator Circuitry
 - Integrated On-chip Temperature Sensor with Thermal Shutdown Function
 - Sensor Interface for External Pressure Sensor and XZ- Motion Sensor
 - Highly Sensitive 1D LF-receiver
 - Programmable Voltage Monitor
 - System Clock Management and Clock Monitoring
 - Master/Slave SPI Serial Interface
 - Integrated Debug-Wire-Interface
 - Interrupt and Wake-up on Pin Change
- **Special Microcontroller Features**
 - Power-on Reset and Programmable Brown-out Detection
 - Internal Calibrated RC Oscillator
 - External and Internal Interrupt Sources
 - Three Sleep Modes: Idle, Sensor Noise Reduction, and Power-down
- **I/O and Package**
 - 15 Programmable I/O Lines

3.2 Overview

The embedded core is an extremely low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the AVR core achieves throughputs approaching 1 MIPS per MHz allowing the designer to optimize power consumption versus processing speed.

3.3 Block Diagram

Figure 3-1. Microcontroller Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The embedded architecture provides the following features: 8K bytes of In-System Programmable Flash with Read-While-Write capabilities, 320 (256 + 64) bytes EEPROM, 512 bytes SRAM, 11(19) general purpose I/O lines, 32 general purpose working registers, On-chip Debugging support and programming, two flexible Timer/Counters with compare modes, internal and external interrupts, a sensor interface for external pressure sensor and Acceleration/Motion sensor, a programmable Watchdog Timer with internal calibrated Oscillator, an SPI serial port, and three software selectable power saving modes.

The device is manufactured using Atmel[®]'s high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip Boot program running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmegaT is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation Kits.



4. UHF ASK/FSK Transmitter for ATA6285/ATA6286

4.1 Features

- PLL Transmitter IC with Single-ended Output
- High output Power (6 dBm) at 8.1 mA (315 MHz) and 8.5 mA (433 MHz) Typical Values
- Divide by 24 (ATA6285) and 32 (ATA6286) Blocks for 13 MHz Crystal Frequencies and for Low XTO Start-up Times
- Modulation Scheme ASK/FSK with Internal FSK Switch
- Up to 20 Kbits/s Manchester Coding, Up to 40 Kbits/s NRZ Coding
- Power-down Idle and Power-up Modes to Adjust Corresponding Current Consumption through ASK/FSK/Enable Input Pins
- ENABLE Input for Parallel Usage of Controlling Pins in a 3-wire Bus System
- CLK Output Switches ON if the Crystal Current Amplitude Has Reached 35% to 80% of its Final Value
- Crystal Oscillator Time until CLK Output Is Activated, Typically 0.6 ms

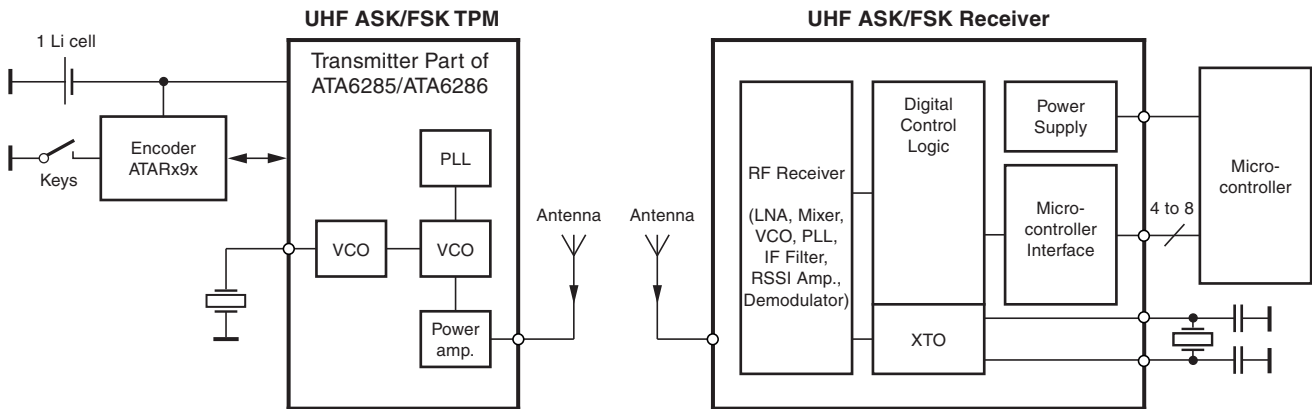
4.2 Benefits

- Low Parasitic FSK Switch Integrated
- Very Short and Reproducible Time to Transmit Typically < 0.85 ms
- 13.125 MHz/13.56 MHz Crystals Give Opportunity for Small Package Sizes

4.3 Description

The ATA6285/ATA6286 is a PLL transmitter part which has been developed for the demands of RF low-cost transmission systems at data rates up to 20 Kbits/s Manchester coding and 40 Kbits/s NRZ coding. The transmitting frequency range is 313 MHz to 317 MHz (ATA6285) and 432 MHz to 448 MHz (ATA6286), respectively. It can be used in both FSK and ASK systems. Due to its shortened crystal oscillator settling time it is well suited for Tire Pressure Monitoring (TPMS) and for Passive Entry Go applications.

Figure 4-1. System Block Diagram



4.4 General Description

This fully integrated PLL transmitter allows the design of simple, low-cost RF miniature transmitters for TPM and RKE applications. The VCO is locked to $24 \times f_{XTAL}/32 \times f_{XTAL}$ for ATA6285/ATA6286. Thus, a 13.125 MHz/13.56 MHz crystal is needed for a 315 MHz/433.92 MHz transmitter. All other PLL and VCO peripheral elements are integrated.

The XTO is a series resonance (current mode) oscillator. Only one capacitor and a crystal connected in series to GND are needed as external elements in an ASK system. The internal FSK switch, together with a second capacitor, can be used for FSK modulation. The crystal oscillator needs typically 0.6 ms until the CLK output is activated if a crystal as defined in the electrical characteristics is used (e.g., TPM crystal). For most crystals used in RKE systems, a shorter time will result.

The CLK output is switched on if the amplitude of the current flowing through the crystal has reached 35% to 80% of its final value. This is synchronized with the 1.64 MHz/1.69 MHz CLK output. As a result, the first period of the CLK output is always a full period. The PLL is then locked $< 250 \mu\text{s}$ after CLK output activation. This means an additional wait time of $\geq 250 \mu\text{s}$ is necessary before the PA can be switched on and the data transmission can start. This results in a significantly lower time of about 0.85 ms between enabling the ATA6285/ATA6286 and the beginning of the data transmission which saves battery power especially in tire pressure monitoring systems.

The power amplifier is an open-collector output delivering a current pulse which is nearly independent from the load impedance and therefore the output power can be controlled via the connected load impedance.

This output configuration enables a simple matching to any kind of antenna or to 50Ω . A high power efficiency for the power amplifier results if an optimized load impedance of $Z_{\text{Load, opt}} = 380\Omega + j340\Omega$ (ATA6285) at 315 MHz and $Z_{\text{Load, opt}} = 280\Omega + j310\Omega$ (ATA6286) at 433.92 MHz is used at the 3V supply voltage.

4.5 Functional Description

If ASK = Low, FSK = Low and ENABLE = open or Low, the circuit is in power-down mode consuming only a very small amount of current so that a lithium cell used as power supply can work for many years.

If the ENABLE pin is left open, ENABLE is the logical OR operation of the ASK and FSK input pins. This means, the IC can be switched on by either the FSK or the ASK input.

If the ENABLE pin is Low and ASK or FSK are High, the IC is in idle mode where the PLL, XTO and power amplifier are off and the microcontroller ports controlling the ASK and FSK inputs can be used to control other devices. This can help to save ports on the microcontroller in systems where other devices with 3-wire interface are used.

With FSK = High and ASK = Low and ENABLE = open or High, the PLL and the XTO are switched on and the power amplifier is off. When the amplitude of the current through the crystal has reached 35% to 80% of its final amplitude, the CLK driver is automatically activated. The CLK output stays Low until the CLK driver has been activated. The driver is activated synchronously with the CLK output frequency, hence, the first pulse on the CLK output is a complete period. The PLL is then locked within $< 250 \mu\text{s}$ after the CLK driver has been activated, and the transmitter is then ready for data transmission.

With ASK = High the power amplifier is switched on. This is used to perform the ASK modulation. During ASK modulation the IC is enabled with the FSK or the ENABLE pin.

With FSK = Low the switch at pin XTO2 is closed, with FSK = High the switch is open. To achieve a faster start-up of the crystal oscillator, the FSK pin should be High during start-up of the XTO because the series resistance of the resonator seen from pin XTO1 is lower if the switch is off.

The different modes of the ATA6285/ATA6286 are listed in [Table 4-1](#).

Table 4-1. Transmitter Part

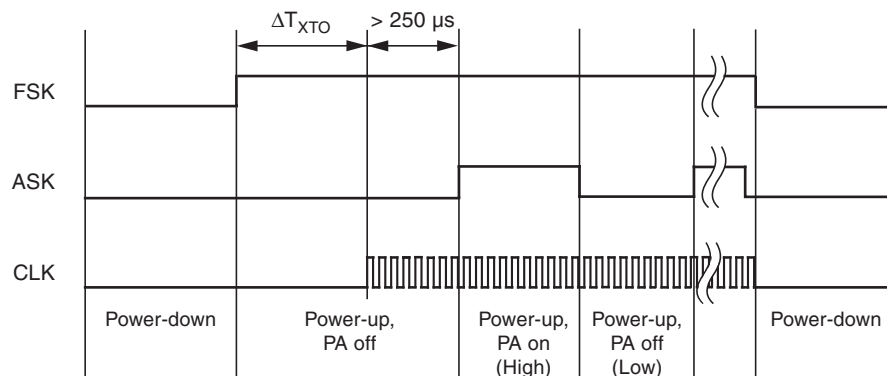
| ASK Pin | FSK Pin | ENABLE Pin | Mode |
|----------|----------|------------|-------------------------------------|
| Low | Low | Low/open | Power-down mode, FSK switch High Z |
| Low | Low | High | Power-up, PA off, FSK switch Low Z |
| Low | High | High/open | Power-up, PA off, FSK switch High Z |
| High | Low | High/open | Power-up, PA on, FSK switch Low Z |
| High | High | High/open | Power-up, PA on, FSK switch High Z |
| Low/High | High | Low | Idle mode, FSK switch High Z |
| High | Low/High | Low | Idle mode, FSK switch High Z |

4.5.1 Transmission with ENABLE = Open

4.5.1.1 ASK Mode

The ATA6285/ATA6286 is activated by ENABLE = open, FSK = High, ASK = Low. The microcontroller is then switched to external clocking. After typically 0.6 ms, the CLK driver is activated automatically (i.e., the microcontroller waits until the XTO and CLK are ready). After another time period of $\leq 250 \mu\text{s}$, the PLL is locked and ready to transmit. The output power can then be modulated by means of pin ASK. After transmission, ASK is switched to Low and the microcontroller returns back to internal clocking. Then, the ATA6285/ATA6286 is switched to power-down mode with FSK = Low.

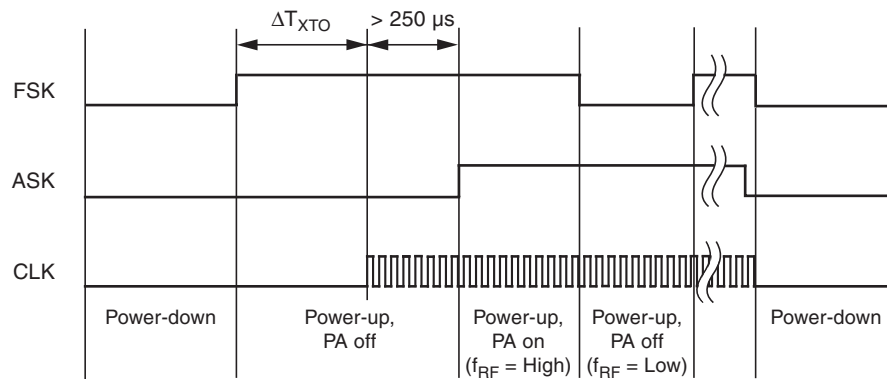
Figure 4-2. Timing ASK Mode with ENABLE Open



4.5.1.2 FSK Mode

The ATA6285/ATA6286 is activated by FSK = High, ASK = Low. The microcontroller is then switched to external clocking. After typically 0.6 ms, the CLK driver is activated automatically (i.e., the microcontroller waits until the XTO and CLK are ready). After another time period of $\leq 250 \mu\text{s}$, the PLL is locked and ready to transmit. The power amplifier is switched on with ASK = H. The ATA6285/ATA6286 is then ready for FSK modulation. The microcontroller starts to switch on and off the capacitor between the crystal load capacitor and GND by means of pin FSK, thus, changing the reference frequency of the PLL. IF FSK = L the output frequency is lower, if FSK = H output frequency is higher. After transmission, FSK stays High and ASK is switched to Low and the microcontroller returns back to internal clocking. Then, the ATA6285/ATA6286 is switched to power-down mode with FSK = Low.

Figure 4-3. Timing FSK Mode with ENABLE Open

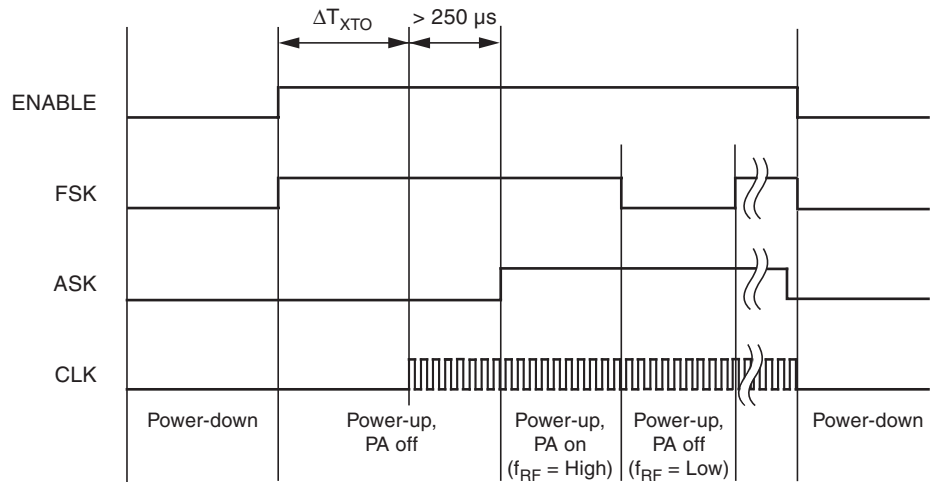


4.5.2 Transmission with ENABLE = High

4.5.2.1 FSK Mode

The ATA6285/ATA6286 is activated by ENABLE = High, FSK = High and ASK = Low. The microcontroller is then switched to external clocking. After typically 0.6 ms, the CLK driver is activated automatically (i.e., the microcontroller waits until the XTO and CLK are ready). After another time period of $\leq 250 \mu\text{s}$, the PLL is locked and ready to transmit. The power amplifier is switched on with ASK = H. The ATA6285/ATA6286 is then ready for FSK modulation. The microcontroller starts to switch on and off the capacitor between the crystal load capacitor and GND by means of pin FSK, thus, changing the reference frequency of the PLL. IF FSK = L the output frequency is lower, if FSK = H output frequency is higher. After transmission, ASK is switched to Low and the microcontroller returns back to internal clocking. Then, the ATA6285/ATA6286 is switched to power-down mode with ENABLE = Low and FSK = Low.

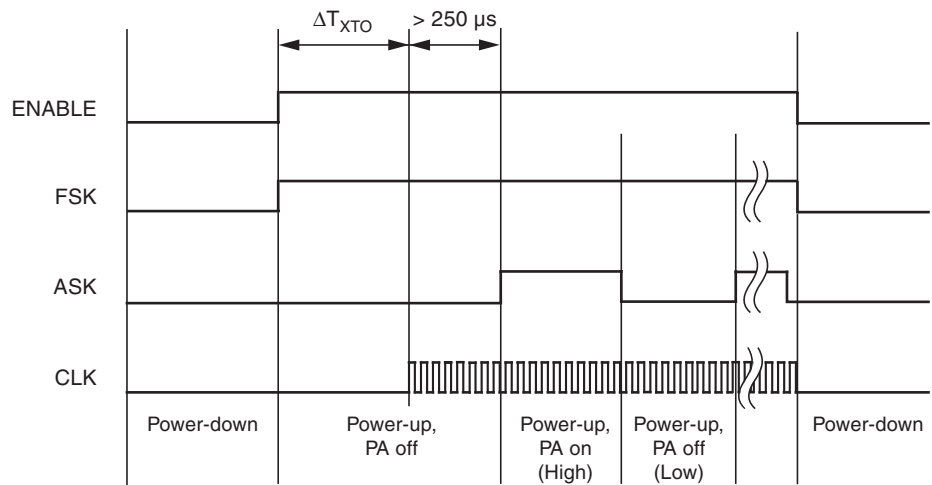
Figure 4-4. Timing FSK Mode with ENABLE Connected to the Microcontroller



4.5.2.2 ASK Mode

The ATA6285/ATA6286 is activated by ENABLE = High, FSK = High and ASK = Low. After activation the microcontroller is switched to external clocking. After typically 0.6 ms, the CLK driver is activated automatically (the microcontroller waits until the XTO and CLK are ready). After another time period of $\leq 250 \mu\text{s}$, the PLL is locked and ready to transmit. The output power can then be modulated by means of pin ASK. After transmission, ASK is switched to Low and the microcontroller returns back to internal clocking. Then, the ATA6285/ATA6286 is switched to power-down mode with ENABLE = Low and FSK = Low.

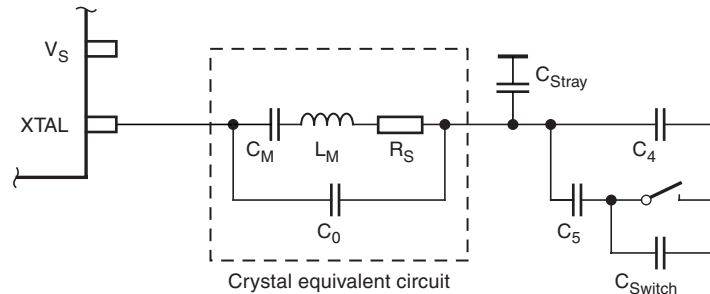
Figure 4-5. Timing ASK Mode with ENABLE Connected to the Microcontroller



4.5.3 Accuracy of Frequency Deviation

The accuracy of the frequency deviation using the XTAL pulling method is about $\pm 20\%$ if the following tolerances are considered. One important aspect is that the values of C_0 and C_M of typical crystals are strongly correlated which reduces the tolerance of the frequency deviation.

Figure 4-6. Tolerances of Frequency Modulation



Using a crystal with a motional capacitance of $C_M = 4.37 \text{ fF} \pm 15\%$, a nominal load capacitance of $CL_{\text{NOM}} = 18 \text{ pF}$ and a parallel capacitance of $C_0 = 1.30 \text{ pF}$ correlated with C_M results in $C_0 = 297 \times C_M$ (the correlation has a tolerance of 10%, so $C_0 = 267$ to $326 \times C_M$). If using the internal FSK switch with $C_{\text{Switch}} = 0.9 \text{ pF} \pm 20\%$ and estimated parasitics of $C_{\text{Stray}} = 0.7 \text{ pF} \pm 10\%$, the resulting C_4 and C_5 values are $C_4 = 10 \text{ pF} \pm 1\%$ and $C_5 = 15 \text{ pF} \pm 1\%$ for a nominal frequency deviation of $\pm 19.3 \text{ kHz}$ with worst case tolerances of $\pm 15.8 \text{ kHz}$ to $\pm 23.2 \text{ kHz}$.

4.5.4 Accuracy of the Center Frequency

The imaginary part of the impedance in large signal steady state oscillation IM_{XTO} , seen into the pin 7 (XTO1), causes some additional frequency tolerances, due to pulling of the XTO oscillation frequency. These tolerances have to be added to the tolerances of the crystal itself (adjustment tolerance, temperature stability and ageing) and the influence to the center frequency due to tolerances of C_4 , C_5 , C_{Switch} and C_{Stray} . The nominal value of $IM_{\text{XTO}} = 110\Omega$, C_{Switch} and C_{Stray} should be absorbed into the C_4 and C_5 values by using a crystal with known frequency and choosing C_4 and C_5 , so that the XTO center frequency equals the crystal frequency, and the frequency deviation is as expected. Then, from the nominal value, the IM_{XTO} has $\pm 90\Omega$ tolerances, using the pulling formula $P = -IM_{\text{XTO}} \times C_M \times \text{Pi} \times f_{\text{XTO}}$ with $f_{\text{XTO}} = 13.56 \text{ MHz}$ and $C_M = 4.4 \text{ fF}$ an additional frequency tolerance of $P = \pm 16.86 \text{ ppm}$ results. If using crystals with other C_M the additional frequency tolerance can be calculated in the same way. For example, a lower $C_M = 3.1 \text{ fF}$ will reduce the frequency tolerance to 11.87 ppm, where a higher $C_M = 5.5 \text{ fF}$ increases the tolerance to 21.07 ppm.

4.5.5 CLK Output

An output CLK signal of 1.64 MHz (ATA6285 operating at 315 MHz) and 1.69 MHz (ATA6286 operating at 433.92 MHz) is provided for a connected microcontroller. The delivered signal is CMOS-compatible with a High and Low time of $>125 \text{ ns}$ if the load capacitance is lower than 20 pF. The CLK output is Low in power-down mode due to an internal pull-down resistor. After enabling the PLL and XTO the signal stays Low until the amplitude of the crystal oscillator has reached 35% to 80% of its amplitude. Then, the CLK output is activated synchronously with its output signal so that the first period of the CLK output signal is a full period.

4.5.5.1 Clock Pulse Take-over by Microcontroller

The clock of the crystal oscillator can be used for clocking the microcontroller. Atmel's ATARx9x microcontroller family provides the special feature of starting with an integrated RC oscillator to switch on the ATA6285/ATA6286 external clocking and to wait automatically until the CLK output of the ATA6285/ATA6286 is activated. After a time period of 250 μ s the message can be sent with crystal accuracy.

4.5.6 Output Matching and Power Setting

The output power is set by the load impedance of the antenna. The maximum output power is achieved with a load impedance of $Z_{Load, opt} = 380\Omega + j340\Omega$ (ATA6286) at 315 MHz and $Z_{Load, opt} = 280\Omega + j310\Omega$ (ATA6285) at 433.92 MHz. A low resistive path to V_S is required to deliver the DC current.

The power amplifier delivers a current pulse and the maximum output power is delivered to a resistive load if the 0.66 pF output capacitance of the power amplifier is compensated by the load impedance.

At the ANT1 pin, the RF output amplitude is about $V_S - 0.5V$.

The load impedance is defined as the impedance seen from the ATA6285's ANT1, ANT2 into the matching network. Do not mix up this large-signal load impedance with a small-signal input impedance delivered as an input characteristic of RF amplifiers.

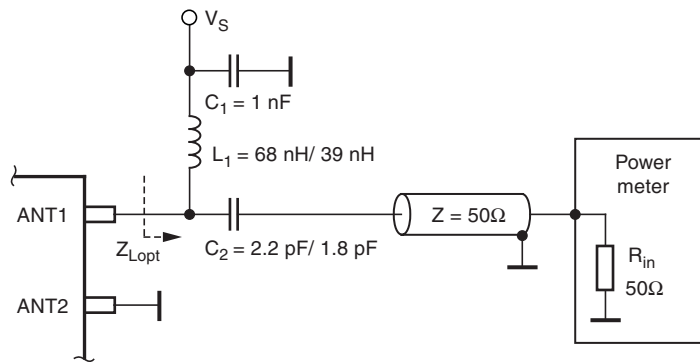
The latter is measured from the application into the IC instead of from the IC into the application for a power amplifier.

The 0.66 pF output capacitance absorbed into the load impedance a real impedance of 684 Ω (ATA6285) at 315 MHz and 623 Ω (ATA6286) at 433.92 MHz should be measured with a network analyses at pin 5 (ANT1) with the ATA6285/ATA6286 soldered, an optimized antenna connected and the power amplifier switched off.

Less output power is achieved by lowering the real parallel part where the parallel imaginary part should be kept constant. Lowering the real part of the load impedance also reduces the supply voltage dependency of the output power.

Output power measurement can be done with the circuit as shown in Output Power Measurement. Please note that the component values must be changed to compensate the individual board parasitics until the ATA6285/ATA6286 has the right load impedance. Also, the damping of the cable used to measure the output power must be calibrated.

Figure 4-7. Output Power Measurement ATA6285/ATA6286



5. Ordering Information

| Extended Type Number | Package | Frequency | MOQ | Remarks |
|----------------------|---------|-----------|-----------------------|------------------|
| ATA6285-PNPW | QFN32 | 315 MHz | Packaging unit: 1,500 | Taped and reeled |
| ATA6286-PNPW | QFN32 | 433 MHz | Packaging unit: 1,500 | Taped and reeled |
| ATA6285-PNQW | QFN32 | 315 MHz | 6,000 | Taped and reeled |
| ATA6286-PNQW | QFN32 | 433 MHz | 6,000 | Taped and reeled |

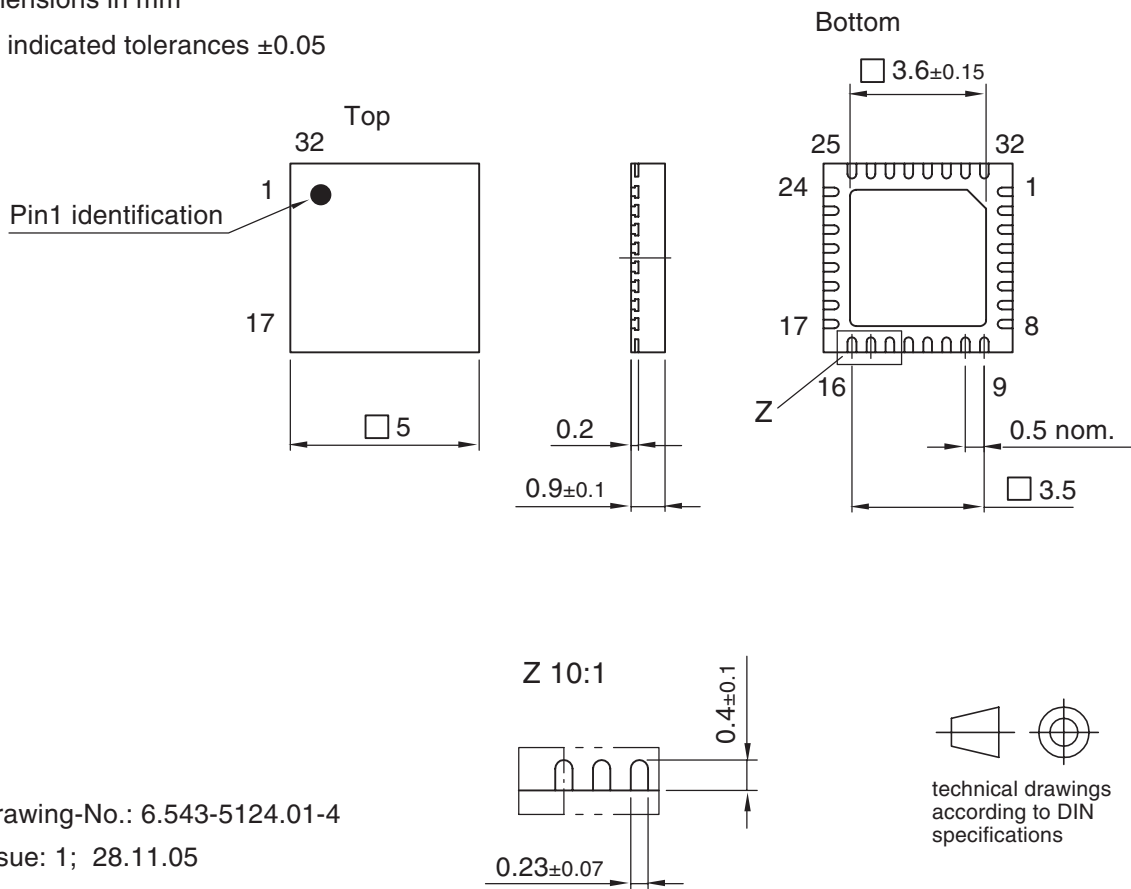
6. Package Information

Package: QFN_ 5 x 5_32L

Exposed pad 3.6 x 3.6

Dimensions in mm

Not indicated tolerances ± 0.05



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