



512MB – 64Mx72 DDR2 SDRAM REGISTERED DIMM, w/PLL

FEATURES

- Registered 240-pin, dual in-line memory module
- Fast data transfer rates: PC2-6400*, PC2-5300*, PC2-4200 and PC2-3200
- Utilizes 800*, 667*, 533 and 400 MT/s DDR2 SDRAM components
- $V_{CC} = V_{CCQ} = 1.8V \pm 0.1V$
- $V_{CCSPD} = 1.7V$ to 3.6V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Write Latency = Read Latency $1^{t_{CK}}$
- Programmable CAS# latency (CL): 3, 4, 5* and 6*
- Adjustable data-output drive strength
- On-die termination (ODT)
- 7.8µs average periodic refresh interval
- Posted CAS# latency: 0, 1, 2, 3 and 4
- Serial Presence Detect (SPD) with EEPROM
- Auto & Self Refresh (8k/64ms refresh)
- Gold edge contacts
- RoHS compliant
- Package option
 - 240 Pin DIMM
 - PCB – 30.00mm (1.181") TYP

DESCRIPTION

The WV3HG64M72EER is a 64Mx72 Double Data Rate DDR2 SDRAM high density module. This memory module consists of nine 64Mx8 bit with 4 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a 240-pin DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

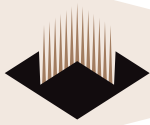
NOTE: Consult factory for availability of:

- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-3200	PC2-4200	PC2-5300*	PC2-6400*
Clock Speed	200MHz	266MHz	333MHz	400MHz
CL-t _{RP} -t _{RP}	3-3-3	4-4-4	5-5-5	6-6-6

* Consult factory for availability



PIN CONFIGURATION

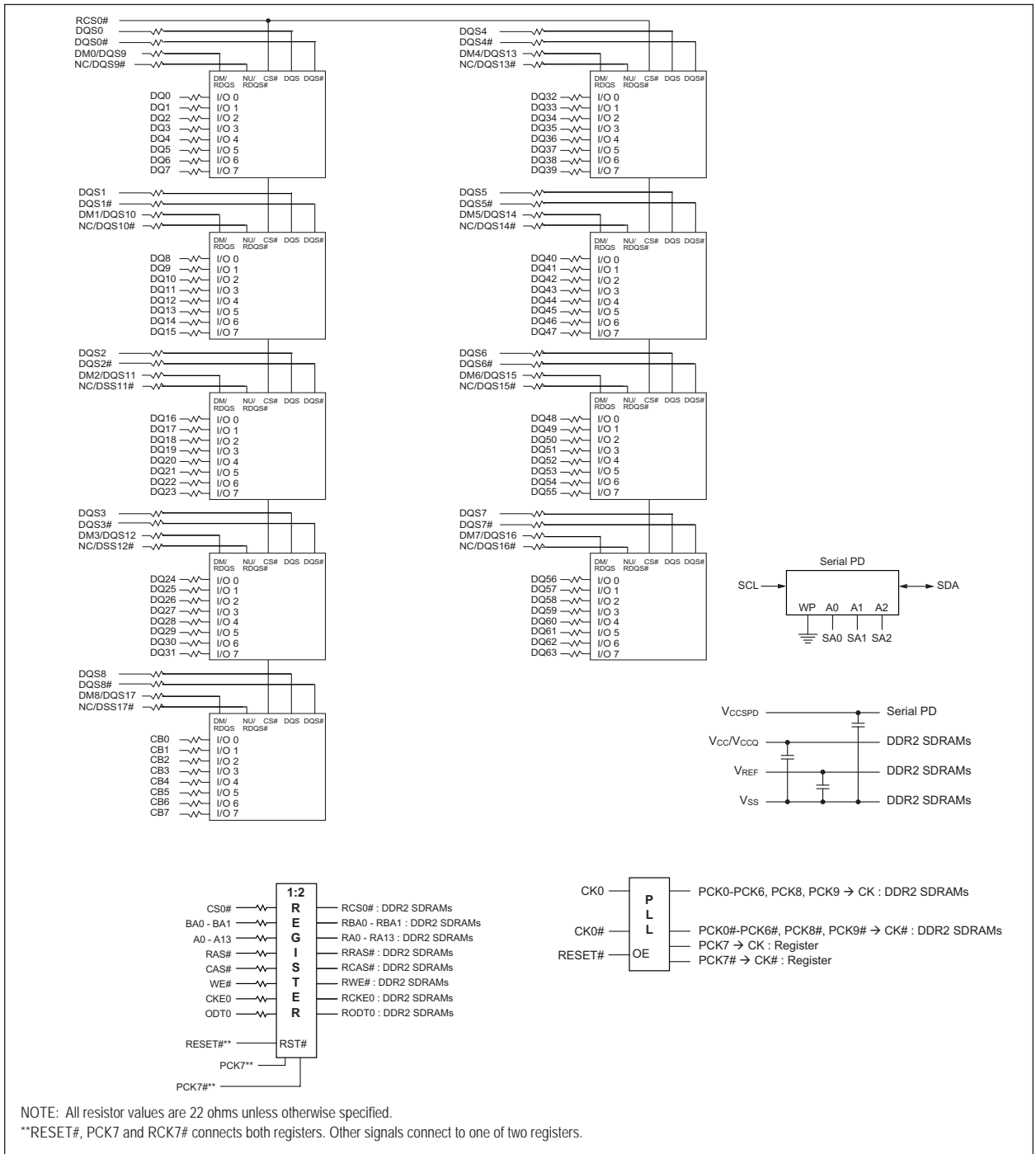
Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	V _{REF}	61	A4	121	V _{SS}	181	V _{CC}
2	V _{SS}	62	V _{CC}	122	DO4	182	A3
3	DQ0	63	A2	123	DO5	183	A1
4	DQ1	64	V _{CC}	124	V _{SS}	184	V _{CC}
5	V _{SS}	65	V _{SS}	125	DM0/DQS9	185	CK0
6	DQS0#	66	V _{SS}	126	NC/DQS9#	186	CK0#
7	DQS0	67	V _{CC}	127	V _{SS}	187	V _{CC}
8	V _{SS}	68	NC	128	DO6	188	A0
9	DQ2	69	V _{CC}	129	DO7	189	V _{CC}
10	DQ3	70	A10/AP	130	V _{SS}	190	BA1
11	V _{SS}	71	BA0	131	DQ12	191	V _{CC}
12	DO8	72	V _{CC}	132	DQ13	192	RAS#
13	DO9	73	WE#	133	V _{SS}	193	CS0#
14	V _{SS}	74	CAS#	134	DM1/DQS10	194	V _{CC}
15	DQS1#	75	V _{CC}	135	NC/DQS10#	195	ODT0
16	DQS1	76	NC	136	V _{SS}	196	A13
17	V _{SS}	77	NC	137	NC	197	V _{CC}
18	RESET#	78	V _{CC}	138	NC	198	V _{SS}
19	NC	79	V _{SS}	139	V _{SS}	199	DQ36
20	V _{SS}	80	DO32	140	DO14	200	DO37
21	DQ10	81	DO33	141	DO15	201	V _{SS}
22	DQ11	82	V _{SS}	142	V _{SS}	202	DM4/DQS13
23	V _{SS}	83	DQS4#	143	DO20	203	NC/DQS13#
24	DO16	84	DQS4	144	DO21	204	V _{SS}
25	DO17	85	V _{SS}	145	V _{SS}	205	DO38
26	V _{SS}	86	DQ34	146	DM2/DQS11	206	DQ39
27	DQS2#	87	DO35	147	NC/DQS11#	207	V _{SS}
28	DQS2	88	V _{SS}	148	V _{SS}	208	DO44
29	V _{SS}	89	DO40	149	DO22	209	DO45
30	DQ18	90	DO41	150	DO23	210	V _{SS}
31	DO19	91	V _{SS}	151	V _{SS}	211	DM5/DQS14
32	V _{SS}	92	DQS5#	152	DO28	212	NC/DQS14#
33	DO24	93	DQS5	153	DO29	213	V _{SS}
34	DO25	94	V _{SS}	154	V _{SS}	214	DO46
35	V _{SS}	95	DO42	155	DM3/DQS12	215	DO47
36	DQS3#	96	DO43	156	NC/DQS12#	216	V _{SS}
37	DQS3	97	V _{SS}	157	V _{SS}	217	DO52
38	V _{SS}	98	DO48	158	DO30	218	DO53
39	DO26	99	DO49	159	DO31	219	V _{SS}
40	DO27	100	V _{SS}	160	V _{SS}	220	NC
41	V _{SS}	101	SA2	161	CB4	221	NC
42	CB0	102	NC	162	CB5	222	V _{SS}
43	CB1	103	V _{SS}	163	V _{SS}	223	DM6/DQS15
44	V _{SS}	104	DQS6#	164	DM8/DQS17	224	NC/DQS15#
45	DQS8#	105	DQS6	165	NC/DQS17#	225	V _{SS}
46	DQS8	106	V _{SS}	166	V _{SS}	226	DO54
47	V _{SS}	107	DO50	167	CB6	227	DO55
48	CB2	108	DO51	168	CB7	228	V _{SS}
49	CB3	109	V _{SS}	169	V _{SS}	229	DO60
50	V _{SS}	110	DO56	170	V _{CC}	230	DO61
51	V _{CC}	111	DO57	171	NC	231	V _{SS}
52	CKE0	112	V _{SS}	172	V _{CC}	232	DM7/DQS16
53	V _{CC}	113	DQS7#	173	NC	233	NC/DQS16#
54	NC	114	DQS7	174	NC	234	V _{SS}
55	NC	115	V _{SS}	175	V _{CC}	235	DO62
56	V _{CC}	116	DO58	176	A12	236	DO63
57	A11	117	DO59	177	A9	237	V _{SS}
58	A7	118	V _{SS}	178	V _{CC}	238	V _{CC} SPD
59	V _{CC}	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

PIN NAMES

Pin Name	Function
A0-A13	Address Inputs
BA0,BA1	SDRAM Bank Addresses
DQ0-DQ63	Data Input/Output
CB0-CB7	Check Bits
DQS0-DQS17	Data strobes
DQS0#-DQS17#	Data strobes complement
DM0 - DM8	Data Masks
ODT0	On-die termination control
CK0,CK0#	Clock Inputs
CKE0	Clock Enable
CS0#	Chip Select
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
RESET#	Register Reset Input/PLL OE
V _{CC}	Core and I/O Power (1.8V)
V _{SS}	Ground
SA0-SA2	SPD address
SDA	SPD Data Input/Output
SCL	Serial Presence Detect (SPD) Clock Input
V _{REF}	Input/Output Reference Voltage
V _{CC} SPD	SPD Power
NC	Spare pins, No connect



FUNCTIONAL BLOCK DIAGRAM





DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply Voltage	V _{CC}	1.7	1.8	1.9	V	3
I/O Reference Voltage	V _{REF}	0.49 x V _{CC}	0.50 x V _{CC}	0.51 x V _{CC}	V	1
I/O Termination Voltage	V _{TT}	V _{REF} -0.04	V _{REF}	V _{REF} +0.04	V	2
SPD Supply Voltage	V _{CCSPD}	1.7	-	3.6	V	

Notes:

- V_{REF} is expected to equal V_{CC/2} of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed +/-2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
- V_{CCO} of all IC's are tied to V_{CC}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	
V _{CC}	Voltage on V _{CC} pin relative to V _{SS}	-0.5	2.3	V	
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}	-0.5	2.3	V	
T _{STG}	Storage Temperature	-55	100	°C	
I _L	Input leakage current: Any input 0V < V _{IN} < V _{CC} ; V _{REF} input 0V < V _{IN} < 0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#, CS#, CKE	-5	5	μA
		CK, CK#	-10	10	
		DM	-5	5	
I _{OZ}	Output leakage current; 0V < V _{OUT} < V _{CC} ; DQs and ODT are disable	-5	5	μA	
I _{VREF}	V _{REF} leakage current; V _{REF} = Valid V _{REF} level	-18	18	μA	

CAPACITANCE

T_A = 25°C, f = 100MHz

Parameter	Symbol	Min	Max	Units
Input Capacitance: (A0-A13, BA0-BA1, RAS#, CAS#, WE#)	CIN ₁	11	12	pF
Input Capacitance: (CKE0), (ODT0)	CIN ₂	11	12	pF
Input Capacitance: (CS0#)	CIN ₃	11	12	pF
Input Capacitance: (CK0, CK0#)	CIN ₄	10	11	pF
Input Capacitance: (DM0-DM8), (DQS0-DQS17)	CIN ₅	6.5	8	pF
Input/Output Capacitance: (DQ0 - DQ63), (CB0 -CB7)	COU _{T1}	6.5	8	pF



OPERATING TEMPERATURE CONDITION

Parameter	Symbol	Rating	Units	Notes
Operating Case Temperature (Commercial)	TOPER	0 to +85°C	°C	1, 2

- NOTE:
1. Operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51.2
 2. At 0 to +85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVEL

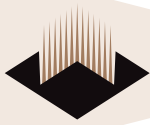
All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
Input High (Logic 1) Voltage	V _{IH} (DC)	V _{REF} + 0.125	V _{CC} + 0.300	V
Input Low (Logic 0) Voltage	V _{IL} (DC)	- 0.300	V _{REF} - 0.125	V

INPUT AC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
AC Input High (Logic 1) Voltage DDR2-400 & DDR2-533	V _{IH} (AC)	V _{REF} + 0.250	-	V
AC Input High (Logic 1) Voltage DDR2-667	V _{IH} (AC)	V _{REF} + 0.200	-	V
AC Input High (Logic 0) Voltage DDR2-400 & DDR2-533	V _{IL} (AC)	-	V _{REF} - 0.250	V
AC Input High (Logic 0) Voltage DDR2-667	V _{IL} (AC)	-	V _{REF} - 0.200	V



DDR2 I_{cc} SPECIFICATIONS AND CONDITIONS

Includes DDR2 SDRAM components only

Symbol	Proposed Conditions	806	665	534	403	Units	
I _{cc0*}	Operating one bank active-precharge current; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RASmin} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	TBD	1,120	1,120	mA	
I _{cc1*}	Operating one bank active-read-precharge current; I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RASmin} (I _{CC}), t _{RCD} = t _{RCD} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{cc4W}	TBD	TBD	1,255	1,255	mA	
I _{cc2P*}	Precharge power-down current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	TBD	472	472	mA	
I _{cc2O**}	Precharge quiet standby current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	TBD	670	670	mA	
I _{cc2N**}	Precharge standby current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	TBD	715	715	mA	
I _{cc3P**}	Active power-down current; All banks open; t _{CK} = t _{CK} (I _{CC}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	TBD	TBD	670	670	mA
		Slow PDN Exit MRS(12) = 1	TBD	TBD	508	508	mA
I _{cc3N**}	Active standby current; All banks open; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RASmax} (I _{CC}), t _{RP} = t _{RP} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	TBD	850	850	mA	
I _{cc4W*}	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RASmax} (I _{CC}), t _{RP} = t _{RP} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	TBD	1,480	1,390	mA	
I _{cc4R*}	Operating burst read current; All banks open, Continuous burst reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RASmax} (I _{CC}), t _{RP} = t _{RP} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{cc4W}	TBD	TBD	1,525	1,390	mA	
I _{cc5B**}	Burst auto refresh current; t _{CK} = t _{CK} (I _{CC}); Refresh command at every t _{REFC} (I _{CC}) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	TBD	1,160	1,660	mA	
I _{cc6**}	Self refresh current; CK and CK\ at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	TBD	TBD	72	72	mA
I _{cc7*}	Operating bank interleave read current; All bank interleaving reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = t _{RCD} (I _{CC}) - 1 * t _{CK} (I _{CC}); t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RRD} = t _{RRD} (I _{CC}), t _{RCD} = 1 * t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTS; Data bus inputs are SWITCHING.	TBD	TBD	2,380	2,380	mA	

Note: I_{cc} specification is based on SAMSUNG components. Other DRAM Manufacturers specification may be different.

*: Value calculated as one module rank in this operating condition, and all other module ranks in I_{cc2P} (CKE LOW) mode.

** : Value calculated reflects all module ranks in this operating condition.



AC TIMING PARAMETERS & SPECIFICATIONS

AC CHARACTERISTICS			806		665		534		403		UNIT	
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock	Clock cycle time	CL = 6	t _{CK (6)}	TBD	TBD						ps	
		CL = 5	t _{CK (5)}	TBD	TBD	3,000	8,000				ps	
		CL = 4	t _{CK (4)}	TBD	TBD	3,750	8,000	3,750	8,000	5,000	8,000	ps
		CL = 3	t _{CK (3)}	TBD	TBD	5,000	8,000	5,000	8,000	5,000	8,000	ps
	CK high-level width	t _{CH}	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	
	CK low-level width	t _{CL}	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	
	Half clock period	t _{HP}	TBD	TBD	MIN(t _{CH} , t _{CL})		MIN(t _{CH} , t _{CL})		MIN(t _{CH} , t _{CL})		ps	
Clock jitter	t _{JIT}	TBD	TBD	-125	125	-125	125	-125	125	ps		
Data	DQ output access time from CK/CK#	t _{AC}	TBD	TBD	-450	+450	-500	+500	-600	+600	ps	
	Data-out high-impedance window from CK/CK#	t _{HZ}	TBD	TBD		t _{AC(MAX)}		t _{AC(MAX)}		t _{AC(MAX)}	ps	
	Data-out low-impedance window from CK/CK#	t _{LZ}	TBD	TBD	t _{AC(MIN)}	t _{AC(MAX)}	t _{AC(MIN)}	t _{AC(MAX)}	t _{AC(MIN)}	t _{AC(MAX)}	ps	
	DQ and DM input setup time relative to DQS	t _{DS}	TBD	TBD	100		100		150			
	DQ and DM input hold time relative to DQS	t _{DH}	TBD	TBD	225		225		275			
	DQ and DM input pulse width (for each input)	t _{DLPW}	TBD	TBD	0.35		0.35		0.35		t _{CK}	
	Data hold skew factor	t _{QHS}	TBD	TBD		340		400		450	ps	
	DQ...DQS hold, DQS to first DQ to go nonvalid, per access	t _{QH}	TBD	TBD	t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		ps	
	Data valid output window (DVW)	t _{DVW}	TBD	TBD	t _{QH} - t _{DQSQ}		t _{QH} - t _{DQSQ}		t _{QH} - t _{DQSQ}		ns	
Data Strobe	DQS input high pulse width	t _{DQSH}	TBD	TBD	0.35		0.35		0.35		t _{CK}	
	DQS input low pulse width	t _{DQSL}	TBD	TBD	0.35		0.35		0.35		t _{CK}	
	DQS output access time from CK/CK#	t _{DQSCK}	TBD	TBD	-400	+400	-450	+450	-500	+500	ps	
	DQS falling edge to CK rising ... setup time	t _{DSS}	TBD	TBD	0.2		0.2		0.2		t _{CK}	
	DQS falling edge from CK rising ... hold time	t _{DSH}	TBD	TBD	0.2		0.2		0.2		t _{CK}	
	DQS...DQ skew, DQS to last DQ valid, per group, per access	t _{DQSQ}	TBD	TBD		240		300		350	ps	
	DQS read preamble	t _{RPRE}	TBD	TBD	0.9	1.1	0.9	1.1	0.9	1.1	t _{CK}	
	DQS read postamble	t _{RPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}	
	DQS write preamble setup time	t _{WPRES}	TBD	TBD	0		0		0		ps	
	DQS write preamble	t _{WPRE}	TBD	TBD	0.35		0.35		0.35		t _{CK}	
	DQS write postamble	t _{WPST}	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}	
Write command to first DQS latching transition	t _{DQSS}	TBD	TBD	WL- 0.25	WL+ 0.25	WL- 0.25	WL+ 0.25	WL- 0.25	WL+ 0.25	t _{CK}		
Address and control	Address and control input pulse width for each input	t _{IPW}	TBD	TBD	0.6		0.6		0.6		t _{CK}	
	Address and control input setup time	t _{IS}	TBD	TBD	200		250		250		ps	
	Address and control input hold time	t _{IH}	TBD	TBD	275		375		475		ps	
	Address and control input hold time	t _{ICD}	TBD	TBD	2		2		2		t _{CK}	

* AC specification is based on SAMSUNG components. Other DRAM manufactures specification may be different.

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AC TIMING PARAMETERS (cont'd)

AC CHARACTERISTICS			806		665		534		403		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Command and Address	ACTIVE to ACTIVE (same bank) command	t _{RC}	TBD	TBD	55		55		55		ns
	ACTIVE bank a to ACTIVE bank b command	t _{RRD}	TBD	TBD	7.5		7.5		7.5		ns
	ACTIVE to READ or WRITE delay	t _{RCD}	TBD	TBD	15		15		15		ns
	Four Bank Activate period	t _{FAW}	TBD	TBD	37.5	37.5	37.5	37.5	37.5	37.5	ns
	ACTIVE to PRECHARGE command	t _{RAS}	TBD	TBD	40	70,000	40	70,000	40	70,000	ns
	Internal READ to precharge command delay	t _{RTP}	TBD	TBD	7.5		7.5		7.5		ns
	Write recovery time	t _{WR}	TBD	TBD	15		15		15		ns
	Auto precharge write recovery + precharge time	t _{DAL}	TBD	TBD	t _{WR} +t _{RP}		t _{WR} +t _{RP}		t _{WR} +t _{RP}		ns
	Internal WRITE to READ command delay	t _{WTR}	TBD	TBD	7.5		7.5		7.5		ns
	PRECHARGE command period	t _{RP}	TBD	TBD	15		15		15		ns
	PRECHARGE ALL command period	t _{RPA}	TBD	TBD	t _{RP} +t _{CK}		t _{RP} +t _{CK}		t _{RP} +t _{CK}		ns
	LOAD MODE command cycle time	t _{MRD}	TBD	TBD	2		2		2		tck
CKE low to CK,CK# uncertainty	t _{DELAY}	TBD	TBD	t _{IS} +t _{CK} t _{IH}		t _{IS} +t _{CK} t _{IH}		t _{IS} +t _{CK} t _{IH}		ns	
Self Refresh	REFRESH to Active of Refresh to Refresh command interfal	t _{RFC}	TBD	TBD	127.5	70,000	127.5	70,000	127.5	70,000	ns
	Average periodic refresh interval	t _{REFI}	TBD	TBD		7.8		7.8		7.8	μs
	Exit self refresh to non-READ command	t _{XSNR}	TBD	TBD	t _{RFC(MIN)} +10		t _{RFC(MIN)} +10		t _{RFC(MIN)} +10		ns
	Exit self refresh to READ command	t _{XSRD}	TBD	TBD	200		200		200		tck
	Exit self refresh timing reference	t _{ISXR}	TBD	TBD	t _{IS}		t _{IS}		t _{IS}		ps
ODT	ODT turn-on delay	t _{AOND}	TBD	TBD	2	2	2	2	2	2	tck
	ODT turn-on	t _{AON}	TBD	TBD	t _{AC(MIN)}	t _{AC(MAX)} +1000	t _{AC(MIN)}	t _{AC(MAX)} +1000	t _{AC(MIN)}	t _{AC(MAX)} +1000	ps
	ODT turn-off delay	t _{AOFD}	TBD	TBD	2.5	2.5	2.5	2.5	2.5	2.5	tck
	ODT turn-off	t _{AOF}	TBD	TBD	t _{AC(MIN)}	t _{AC(MAX)} +600	t _{AC(MIN)}	t _{AC(MAX)} +600	t _{AC(MIN)}	t _{AC(MAX)} +600	ps
	ODT turn-on (power-down mode)	t _{AONPD}	TBD	TBD	t _{AC(MIN)} +2000	2 x t _{CK} + t _{AC(MAX)} +1000	t _{AC(MIN)} +2000	2 x t _{CK} + t _{AC(MAX)} +1000	t _{AC(MIN)} +2000	2 x t _{CK} + t _{AC(MAX)} +1000	ps
	ODT turn-off (power-down mode)	t _{AOFPD}	TBD	TBD	t _{AC(MIN)} +2000	2.5 x t _{CK} + t _{AC(MAX)} +1000	t _{AC(MIN)} +2000	2.5 x t _{CK} + t _{AC(MAX)} +1000	t _{AC(MIN)} +2000	2.5 x t _{CK} + t _{AC(MAX)} +1000	ps
	ODT to power-down entry latency	t _{ANPD}	TBD	TBD	3		3		3		tck
	ODT power-down exit latency	t _{AXPD}	TBD	TBD	8		8		8		tck
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t _{XARD}	TBD	TBD	2		2		2		tck
	Exit active power-down to READ command, MR[bit12=1]	t _{XARDS}	TBD	TBD	7-AL		6-AL		6-AL		tck
	A Exit precharge power-down to any non-READ command.	t _{XP}	TBD	TBD	2		2		2		tck
	CKE minimum high/low time	t _{CKE}	TBD	TBD	3		3		3		tck

* AC specification is based on SAMSUNG components. Other DRAM manufactures specification may be different.



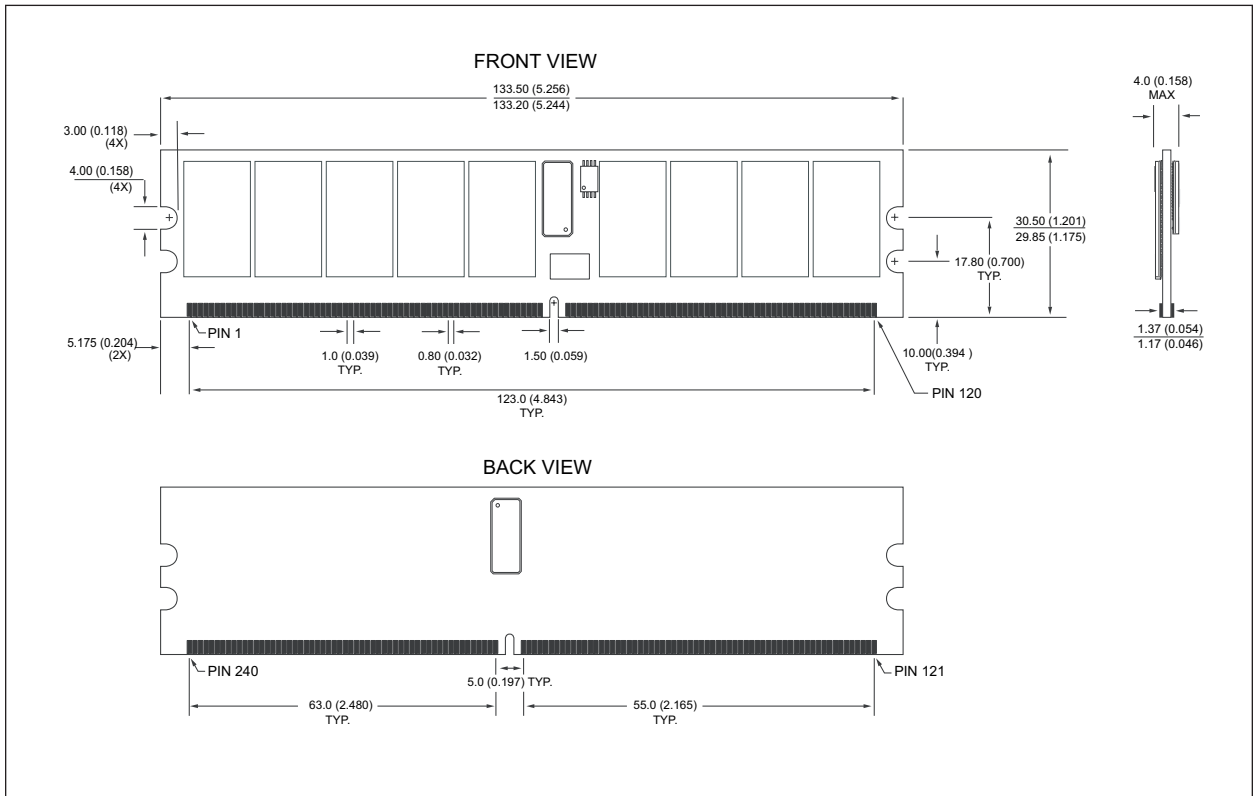
ORDERING INFORMATION FOR D6

Part Number	Speed	CAS Latency	t _{RCD}	t _{RP}	Height*
WV3HG64M72EER806D6	400MHz/800Mb/s	6	6	6	30.00mm (1.181") TYP
WV3HG64M72EER665D6	333MHz/667Mb/s	5	5	5	30.00mm (1.181") TYP
WV3HG64M72EER534D6	266MHz/533Mb/s	4	4	4	30.00mm (1.181") TYP
WV3HG64M72EER403D6	200MHz/400Mb/s	3	3	3	30.00mm (1.181") TYP

NOTES:

- RoHS products. ("G" = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

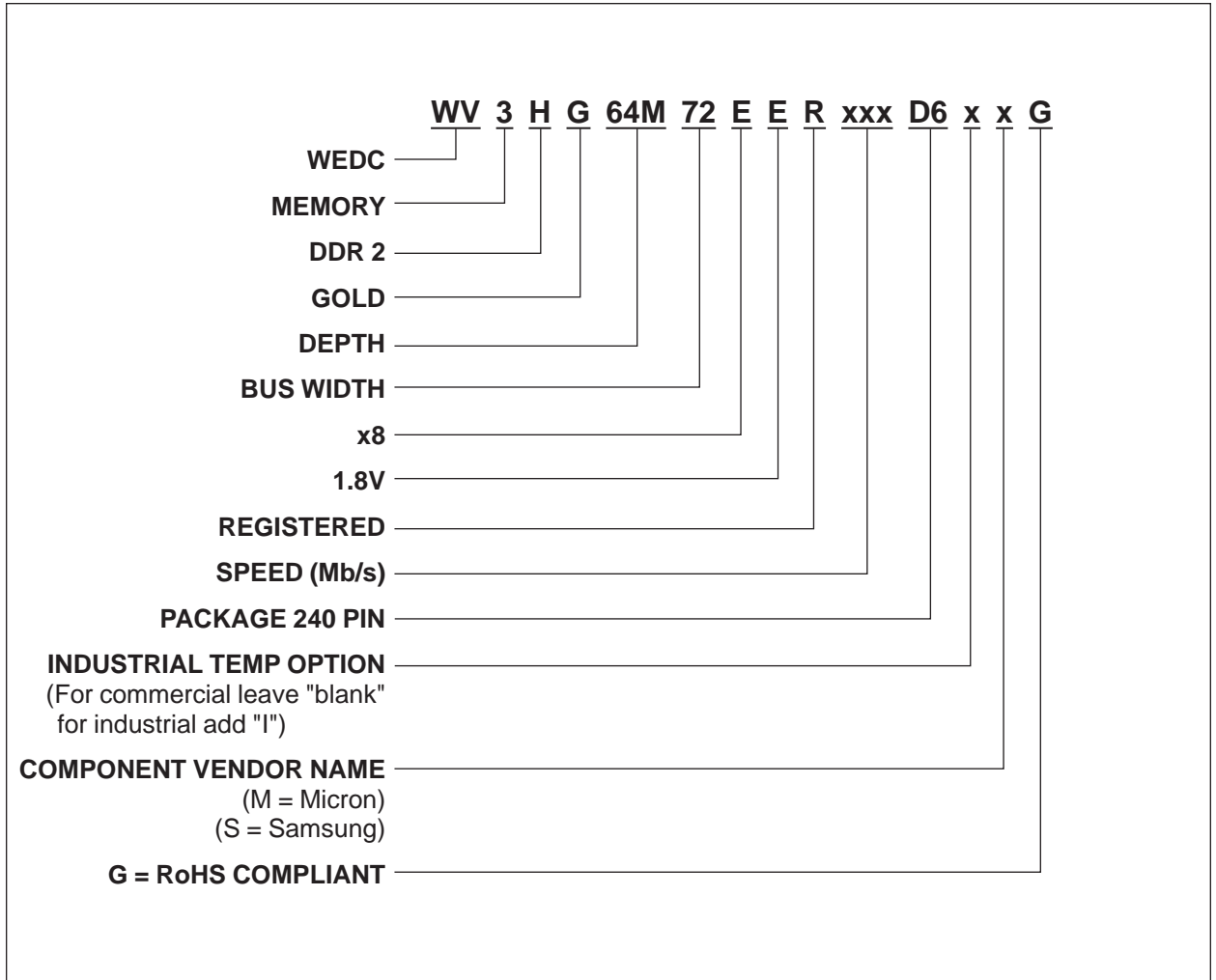
PACKAGE DIMENSIONS FOR D6



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



PART NUMBERING GUIDE





Document Title

512MB – 64Mx72 DDR2 SDRAM REGISTERED, w/PLL

DRAM DIE OPTIONS:

- SAMSUNG: C-Die, will move to E-Die Q2'06
- MICRON: U37: B-Die

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	August 2006	Concept
Rev 1	1.0 Moved to Advanced	August 14 2006	Advanced