

STEERING DIODE TVS ARRAY

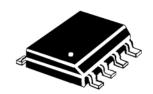
SRDA70-4



DESCRIPTION

These low capacitance diode arrays are multiple, discrete, isolated junctions fabricated by a planar process and mounted in a SO-8 package for use as steering diodes protecting up to four I/O ports from ESD, EFT, or surge by directing them either to the positive side of the power supply line or to ground (see schematic, page 2). An external TVS diode may be added between the positive supply line and ground to prevent overvoltage on the supply rail. These arrays offer many advantages of integrated circuits such as high-density packaging and improved reliability. This is a result of fewer pick and place operations, smaller footprint, smaller weight, and elimination of various discrete packages that may not be as user friendly in PC board mounting.

TVS array[™] SERIES



IMPORTANT: For the most current data, consult *MICROSEMI's* website: http://www.microsemi.com

FEATURES

- Diode Array to Protect Four I/O Lines
- Surge protection per IEC 61000-4-2, IEC 61000-4-4 and IEC61000-4-5 (1 kV, 24 A at 8/20 µs)
- UL 94V-0 Flammability Classification
- Low Capacitance for High-Speed Interfaces

APPLICATIONS / BENEFITS

- Data Line Protection
- Latch-Up Protection
- RS-232 & RS-422 Interface Networks
- Computer I/O Ports
- LAN

MAXIMUM RATINGS

- Operating Temperature: -55°C to +150°C
 Storage Temperature: -55°C to +150°C
- Peak Pulse Power: 500 Watts (8/20 μs, Figure 1)
- Peak Pulse Current: 24 Amps (8/20 µs, Figure 1)
- Pulse Repetition Rate: < .01%
- Lead Soldering Temperature: 260°C for 10 seconds

MECHANICAL AND PACKAGING

- Molded SO-8 Surface Mount
- Weight 0.066 grams (approximate)
- Marking: Logo, device marking code, date code
- Pin #1 defined by dot on top of package
- Tape & Reel per EIA Standard 481
- 13 inch reel; 2,500 pieces (OPTIONAL)
- Carrier tubes; 95 pcs (STANDARD)

	ELECTRICAL CHARACTERISTICS										
PART NUMBER	DEVICE MARKING	PEAK REVERSE VOLTAGE V _{RWM}	BREAKDOWN VOLTAGE V _{BR} @50 μA VOLTS	FORWARD CLAMPING VOLTAGE V _{FC} @ 1 Amp (Figure 2) VOLTS	FORWARD CLAMPING VOLTAGE V _{FC} @ 10 Amp (Figure 2) VOLTS	REVERSE LEAKAGE CURRENT I _R @ V _{RWM} µA	CAPACITANCE (f=1 MHz) C @ 0V Between I/O pins and ground pF	CAPACITANCE (f=1 MHz) C Q 0V Between I/O pins pF			
		MAX	MIN	MAX	MAX	MAX	MAX	TYP			
SRDA70-4	SM70-4	70	85	1.3	3.3	5	15	4			



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SYMBOLS & DEFINITIONS							
Symbol	Definition						
V_{BR}	Minimum Breakdown Voltage: The minimum voltage the device will exhibit at a specified current.						
V_{RWM}	Working Peak Reverse Voltage: The maximum peak voltage that can be applied over the operating temperature range.						
V _{FC}	Forward Clamping Voltage: The maximum forward clamping voltage across the device when subjected to a given current at a pulse time of 20 µs.						
I _R	Maximum Leakage Current: The maximum leakage current at V _{RWM} .						
С	Capacitance: The capacitance of the TVS as defined @ 0 volts at a frequency of 1 MHz and stated in picofarads.						

GRAPHS

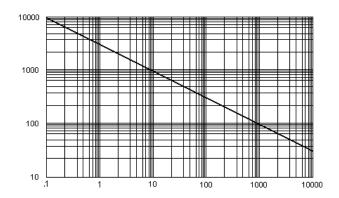


Figure 1
Peak Pulse Power Vs Pulse Time t = μsec

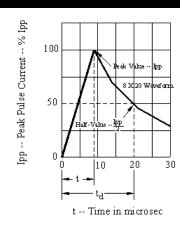
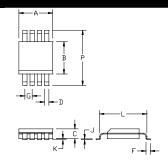


Figure 2 Pulse Wave Form

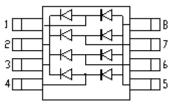
0.045" +/- .005"

OUTLINE AND SCHEMATIC



	INC	HES	MILLIMETERS					
DIM	MIN	MAX	MIN	MAX				
Α	0.188	0.197	4.77	5.00				
В	0.150	0.158	3.81	4.01				
С	0.053	0.069	1.35	1.75				
D	0.011	0.021	0.28	0.53				
F	0.016	0.050	0.41	1.27				
G	0.050	BSC	1.27 BSC					
J	0.006	0.010	0.15	0.25				
K	0.004	0.008	0.10	0.20				
L	0.189	0.206	4.80	5.23				
Р	0.228	0.244	5.79	6.19				
OUTLINE								

0.245" MIN MIN 0.160" +/- .005" 0.30" +/- .005 PAD LAYOUT



SCHEMATIC