256 X 8 BIT STATIC CMOS EEPROM WITH I^2C-BUS. (ANALOG - MICROCIRCUIT PCF8582E, F.PHILIPS).

INF8582E - 2Kbit (256x8 bit) electronically erasable programmable ROM with “floating” gate. Internal reduntant code correcting errors as single bit errors is used to enhance the reliability. Microcircuit operates in systems with serial I^2C-bus consisting of two lines: for data signals (SDA) (bidirectional) and for clock signals (SCL). Up to 8 microcircuits may be connected to I^2C-bus. Stacker programming is done by tunneling electrons. Programming voltage is generated by voltage multiplier built-in chip. The implementation of CMOS technology in full provides low power consumption.

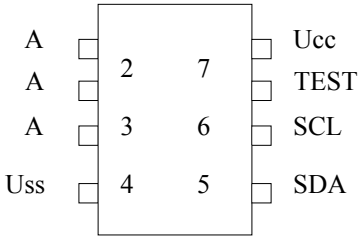
These products are purposed for implementation in portable consumer applications, in autoelectronics, in **peripheric computer devices.** Thea are used in TV channel selectors, for storage of frequency, volume and image data, in tuning control blocks in radioset, , in measuring devices for standard curves storage, calibration data, minimum and maximum values, in , seat position adgusting systems, side glass, in speedometers.

Characteristic properties:

- without decay storage 2 Kbit 10 years;
- single-error correction circuit;
- one power supply (Ucc=4,5V - 5,5V);
- built-in voltage multiplier in chip;
- input/output consecutive bus ;
- automatic increment of word address;
- internal timer for recording;
- 100 000 cycles erasure/**recording on** byte with low failure rate;
- unlimited number of reading cycles;
- low power consumption;
- temperature range -40 - +85 ^{O}C.

The basing circuit diagram and Pins purpose table are given below in fig.1, main electrical characteristics are indicated in Table 1.

Microcircuit basing diagram



Package: 2101.8-A

Рис.1

Pins purpose table

Pin №	Sym-bol	Purpose
1	A0	address input
2	A1	address input
3	A2	address input
4	Uss	"ground"
5	SDA	data line, input/output
6	SCL	clock signal line (input)
7	TEST	synchronizing signal of programming
8	Ucc	power supply

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BLOCK DIAGRAM

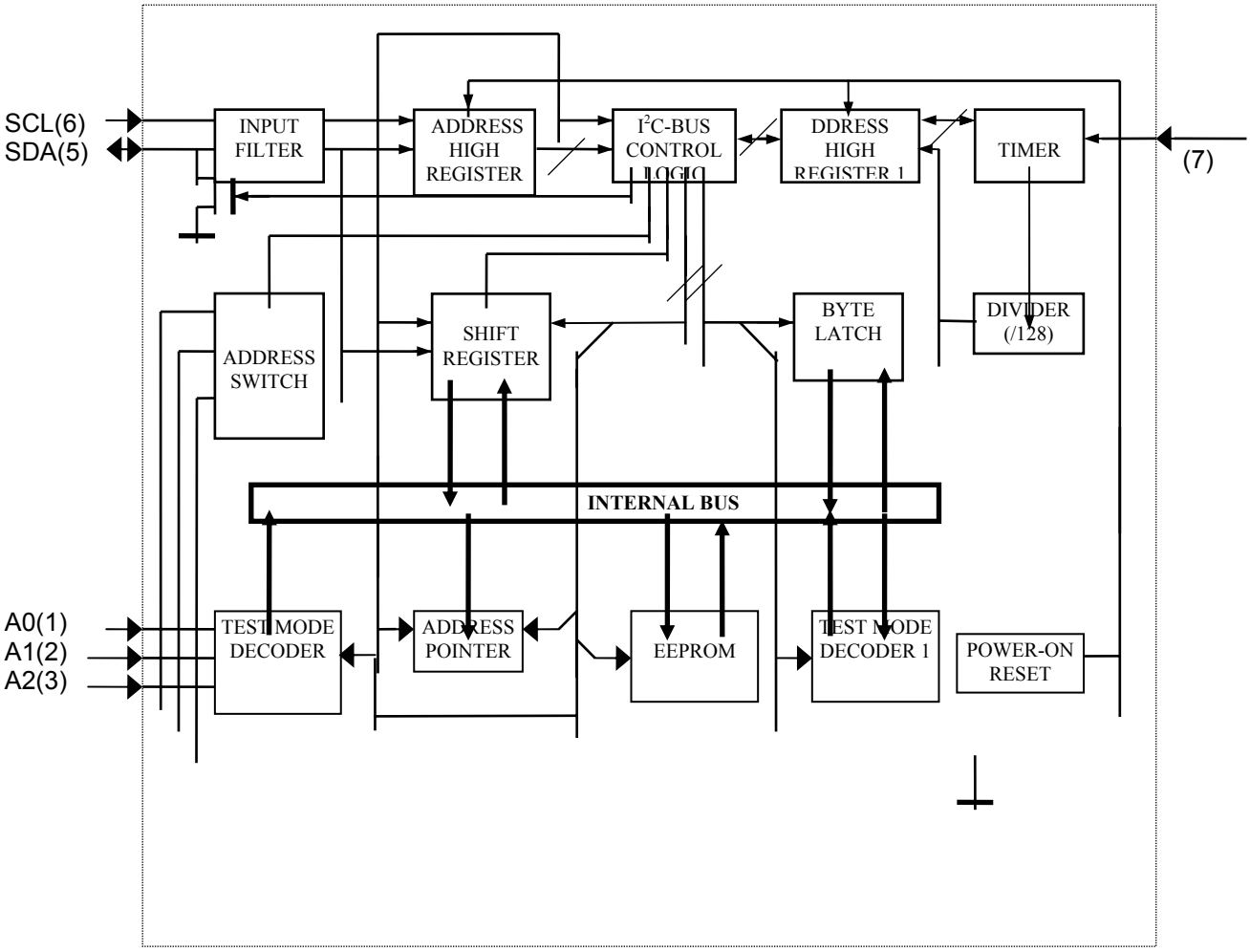

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Table 1 - Main characteristics of microcircuits

Parameters	Mode	Symbol	Min	Max
Dynamic consumption current (reading), mA	f_{SCL}=100кHz U_{CC}=5.5V	$I_{CC0(RD)}$	-	1,6
Dynamic consumption current(erasure/recording), mA	f_{SCL}=100кHz U_{CC}=5.5V	$I_{CC0(E/WR)}$	-	2,5
Supply voltage, V		V_{DD}	4.5	5.5
Static consumption current, μA	U_{CC}=5,5V	I_{CCS}	-	10,0
Clock frequency, кHz		f_{SCL}	0	100
Max output current, mA		I_{OL}		3.0
Duration of " erasure/recording " cycle, ms: - input external control TEST - inside chip control		$t_{E/WR}$	 5 10 ÷ 13 (standard)	 25
Input TEST				
High level input voltage, V		U_{IH}	0,9U_{CC}	U_{CC}+0,8
Low level input voltage, V		U_{IL}	-0,8	0,1U_{CC}
InputsSCL and SDA				
High level input voltage, V		U_{IH}	0,7U_{CC}	U_{CC}+0,8
Low level input voltage, V		U_{IL}	-0,8	0,3U_{CC}
Output SDA				
Low level output voltage, V	I_{OL}=3,0 mA U_{CC}=4,5 V	U_{OL}	-	0,4

In order to make the understanding of the microcircuit INF8582E way of operation easier it is necessary to **examine** I²C-bus interface characteristics.

I²C-bus is a bidirectional double-wire serial bus purposed for data exchange between different (various) integrated circuits. It consists of date line (SDA) and clock signals line (SCL). **In common case** the both lines should be connected to the positive power supply by charging resistor (output stage with open drain/collector). As for the designed product, only SDA line (input/output) is bidirectional therefore charging resistor on SCL line is not necessary. Resistor nominal value is limited **at the bottom** - by load capability of microcircuit (I_{OL}=3,0 mA), **at the top** - by the build-up font duration (t_R=1,0 **μs**). Operation of the microcurcuit is stable within the resistance range from 1,5 kOhm up to 10 kOhm. The **possible** operation modes of I²C-bus are showed in figure 2.

Operation modes of I²C-bus

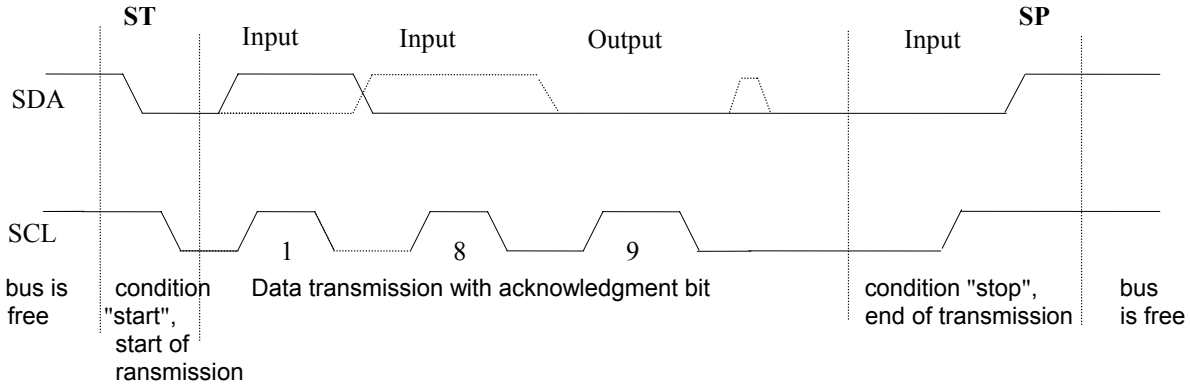

Fig. 2

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The following modes of I²C-bus are defined:

- bus is free (not engaged) - both lines are in "high" mode;
- transmission start (condition "Start") - passing of the line SDA from "high" level to "low" when SCL is in "high" mode;
- data transmission;
- end of transmission (condition "Stop") - passing of the line SDA from "low" level to "high" while the line SCL is in "high" mode.

The data transmission can start only when the bus is free. During the data transmission the data line must be stable all the time while clock line is “high”. The SDA line mode can change only when the clock signals line SCL is in “low” mode. One clock signal falls at one data bit. The change in SDA line mode when Clock line is “high” will be interpreted as check signals: “Start” or “Stop”.

Each transmission of data starts with the condition “Start” and is finished with the condition “Stop”. The information is always transmitted in bytes. The number of data bytes transmitted between the conditions “Start” and “Stop” is limited in “Erasure/recording” mode and not limited in “Reading” mode. Each word of 8 bits (each byte) is accompanied by the 9th test bit, acknowledgment bit. This bit is always generated on SDA line by the **device** which received the previous data byte (i.e. “receiver”). The **device** acknowledging the receipt of the data (if it meets the requirements), rarefies the SDA line so that this line is constantly “low” during all period of “high” level of clock acknowledgment pulse (9th bit) on SCL line. The device transmitting the data during acknowledgment **forming** must take the **mode** with high output resistance. If the received data byte does not comply with the requirements, the receiving **device** does not generate the acknowledgment which indicates to the error in exchange protocol on I²C-bus.

All devices connected to I²C-bus may be devided in two groups: «main» devices which control the data transmission along the bus (microcontrollers, microprocessors), and «subordinate» devices, which are controlled by «main» devices (service and peripheric devices). In their turn the both groupsof devices may be as «receivers» (devices receiving the data at that moment) and «transmitters» (devices transmitting the data the bus). The designed microcircuit INF8582E may be only «subordinate receiver» or «subordinate transmitter».The time diagram of I²C-bus is showed in fig.3. Signal parameters of I²C-bus time diagram are given in table 2.

I²C-bus time diagram

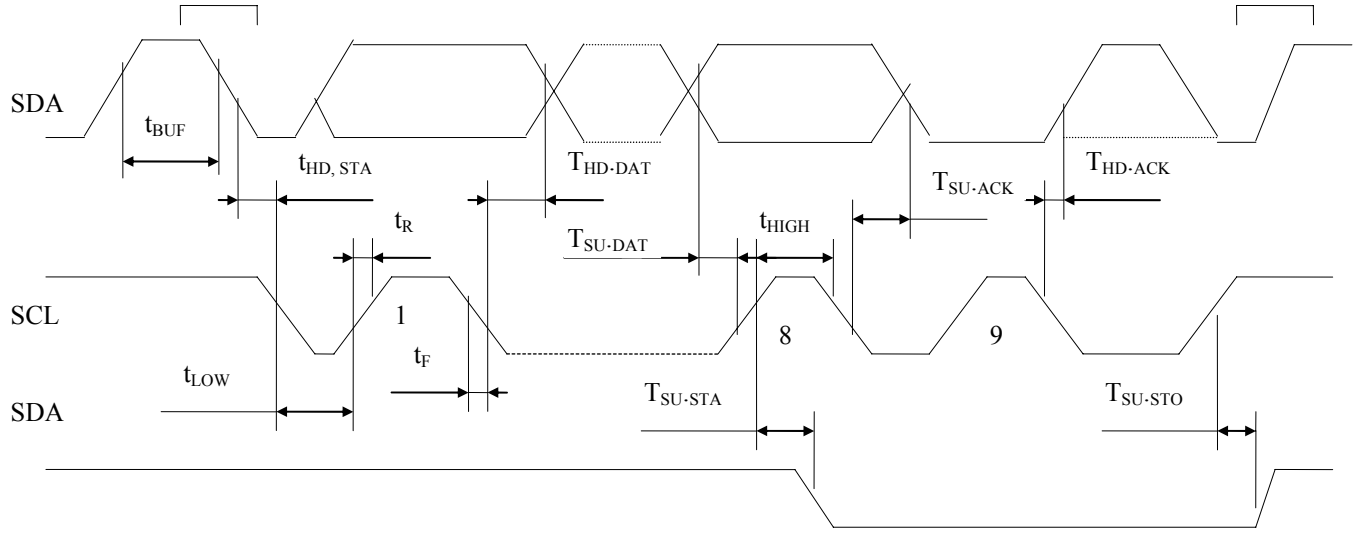

Fig. 3

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Table 2 Signal parameters on I²C-bus

Parameter name, unit of the measurement	Symbol	Value		Notes
		min	max	
Time when the bus is free before generation of «start» condition, μs	t_{BUF}	4.7	-	
Condition«start» set up time, μs	$T_{SU\cdot STA}$	4.7	-	1
Condition «start» retention time, μs	$t_{HD\cdot STA}$	4.0	-	
«Low» period of clock signal, μs	t_{LOW}	4.5	-	
«High» period of clock signal, μs	t_{HIGH}	4.0	-	
Rise front duration, ns	t_R	-	1.0	
Fall front duration, ns	t_F	-	300.0	
Data retention time,ns	$t_{HD\cdot DAT}$	0	-	2
Data retention time, μs	$t_{HD\cdot DAT}$	5.0	-	3
Data set up time, ns	$t_{SU\cdot DAT}$	250.0	-	
Acknowledgment generation time, μs	$t_{SU\cdot ACK}$	-	3.5	
Acknowledgment retention time, μs	$t_{HD\cdot ACK}$	0	-	
Condition «Stop» set up time, μs	$t_{HD\cdot STO}$	4.7	-	

Notes: 1. For repeated start.
2. Microcircuit INF8582E is a "subordinate transmitter".
3.Microcircuit INF8582E is a "subordinate receiver".

Among the parameters stipulated in table 2 the particular attention should be paid to set up and data retention time. Two modes should be considered.

The first mode.

Первый режим. Microcircuit INF8582E receive data, i.e. is a "subordinate receiver. In this case time $t_{SU.DAT}$ and $t_{HD.DAT}$ must be garanteed by "main transmitter". "Latchup" of data being received in microcircuit is effected onback front of clock pulse.

The second mode. Microcircuit INF8582E generate a data which goes to the line SDA, i.e.. is a " subordinate transmitter". In this case time $t_{SU.DAT}$ and $t_{HD.DAT}$ are determined by the microcircuit parameters. True information on the line SDA is set by back front of the previous clock pulse. In other words, usefull information is already on the leading edge of the next clock pulse on the line SDA.

The protocols of I²C -bus for all microcircuits operating modes are shown in fig. 4-6, in fig.7 - time diagram of signals on the bus in the mode «erasure/recording» using external master oscillator. The signal parameters in the mode «erasure/recording» are stated in table 3, in tables 4,5 - interpretation of key words and symbols, **used for presentation of these protocols.**

I²C-bus protocol in the «Reading » mode with input of word address

S T	CS/WR	A s	WA	A s	S T	CS/R D	A s	DA	Am	DA	Am	SP
								n bytes		last byte		

↑
automatic increment of word being read-out

Fig. 4

I²C-bus short protocol in the mode "Reading"

ST	CS/RD	As	DA	Am	DA	Am	SP

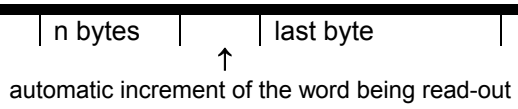


Fig. 5

The particularity of protocols in the mode «Reading» is the change of direction of the data transfer on SDA line: before the end of the control word CS/RD microcircuit receives the information and **afterwards the data transfer (read-out)** Once setting the protocol it is possible to read-out an unlimited number of data bytes sequentially. After each byte is read-out embedded address counter automatically get an increment of «unit» after having received the acknowledgment from «main receiver» (Am=0). And so on up to the address 256. When the counter is overfilled «zero» address is initialized. Straight away after Acknowledgment clock pulse **negative front** (in case if As or Am=0) microcircuit output is lowimpedence and the first bit of the read-out information byte is set on SDA line. In case of the transfer by microcircuit («sabordinate transmitter») of the last byte «main receiver» has to transmit to «sabordinate transmitter» the information about the end of receit (Am=1), not to generate a sygnal conforming the receipt. In this case after Acknowledgment clock pulse back front output of microcircuit is set in the condition with high output resistance (is closing), high level is set on SDA line permitting «main receiver» to generate the condition «Stop».

Short protocol of the mode “Reading” (without writing the address of word being read-out) is used if while working with the microcircuit (without turning off supply voltage) the necessity to continue reading from the last address occured.

I^2C-bus short protocol in the mode "erasure/зrecording"

ST	CS/WR	As	WA	As	DE	As	DE	As	SP

automatic increment of the word being read-out

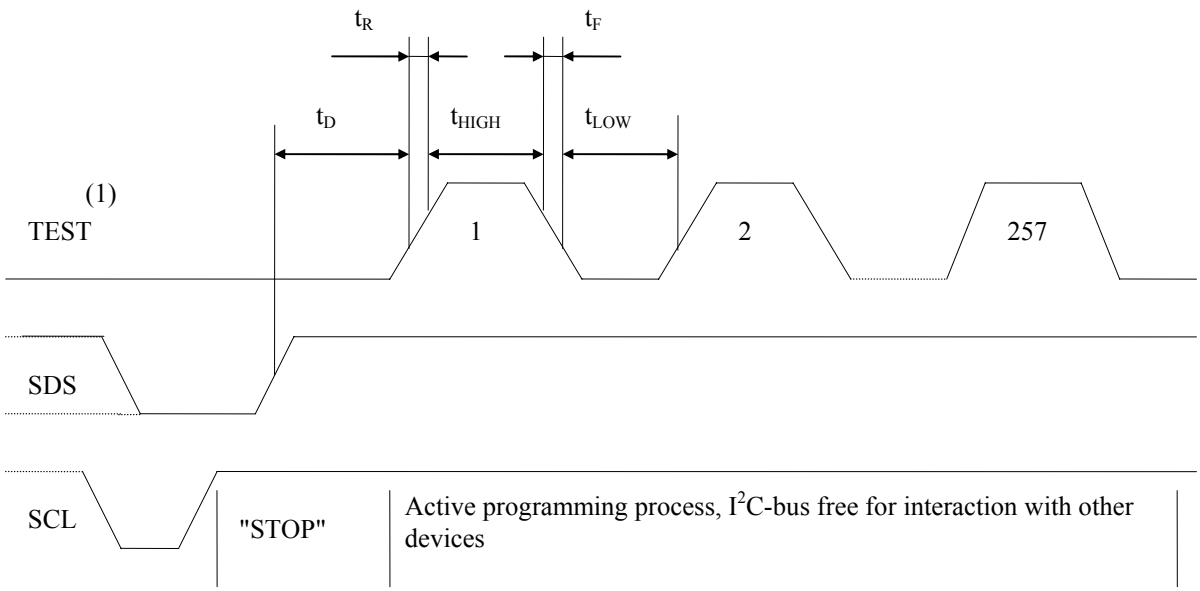
Fig. 6

The active reprogramming process starts after **supply** of the whole protocol on generating condition “Stop”. The presence of the second data byte is not necessary. In one cycle ‘erasure/recording’ no more than two information bytes may be programmed. The programming can be effected under embedded control (the internal programming master oscillator is used), as well as using external generator.

If an internal generator is meant to be used, high level must be set on output “TEST" or it must be let free (inside the chip this output is connected to the bus Ucc through resistor approx. **1**,5 **кOhm**). In this case programming cycle duration depends on the manufacturing process, it is equal to 10.0 - 15.0 ms when recording one data byte and 20.0 - 25.0 ms - two.

When using external master oscillator on output “Test” low level must be set preliminary. The information on logical state on this particular output is **fixed** after supplying the 8th bit of the address byte (along clock sygnal **back front**). Time diagram is generated on I²C-bus as per fig.7.

Time diagram of signals in the mode "erasure/recording" of one information byte when using external generator.



1 - in the mode "erasure /recording" two information bytes 513 pulses are applied to the input «TEST». Programming cycle duration for 1 byte is approximately 5ms, when recording two bytes - 10 ms.

Fig. 7.

Таблица 3

Parameter name, measurement unit	Symbol	Min	Max
Input "TEST" clock frequency, кHz	f_P	10	50
Duration of the "high", mks	t_{HICH}	10	-
Duration of the "low", mks	t_{LOW}	10	-
Duration of the rise front, ns	t_R	-	300
Fall front duration, ns	t_F	-	300
Delay time, mks	t_D	0	t_{LOW}

Table 4 - Control words

Word name	Word byte No 01	02	03	04	05	06	07	08	Purpose	9-th bit (acknowledgment bit after the word)
CS/WR	1	0	1	0	A2	A1	A0	0	word of chip selection for recording information in m/c	"0", acknowledgment from m/c
CS/RD	1	0	1	0	A2	A1	A0	1	Word of chip selection for reading data from m/c	"0", acknowledgment from m/c
WA	X7	X6	X5	X4	X3	X2	X1	X0	word of byte address, which is addressed to	"0", acknowledgment from m/c
DE	D7	D6	D5	D4	D3	D2	D1	D0	Data word for recording in microcircuit EEPROM	"0", acknowledgment from m/c
DA	D7	D6	D5	D4	D3	D2	D1	D0	Data word read-out from m/c EEPROM	"0" or "1" from the "main"

The word of chip selection consists of several parts.

- bits 1-4 are strictly defined combination, programmed inside chip;
- bits 5-7 (selection bits of device A2-A0) make achievable the connection of 8 memory devices to the bus. Выбор определенного прибора достигается, если логическое состояние данного бита соответствует распайке выводов корпуса A2-A0 на плате. Если выводы на плате не подключены, то в слове выбора кристалла биты 5-7 должны иметь "низкий" логический уровень, так как по включению напряжения питания эти входы внутри кристалла сбрасываются в "0";
- 8 bit define action ("0" – writing of data to circuit, "1" – reading of data);

Developed circuit play role of “Slave receiver” in work with most cases of control words and provide confirmation, exception is case of reading of data, when a external device (“Host receiver”) provide the confirmation .

Table 5 -

Symbol	Definition
ST	START
SP	STOP
As	Confirmation bite from circuit
Am	Confirmation bite from “Host receiver”
X0 - X7	Address bits of byte
D0 - D7	Data bits