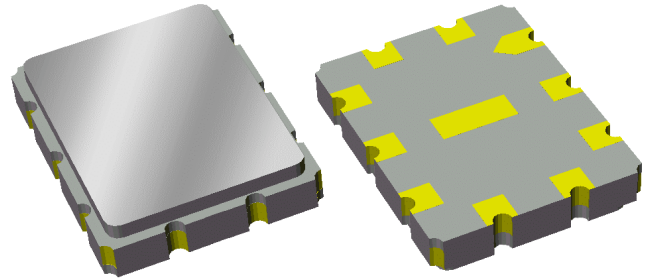


# Preliminary Data Sheet

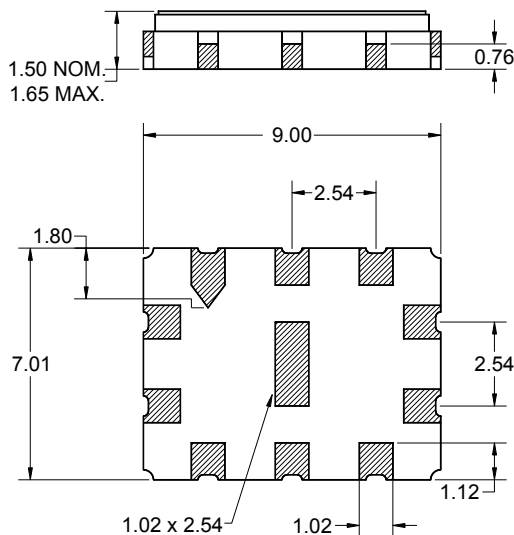
## Features

- For broadband applications
- Typical 3dB bandwidth of 57.0 MHz
- High attenuation
- Single-ended operation
- Ceramic Surface Mount Package (SMP)
- Small size
- Replaces Sawtek P/N 851947 (BW 3dB=56 MHz)



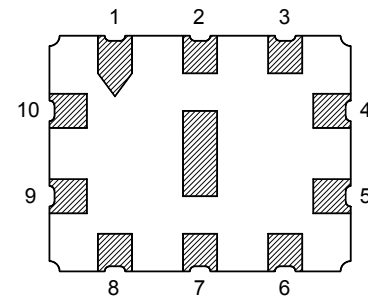
## Package

Surface Mount 9.00 x 7.01 x 1.50 mm



## Pin Configuration

Bottom View



Pin No.	Description
4	Output
5	Output return
9	Input
10	Input return
1,2,3,6,7,8	Case ground

Dimensions shown are nominal in millimeters  
 All tolerances are  $\pm 0.15$ mm except overall  
 length and width  $+0.10$ mm/ $-0.15$ mm

Body:  $Al_2O_3$  ceramic  
 Lid: Kovar, Ni plated  
 Terminations: Au plating 0.5 - 1.0  $\mu$ m,  
 over a 2 - 6  $\mu$ m Ni plating

# Preliminary Data Sheet

## Electrical Specifications <sup>(1)</sup>

Operating Temperature Range: <sup>(2)</sup> 0 to +70 °C

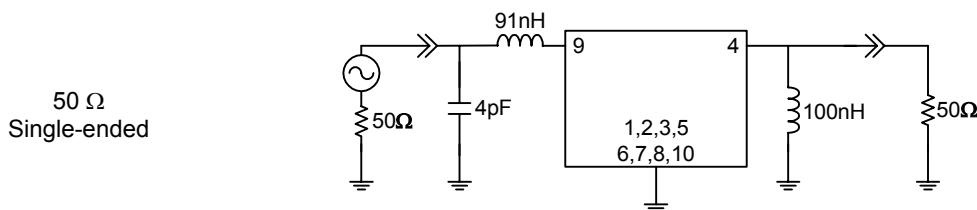
Parameter <sup>(3)</sup>	Minimum	Typical	Maximum	Unit
Center Frequency	-	140	-	MHz
Minimum Insertion Loss	-	18.65	19.5	dB
Lower 1 dB Bandedge <sup>(4)</sup>	-	112.7	115.75	MHz
Upper 1 dB Bandedge	164.25	166.1	-	MHz
Lower 3 dB Bandedge <sup>(4)</sup>	-	111.4	112.80	MHz
Upper 3 dB Bandedge	167.20	168.4	-	MHz
Lower 40 dB Bandedge <sup>(4)</sup>	102.20	106.3	-	MHz
Upper 40 dB Bandedge	-	176.4	177.80	MHz
Amplitude Variation 115.75 - 164.25 MHz	-	0.60	1.15	dB p-p
Phase Linearity 115.75 - 164.25 MHz	-	4.07	7.75	deg p-p
Group Delay Variation 115.75 - 164.25 MHz	-	31	60	ns p-p
Absolute Delay	-	0.531	-	μsec
Relative Attenuation <sup>(4)</sup>				
10 - 27.5 MHz	49	58	-	dB
27.5 - 102 MHz	39	42	-	dB
178 - 252.5 MHz	37	42	-	dB
252.5 - 300 MHz	36	44	-	dB
Terminating Source Impedance: <sup>(5)</sup>	-	50	-	Ω
Terminating Load Impedance: <sup>(5)</sup>	-	50	-	Ω
Substrate Material	-	128 LiNbO <sub>3</sub>	-	-
Temperature Coefficient of Frequency	-	-74	-	ppm/°C

### Notes:

1. All specifications are based on the test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature and manufacturing tolerances
4. All attenuation measurements are measured relative to minimum insertion loss
5. This is the optimum impedance in order to achieve the performance shown

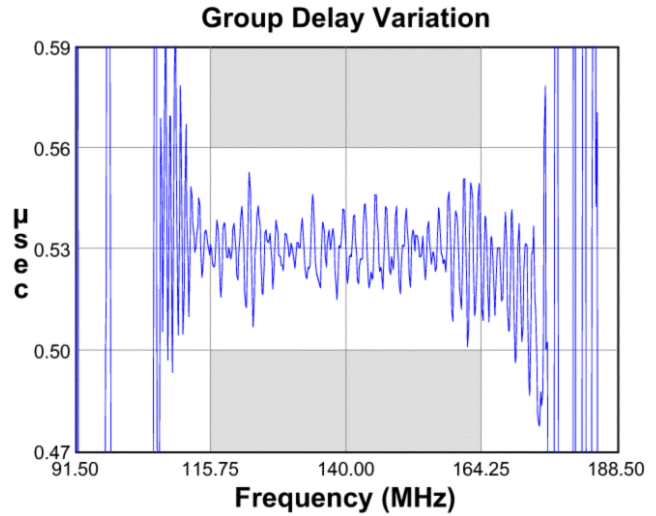
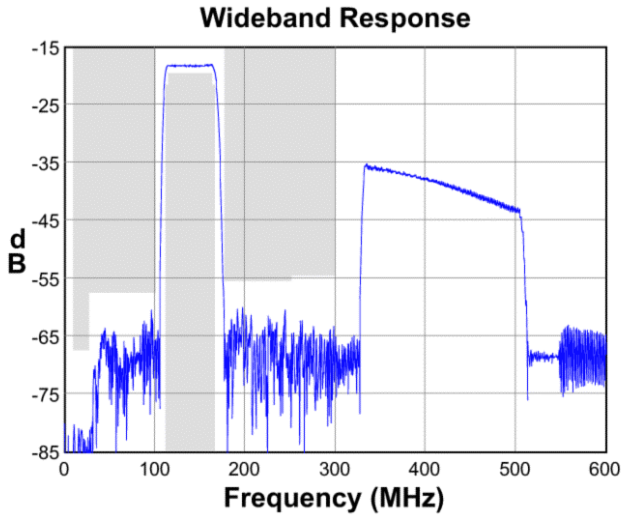
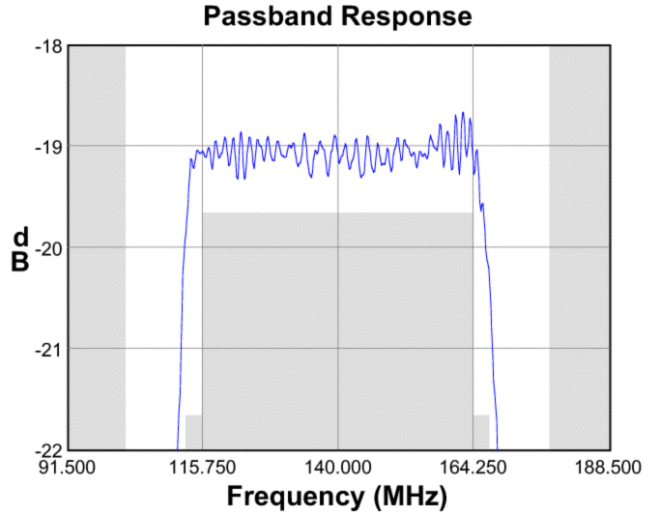
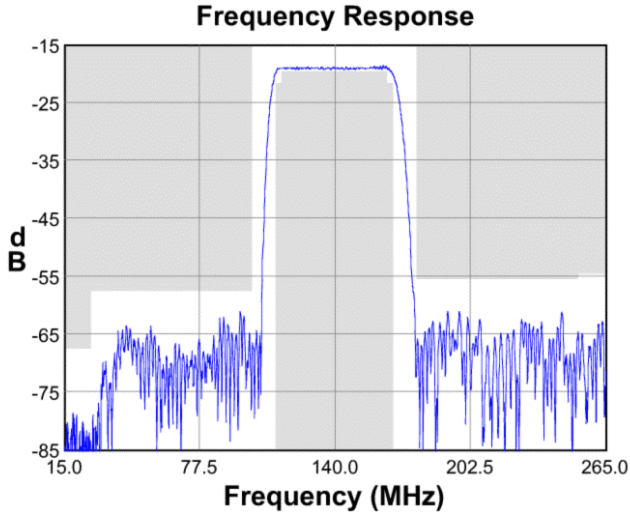
### Test Circuit:

Actual matching values may vary due to PCB layout and parasitics

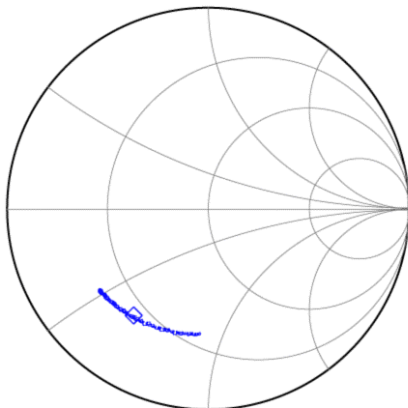


**Preliminary Data Sheet**

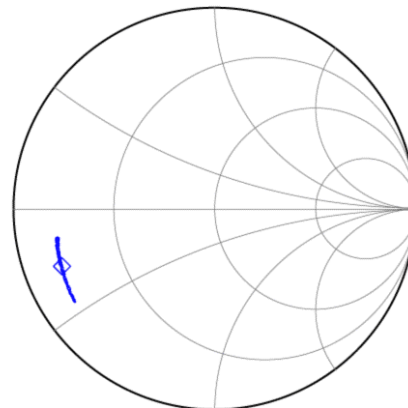
**Typical Performance (at +25°C)**



**Input Smith Chart**



**Output Smith Chart**






# Preliminary Data Sheet

## Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating Temperature Range	T	0	+25	+70	°C
Storage Temperature Range	T <sub>stg</sub>	-40	-	+85	°C

### Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

## Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[Reel and Packaging Label](#)

[Other Technical Information](#)

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