

**Thick Film Resistor Networks, Dual-In-Line,
Small Outline Molded Dip, 01, 03, 05 Schematics, 16 or 20 Pins**



FEATURES

- 0.110" [2.79mm] maximum seated height
- Rugged, molded case construction
- 0.050" [1.27mm] lead spacing
- Reduces total assembly costs
- Compatible with automatic surface mounting equipment
- Uniform performance characteristics
- Meets EIA PDP 100, SOGN-0003 outline dimensions
- Available in tube pack or tape and reel pack

STANDARD ELECTRICAL SPECIFICATIONS							
MODEL	SCHEMATIC	RESISTOR CIRCUIT W @ 70°C	PACKAGE POWER W @ 70°C	TOLERANCE ± %	RESISTANCE RANGE Ω	OPERATING VOLTAGE VDC	TEMPERATURE COEFFICIENT ppm/°C
SOGC-16	01	0.1	1.6	2 (1, 5*)	10-1M0	50 max	100
	03	0.19	1.6	2 (1, 5*)	10-1M0	50 max	100
	05	0.1	1.6	2 (5*)	10-1M0	50 max	100
SOGC-20	01	0.1	2.0	2 (1, 5*)	10-1M0	50 max	100
	03	0.19	2.0	2 (1, 5*)	10-1M0	50 max	100
	05	0.1	2.0	2 (5*)	10-1M0	50 max	100

* Tolerances in brackets available upon request.
 • 100 milliohm maximum on zero ohm jumper

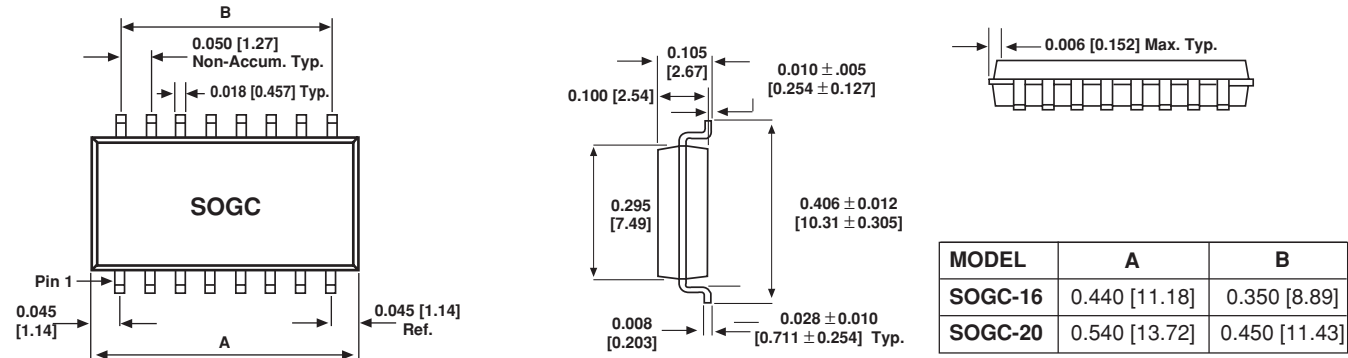
TECHNICAL SPECIFICATIONS		
PARAMETER	UNIT	SOGC-16 / -20
Package Power Rating (max. at + 70°C)	W	1.6 / 2.0
TC Tracking (- 55°C to + 125°C)	ppm/°C	± 50
Voltage Coefficient of Resistance:	ppm/V	< 50 typical.
Maximum Operating Voltage:	VDC	50
Operating Temperature Range:	°C	- 55 to + 125.
Storage Temperature Range:	°C	- 55 to + 150

MECHANICAL SPECIFICATIONS	
Marking:	Model number, schematic number, value tolerance, pin 1 indicator, date code.
Marking Resistance to Solvents:	Permanency testing per MIL-STD-202, Method 215.
Maximum Solder Reflow Temperature:	+ 255°C
Solderability:	Per MIL-STD-202, Method 208E.
Terminals:	Copper alloy. 60/40 solder dipped terminal.
Body:	Molded epoxy.

ORDERING INFORMATION					
01, 03 Schematic	16 20 NUMBER OF LEADS	01 03 SCHEMATIC	xxx or xxxx R ₁ VALUE	G TOLERANCE	
			First 2 digits (3 for F tolerance) are significant figures. Last digit specifies number of zeros to follow.	F = ± 1% G = ± 2% J = ± 5%	
05 Schematic	16 20 NUMBER OF LEADS	05 SCHEMATIC	xxx or xxxx R ₁ VALUE	xxx or xxxx R ₂ VALUE	G TOLERANCE
			First 2 digits (3 for F tolerance) are significant figures. Last digit specifies number of zeros to follow.	F = ± 1% G = ± 2% J = ± 5%	



DIMENSIONS in inches [millimeters]



CIRCUIT APPLICATIONS

01 Schematic

15 or 19 resistors with one pin common
 The SOGC-xx01 circuit provides a choice of 15 or 19 nominally equal resistors, each connected between a common lead (16 or 20) and a discrete PC board pin. Commonly used in the following applications:

- MOS/ROM Pull-up/Pull-down
- TTL Input Pull-down
- Open Collector Pull-up
- Digital Pulse Squaring
- "Wired OR" Pull-up
- TTL Unused Gate Pull-up
- Power Driven Pull-up
- High Speed Parallels Pull-up

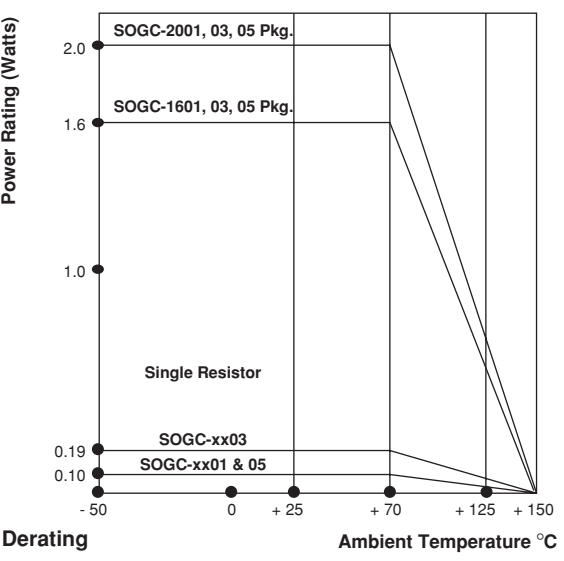
03 Schematic

8 or 10 isolated resistors
 The SOGC-xx03 circuit provides a choice of 8 or 10 nominally equal resistors with each resistor isolated from all others and wired directly across. Commonly used in the following applications:

- "Wired OR" Pull-up
- Long-line Impedance Balancing
- Power Driven Pull-up
- LED Current Limiting
- Powergate Pull-up
- ECL Output Pull-down
- Line Termination
- TTL Input Pull-down

05 Schematic

TTL dual-line terminator; pulse squaring, 14 or 18 pairs of resistors
 (R_1 Resistors are common to leads 16 or 20)
 (R_2 Resistors are common to leads 8 or 10)
 The SOGC-xx05 circuit contains 14 or 18 pairs of resistors. Each pair is connected between ground and a common line. The junctions of these resistor pairs are connected to the input leads.
 The 05 circuits are designed for TTL dual-line termination and pulse squaring.



PERFORMANCE	
TEST	MAX. ΔR (Typical Test Lots)
Power Conditioning	± 0.50% ΔR
Thermal Shock	± 0.50% ΔR
Short Time Overload	± 0.25% ΔR
Low Temperature Operation	± 0.25% ΔR
Moisture Resistance	± 0.50% ΔR
Resistance to Soldering Heat	± 0.25% ΔR
Shock	± 0.25% ΔR
Vibration	± 0.25% ΔR
Load Life	± 0.50% ΔR
Terminal Strength	± 0.25% ΔR
Insulation Resistance	10,000 Megohm (minimum)
Dielectric Withstanding Voltage	No evidence of arcing or damage (200 V RMS for 1 minute)