FEATURES

- **20 clock outputs at primary frequency up to 80 MHz**
- **Leading edge skew for all outputs ≤0.5 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50–75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

APPLICATIONS

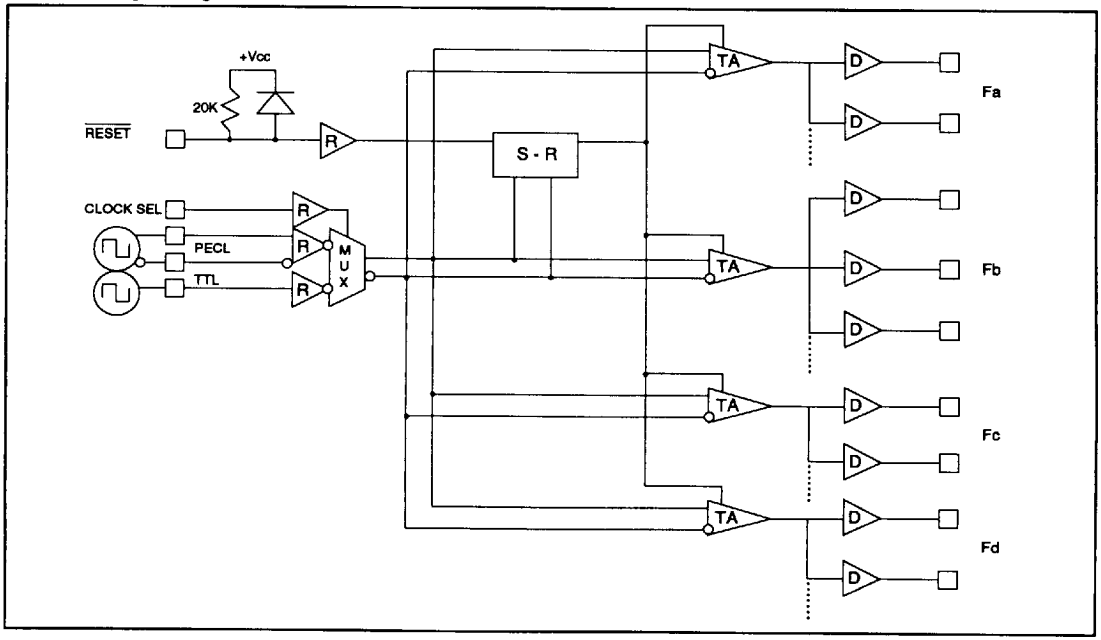
- **Datacom and Telecom networks**
- **Compatible with Intel's Pentium™ processor**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**

GENERAL DESCRIPTION

The SC3508 is a minimum skew clock driver with 20 outputs. It can employ a clock input from a single-ended TTL or an ECL differential source operating between +5V and ground (PECL). This reference frequency input is received and distributed to the clock output drivers.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output-switching noise and distortion.

Figure 1. Logic Diagram



Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package and die total)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

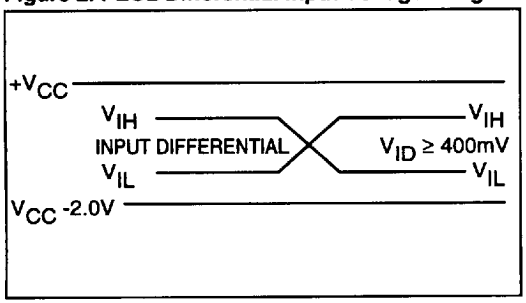
Table 1. Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference Figure 4, AC Test/Evaluation Circuit)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs including Clock	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs including Clock	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	Reset	V_{IN} = 2.4V		-200	uA
	TTL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		25	uA
	Reset	V_{IN} = 0.5V		-325	uA
	TTL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz max C_L = 10pF	2.4		V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz max C_L = 10pF		0.6	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-55		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Core Power Dissipation	Ref. Table 3 @ 70°C, Typ Pwr=340mW		550	mW

1. Maximum test duration, one second.
2. The SC3508 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

Figure 2. PECL Differential Input Voltage Range



DC Characteristics

The SC3508 has been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high-drive, totem-pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the SC3508 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -8mA	2.4V	
V_{OL}	I_{OL} = 4mA		0.6V

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Table 2. AC Specifications—Using Figure 4, AC Test/Evaluation Circuit

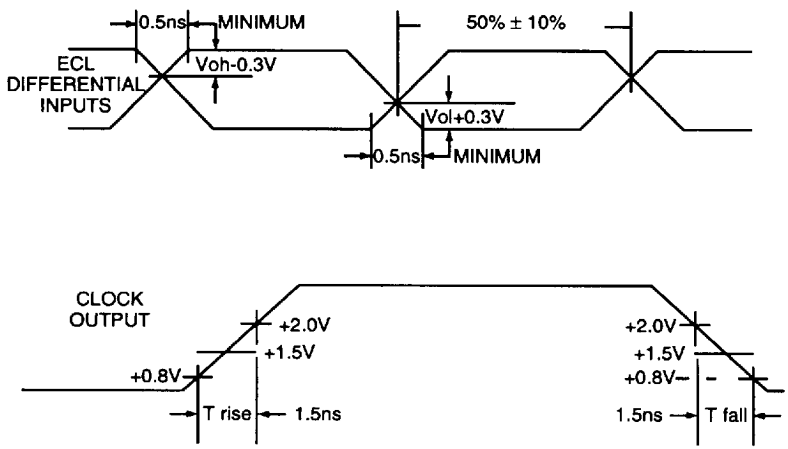
V_{CC} = +5.0V ± 5%, T_a = 0°C to 70°C, C_{LOAD} = 10pF

Parameter	SC3508-2	SC3508-1	SC3508	Units
Maximum Skew Across All Outputs	0.5	0.5	1.0	ns
Maximum Skew Chip to Chip	1.0	—	—	ns
Maximum Skew Across Fa, Fb, Fc, or Fd Outputs	0.25	0.25	0.25	ns
Maximum TTL Input Frequency	80	80	80	MHz
Maximum PECL Differential Input Frequency	80	80	80	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Chip-to-chip skew specification valid only for parts operating at the same voltage and temperature. It is derated at 0.5 ns/V and 10 ps/°C. Chip-to-chip skew tested at 70°C.
3. The SC3508 output symmetry follows input symmetry. Output Duty Cycle will also be affected by voltage and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10pF capacitive load. See "Real Load" evaluation circuit. Synchronous outputs may be paralleled for higher loads.
6. Parameters guaranteed by design and characterization.

Figure 3. Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See the Clock Driver Application Note.

10

DESCRIPTION OF OPERATION
(Refer to Logic Diagram)

AMCC has developed a single-chip clock buffer and twenty-output fanout driver using AMCC's advanced BiCMOS process. This design has been optimized for absolute minimum skew across all twenty outputs.

For best performance, this approach will require a clock source input from a crystal controlled oscillator (XCO) located adjacent to this clock driver. This oscillator can provide either differential ECL inputs (referenced to +5V, PECL) or TTL (CMOS) input levels to AMCC's Clock Driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to translation amplifiers and output drivers, (refer to the Figure 1, Logic Diagram). The output duty cycle asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

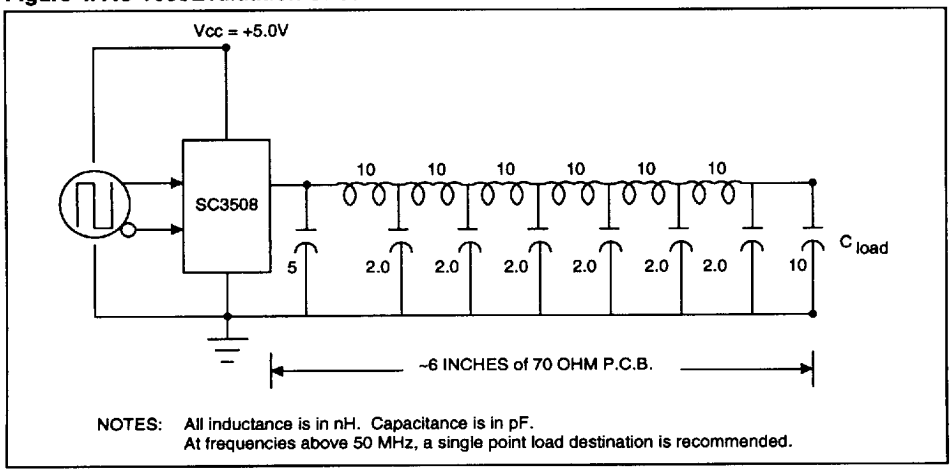
The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100ms) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling edge clock inputs. At the expiration of RESET (high) outputs will resume, after four falling edge clock inputs, from a high (leading edge) count origin.

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note).

Power and ground are interdigitated with the outputs. Of the 52 package pins, 24 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to ensure that the SC3508 will exhibit skews less than the specified maximum. A plastic 52-lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

Figure 4. AC Test/Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF.
At frequencies above 50 MHz, a single point load destination is recommended.

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Power Management

The overall goal of managing the power dissipated by the SC3508 is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the SC3508 is determined by the load that each output drives and the frequency that each output is running. Table 3 summarizes these dependencies (see Figure 4, AC Test/Evaluation Circuit, for complete load definition).

The output power must be added to the core power (550 mW) of the SC3508 to determine the total power being dissipated by the SC3508. This total power is then multiplied by the SC3508's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC3508. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the SC3508 is detailed in the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an SC3508 with 12 outputs driving 15 pF loads at 50 MHz. Total chip power is calculated as follows:

Core Power = 550 mW

12 outputs, 15 pF, 50 MHz = (12 x 39 mW) = 468 mW
8 outputs, no load, 50 MHz = (8 x 14 mW) = 112 mW

Total Power = 1130 mW

The design specifies a 70°C still air ambient. Referring to the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 46.2°C/watt. The SC3508's junction temperature would then be:

70°C + (1.13 watts x 46.2°C/watt) = 122°C

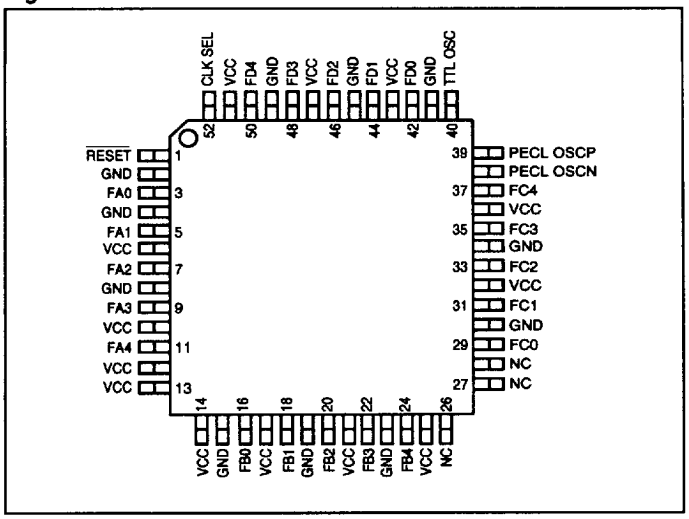
Note this is below the 140°C maximum junction temperature.

Table 3. Output Power Dissipation

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	10 mW

10

Figure 5. SC3508 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**

SC3508 **Q** **–1** **/TD**

Optional Shipping Configuration
Blank = 84-unit matrix tray
/D = dry pack
/TD = tape, reel and dry pack

Skew Option
Blank = 1.0 ns output-output skew
–1 = 500 ps output-output skew

Package Option
Q = 52-pin Plastic Quad Flat Pack (PQFP)

Device Number

Example: SC3508Q–1/D
52-pin PQFP package, 500 ps output-output skew, shipped dry packed in the standard matrix tray.