VAN peripheral circuit - 16 inputs-outputs

1. Features

- Management of 16 inputs-outputs (16-bit or two 8-bit configurable ports)
- VAN protocol V4.0
- 3 external wired address
- Safety mode in case of transmission loss
- Automatic adaptation to speed of bus from 8kTS/s to 250kTS/s
- CMOS 0,5µm, IO CMOS TTL compatible
- Internal power-on-reset
- Internal ring oscillator from 10 to 40MHz (for internal clock)
- 500kHz oscillator with external RC network (for safety mode clock usage)
- Supply voltage 5V±10%
- Typical power consomption 4mA
- SO28 package

2. General description / block diagram

The block diagram given below shows the organization of the circuit as two blocks: the VAN controller (block 1), and the groups of specific functions (block 2) relative to the TSSIO16E. These are based on management of 16 inputs-outputs grouped together to form two 8-bit bi-directional programmable ports: port A and port B. The circuit thus ensures double exchange of information with the VAN bus (via the line interface) on the one hand and the active environment on the other.

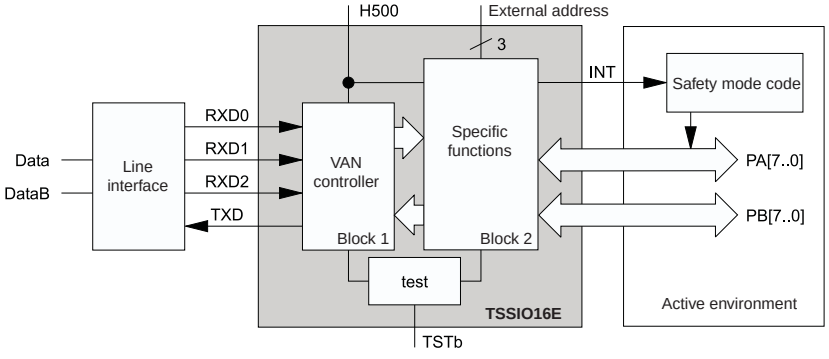


Figure 1.

The bus data is supplied to the circuit (after shaping by the line transmitter/receiver) through 3 input lines RXD0, RXD1 and RXD2 selected one after another when communication on one of the lines is defective (line diagnosis system). Operation outside of the RXD0 line is referred to as in **degrated mode**. If perturbations persist in reception the circuit switches to the **safety mode (INT = 1)** which, by default, ensures safety functions by activating or inhibiting external circuitry. Two CONTROL and STATUS 8-bit registers, are used respectively for setting operation to a given configuration, and for diagnosing the state of the circuit.

The write and read modes of ports A and B are determined by decoding the local address of the identifier field in the VAN frame.

The behaviour of each port can be configured by three registers: DATA, DDR (Data Direction Register) and OPT (Option Register).

External address decoding by 3 pins produces 8 TSSIO16E circuits on the same bus.

3. Pinout / package

The pinout of the circuit is given below.

Table 1.

pin	**name**	**I/O**	**description**
13, 14, 15, 16, 17, 18, 19, 20	PA[0..7]	I/O	Port A, 8 bi-directional bits, TTL compatible, Schmitt trigger
22, 23, 24, 25, 26, 27, 28, 1	PB[0..7]	I/O	Port B event type, 8 bi-directional bits, TTL compatible, Schmitt trigger
2	H500	I/O	Safety mode clock connection to ground or connection of a RC dipole for 500kHz oscillator.
3	TSTb	I	In application, this input is tied to 1. In test mode, this input is tied to 0. TTL compatible with pull-up.
4	AD1	I	External wired address - TTL compatible.
5	AD2	I	
6	AD3	I	
7	RXD1	I	Receives output of comparator controlled by the Data signal from the interface circuit. TTL compatible
8	RXD2	I	Receiving the output of the comparator driven by the Data_B signal of the interface circuit. TTL compatible.
9	RXD0	I	Receives the comparator output driven by the differential (Data signal - Data_B).of the interface circuit. TTL compatible.
12	INT	O	Interrupt. Used to generate an external active safety mode. TTL compatible.
11	TXD	O	Drives the line interface circuit. TTL compatible.
10	VSS		Ground.
21	VDD		External power supply.

The package is SO28 (Figure 2).

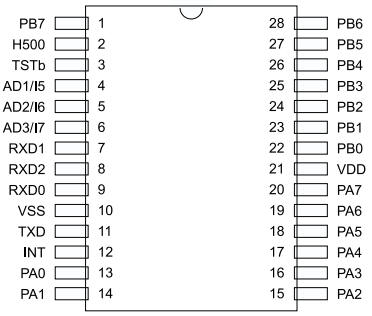


Figure 2.

4. Functional features

4.1 Content of identifier field

The TSSIO16E circuit identifier field is structured as shown below.

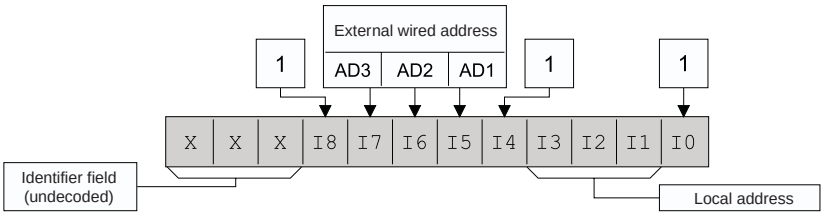


Figure 3.

The local address consists of bits I1, I2 and I3 of the identifier field for the VAN frame addressing the circuit, the Bit I1 indicates reading or writing. The table below gives the significance of these bits.

Table 2.

I3	I2	I1	local address	action
0	0	0	0	writing of VAN CONTROL register
0	0	1	1	reading of VAN STATUS register (RANK 16)
0	1	0	2	writing of port A
0	1	1	3	reading of port A (RANK 16)
1	0	0	4	writing of port AB
1	0	1	5	reading of port AB (RANK 16)
1	1	0	6	writing of port B
1	1	1	7	reading of port B (RANK 16)

4.2 Addressing of ports A and B and of COMMAND and STATUS registers

The specific functions of the circuit are activated by the selection of one or two ports depending on the local address decoding (see § 4.1) as contained in the identifier field of the VAN frame received by the circuit and by the content of the data bytes for this frame.

4.2.1 Local address 0 and 1

	I3	I2	I1
Writing of the COMMAND register	0	0	0
Reading of the STATUS register	0	0	1

Writing and reading of these registers are described in paragraph 4.4.

The writing of the COMMAND register uses a single data byte. The reading of the STATUS register sends a data byte to RANK 16.

4.2.2 Local address 2 and 3

	I3	I2	I1
Writing of port A	0	1	0

The writing of port A must be carried out with 1, 2 or 3 data bytes, otherwise the frame will not be acknowledged and not taken into consideration. If writing uses a single byte, the port will be set as output and output the DATA_A value. The automobile environment is thus affected by interference (possibility of deprogramming), it is advisable to write to ports A and B systematically using 3 bytes.

DATA_A	or	DATA_A	DDR_A	or	DATA_A	DDR_A	OPT_A

DATA_A : Output byte value for port A.

DDR_A : Defines, bit by bit, the direction of the I/O pins for port A (0 = input, 1 = output).

OPT_A : Unused register, this register must be forced to 0.

	I3	I2	I1
Reading of port A	0	1	1

A read frame RANK16 at local address 3 recovers the data byte present on port A wether the direction is input or output.

4.2.3 Local address 4 and 5

	I3	I2	I1
Writing of port A and B	1	0	0

A write frame for port A and B contains 6 bytes. The management of the DATA, DDR and OPT bytes is the same as in the case of port A alone.

DATA_A	DDR_A	OPT_A	DATA_B	DDR_B	OPT_B

OPT_B register must be forced to 0.

	I3	I2	I1
Reading of port A and B	1	0	1

A read frame (RANK 16) at local address 5 recovers of two data bytes present on port A and B wether the direction is input or output.

4.2.4 Local address 6 and 7

	I3	I2	I1
Writing of port B	1	1	0

In the same way as for port A, port B is write-accessible by frames 1, 2 or 3 data bytes.

	I3	I2	I1
Reading of port B	1	1	1

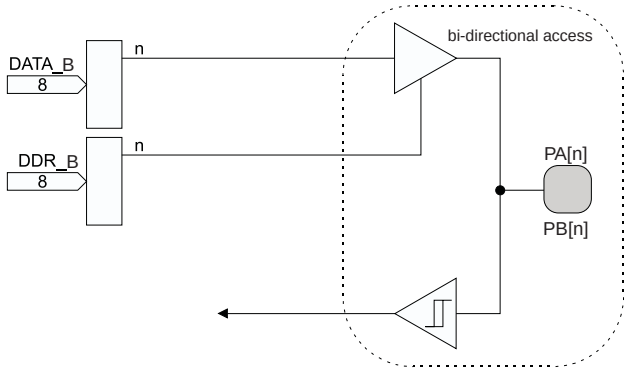
The read mechanism for port B is identical to that of port A.

4.3 Programming and structure of port A and B

Table below summarizes the programming of a port for the corresponding bits in the DATA, DDR and OPT bytes, and shows the structural organization of the logic ports.

Table 3.

OPT_X(n)	DDR_X(n)	DATA_X(n)	programming of pin n of port X
0	0	0	logic input
0	0	1	forbidden case (even input)
0	1	0	logic output set to 0
0	1	1	logic output set to 1
1	X	X	forbidden case



4.4 COMMAND and STATUS registers

These two specialized registers ensure command and monitoring functions as follows:

- Lines management according to a line diagnosis carried out constantly. This line diagnosis analyzes the transmission state and allows a choice of the RXD0, RXD1, RXD2 inputs depending on some of the TIME-OUT's (STO, MTO, LTO and SLTO);
- Accesses management to common peripherals shared by several circuits.

These registers have the following structure:

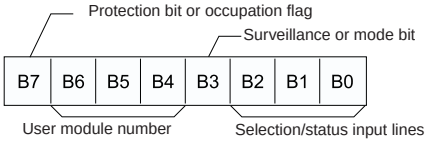


Figure 4.

4.4.1 Management of RXD0, RXD1, RXD2 lines and common access to peripherals

The purpose of line diagnosis is to find a line that operates before exiting from NORMAL mode to enter SAFETY mode. This diagnosis is covered by events or TIME-OUT's with which the time-out's are associated.

Table 4.

STO	Short time-out: the bus remains in a dominant state for a period of time incompatible with the definition of the frames.
MTO	Medium time-out: absence of coherent frame on VAN bus
LTO	Long time-out: no coherent frame addressing the circuit
SLTO	Super long time-out: 4×TOL

The duration of the time-out depends from the internal oscillator which varies in a ratio of 1 to 5. The implementing of the 500kHz external RC oscillator dedicated to the safety mode permits more accurate time delays, for example: Rext = 8.66kΩ± 5% and Cext = 1nF±5%. The tolerances on R and C include all drifts (temperature, ageing...).

Table 5.

	relative	500 kHz external oscillator					
	duration	min	typ	max	min	typ	max
STO (ms)	T/16	30	62.5	75	13	62.5	132
MTO (ms)	T/4	200	250	300	90	250	525
LTO (ms)	T	900	1000	1150	400	1000	2100
SLTO (ms)	4×T	2700	4000	4650	1200	4000	8400

4.4.1.1 Line diagnosis operation

The below shows the mechanism for changing to the safety mode. Exit from the safety mode must be managed by the application.

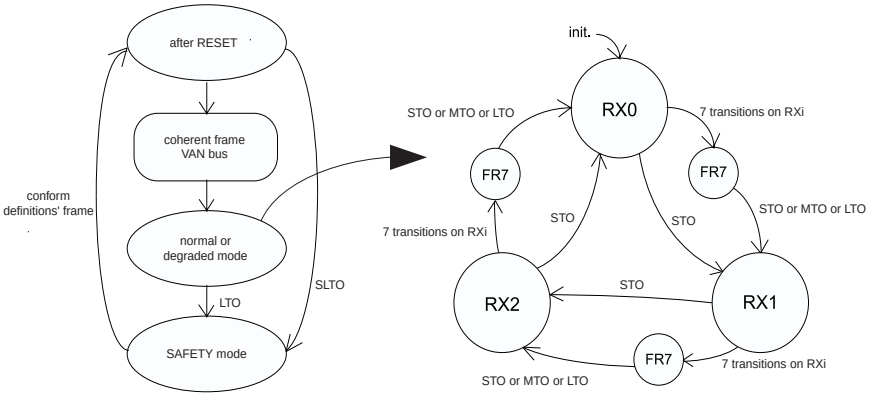


Figure 5.

Note: FR7 status corresponds to the detection of an activity on the lines.

4.4.1.2 Bits B0, B1 and B2

The 3 low significant bits of the COMMAND register define the input line and its mode of use. The 3 low significant bits of the STATUS register inform about the componant's status (line selected by the application) and the possibility of using other lines.

Table 6.

B2	B1	B0	input line selection mode COMMAND register	input line selection status STATUS register
0	0	0	automatic, initialized on RXD0	RXD0 / triple sampling incorrect
0	0	1	automatic, initialized on RXD1	RXD1 / triple sampling incorrect
0	1	0	automatic, initialized on RXD2	RXD2 / triple sampling incorrect
0	1	1	automatic transparent mode	triple sampling incorrect
1	0	0	forced to RXD0	RXD0 / triple sampling correct
1	0	1	forced to RXD1	RXD1 / triple sampling correct
1	1	0	forced to RXD2	RXD2 / triple sampling correct
1	1	1	forced to RXD0 with RXD0 = RXD1 = RXD2	triple sampling correct

- Automatic mode RDXi: successive use of lines RXD0, RXD1, RXD2, starting from RDXi.
- Automatic Transparent mode: no effect on line selection mode, allows modification of bits from B7 to B3 without modifying the selected line
- Forced mode: line unchanged in spite of presence of TIME-OUT.

The "triple sampling correct" function (RXD0 = RXD1 = RXD2) is defined by the logic condition:

E = (RXD0 x RXD1 x RXD2) + (/RXD0 x /RXD1 x /RXD2)

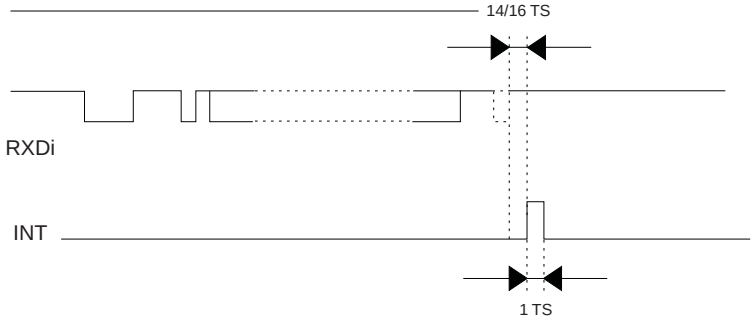
4.4.1.3 Bit B3

Bit B3 is used for activating or inhibiting line surveillance.

Table 7.

B3	COMMAND	STATUS
0	active surveillance	circuit in NORMAL mode
1	inhibited surveillance	circuit in SAFETY mode

Active surveillance: default status.
Inhibited surveillance: no more possibility to switch safety mode. Then, INT pin delivers an interruption at the end of each identified frame adressing the system.



4.4.1.4 Bits B4, B5, B6 and B7

Bits B6, B5 and B4 form an address giving the user module number (see example below). Bit B7 is a protection bit which enables or disables access to the peripheral.

Table 8.

B7	B6	B5	B4	COMMAND	STATUS
0	module			The peripheral becomes free of access	The peripheral is free of access
1				The peripheral becomes busy with a module which address is B6 B5 B4	The peripheral is busy with a module of address B6 B5 B4

Note: whatever the status mode, it is always possible to write into the command register.

Example: Case of a LCD display with a TSSIO16E shared simultaneously by car radio and vehicle computer. In this case, the car radio (B7 = 1) inhibits access to the display line until the full message is displayed.

This access control strategy is only meaningful if the computer (car radio or on-board computer) wants access to the peripheral (display) and reads the control register to ensure that the peripheral is available. Writing to the port is never inhibited.

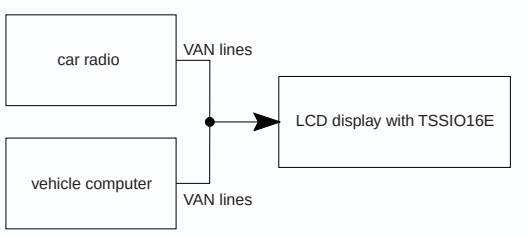


Figure 6.

4.5 State on power on and safety mode

Table 9.

	power-on	safety mode
Port A	high Z	high Z
Port B	high Z	unchanged
INT pin	0	1

This table indicates the state of ports A and B and the INT pin on power on and changeover to the safety mode. In power on mode the command register is initialized to 0.

- selection of RDX0 acces in automatic mode,
- line diagnosis activated,
- access free peripheral.

4.5.1 Condition for enter in safety mode (see Figure 5)

- After reset: in the absence of writing or reading in the circuit for a SLTO
- During operation: in the presence of coherent frames but the absence of reading or writing in the circuit for a LTO

4.5.2 Condition for exit from safety mode

Writing of port A is a way of exiting from the safety mode. Pin INT returns to 0.

5. Wiring of pin H500 (safety mode clock)

After reset and 32 clock periods, the safety mode clock switches automaticaly from internal oscillator to external clock H500.

For greater precision on safety mode temporarisations and on line diagnosis, connect a RC dipole.

Ex: (Rext = 8.66kΩ and Cext = 1nF) to pin H500 in accordance with opposite figure. It must be connected to ground in case it's not used.

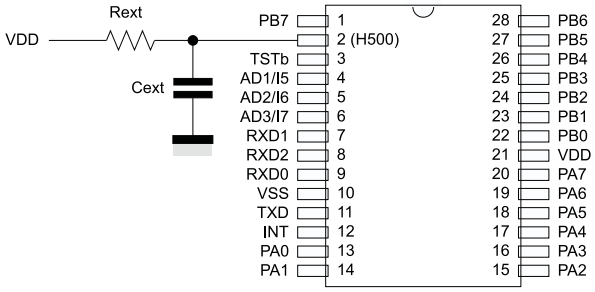


Figure 7.

6. Electrical characteristics

6.1 Consumption

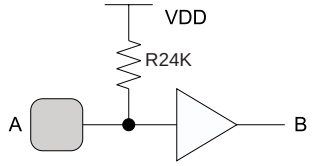
The consumption in the -40˚C / +125˚C range, whatever the VAN speed is, is given in the following table:

symbol	description	typ	max	unit	test conditions
IDD	power supply current	4	12	mA	VDD = 5V ports A and B not loaded

Table 10.

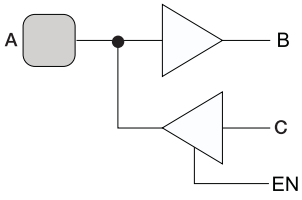
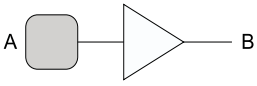
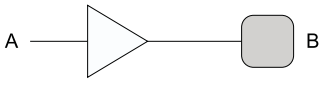
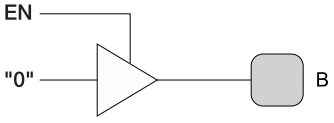
6.2 I/O's Description

The electric characteristics of the inputs-outputs are specified below. They are given for VDD = 5V±10% in the -40˚C / +125˚C temperature range.

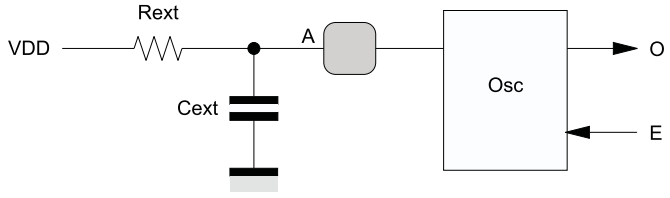
CMOS input buffer TTL compatible with pull-up (PWDF123IOTST)			
pins	see protection in § 5.3 	**A**	**B**
TSTb		L H Hi-Z	L H H

DC Characteristics

symbol	description	min	max	unit	test conditions
VIL-TTL	Input Low Voltage		0.8	V	Vcc=4.5V
VIH-TTL	Input High Voltage	2.2		V	Vcc=5.5V
IIL	Input leakage at Low level	137	400	µA	Vcc=5.5V
IIH	Input leakage at High level		13	µA	Vcc=5.5V
Isur	Transitory overcurrent of 1/10 of time		±2.5 ±5	mA mA	During 500ms max during 5 ms max and DC = 1 mA

CMOS input/output buffer TTL compatible (PWDF000IOTST)						
pins		**C**	**EN**	**A**	**B**	
PA[7..0] **PB[7...0]**		X X X L H	L L L H H	L H Hi-Z L H	L H X L H	
RxD[2...0] **AD[3...1]**		**A**		**B**		
		L H		L H		
INT		**A**		**B**		
		L H		L H		
TXD		**EN**		**A**	**B**	
		L H H		K L H	Hi-Z L H	

DC Characteristics					
symbol	**description**	**min**	**max**	**unit**	**test conditions**
VIL_TTL	Input low Voltage		0.8	V	Vcc=4.5V
VIH_TTL	Input high Voltage	2.2		V	Vcc=5.5V
VOL	Output low Voltage		0.4 0.6	V V	IOL=3mA IOL=6mA
VOH	Output high Voltage	2.4		V	IOH=6mA
IIL	Input Leakage at low level		5	µA	Vcc=5.5V
IIH	Input Leakage at high level		5	µA	Vcc=5.5V
IOZL	Output Leakage in High Z in Low level		5	µA	Vcc=5.5V
IOZH	Output Leakage in High Z in High level		5	µA	Vcc=5.5V
IOS	short-circuit current IOSN IOSP		48 36	mA mA	max duration: 1 sec EN=H Vout=Vcc Vout=Vcc
V	tension area transitorily tolerated	Vss-0.5	Vcc+0.5	V	
Isur	transitory over current of 1/10 of time		±2.5 ±5	mA mA	during 500 ms max. during 5 ms max. and DC = 1 mA

RC 500kHz oscillator (PWDOSC500C5V)				
pins		**E**	**A**	**O**
H500		H L L	X L H	FouT L H

AC/DC Characteristics					
	min	**typ**	**max**	**unit**	**test conditions**
Current consomption	400		1200	µA	
Temperature range	-40		+125	oC	
Oscillator frequency range	400	500	600	kHz	Rext = 8.66kΩ, Cext = 1nF
Cyclic ratio range	40	50	60	%	E = High

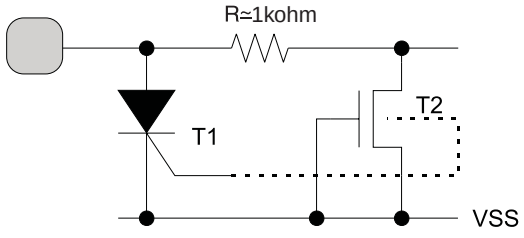
6.3 Internal clock

The internal clock is the main clock which controls all the state machines. It can be the safety mode clock if the external clock H500 is connected to ground. It is generated by a ring oscillator which frequency is given by this table:

	min	typ	Max
Temperature	-40°C	25°C	125°C
Frequency	10Mhz	22Mhz	40Mhz

6.4 Diagram of input protections

The protections types are:



The triac T1 is activated by the **substract** current of transitor T2 when the pad tension strongly increases (ESD pulse).

Figure 8.

7. Operating environment

7.1 Power supply voltage

- Nominal power supply voltage: 5V
- Operating power supply voltage: . . . . . 5V±10%
- Extreme power supply voltages not causing destruction: . . . . . -0.5V / +6V

7.2 Temperature range

- Operating temperature:. . . . . -40˚C / +125˚C
- Storage temperature: . . . . . -65˚C / +150˚C

7.3 Electrostatic discharge

- ESD protection (according to method AEC-Q100-002 rev C): . . . . . ±2kV

7.4 Overvoltages

The inputs-outputs are protected internally against overshoot and undershoot by clamping diodes.

7.5 Latch-up

Inputs-outputs are immunized to latch-up according to IEA/JESD78 norm (equivalent to AEC-Q100-004rev C). The maximum injected garanteed power is 50mW.

7.6 Shortcuts

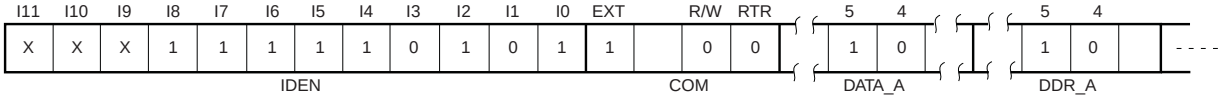
The outputs are protected against shortcuts for a maximal period of 1 second.

8. Typical application

8.1 Examples of use

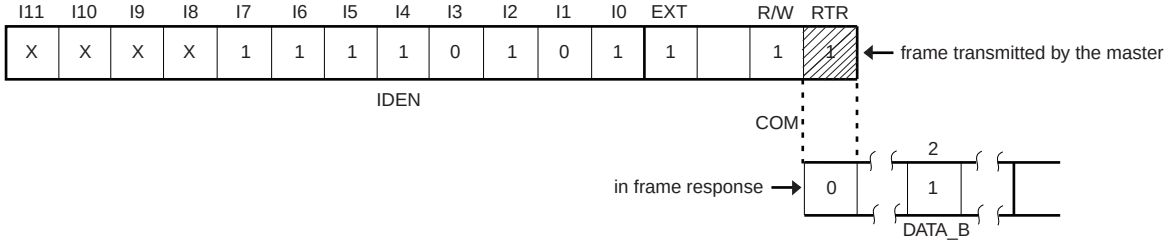
8.1.1 Headlight control (writing of port PA5)

Frame sent by central processing unit:



8.1.2 Blinkers status (reading of port PB2 - transmission RANK 16)

The TSS IO16E takes over on RTR bit of the COM field:



8.2 Circuit diagram

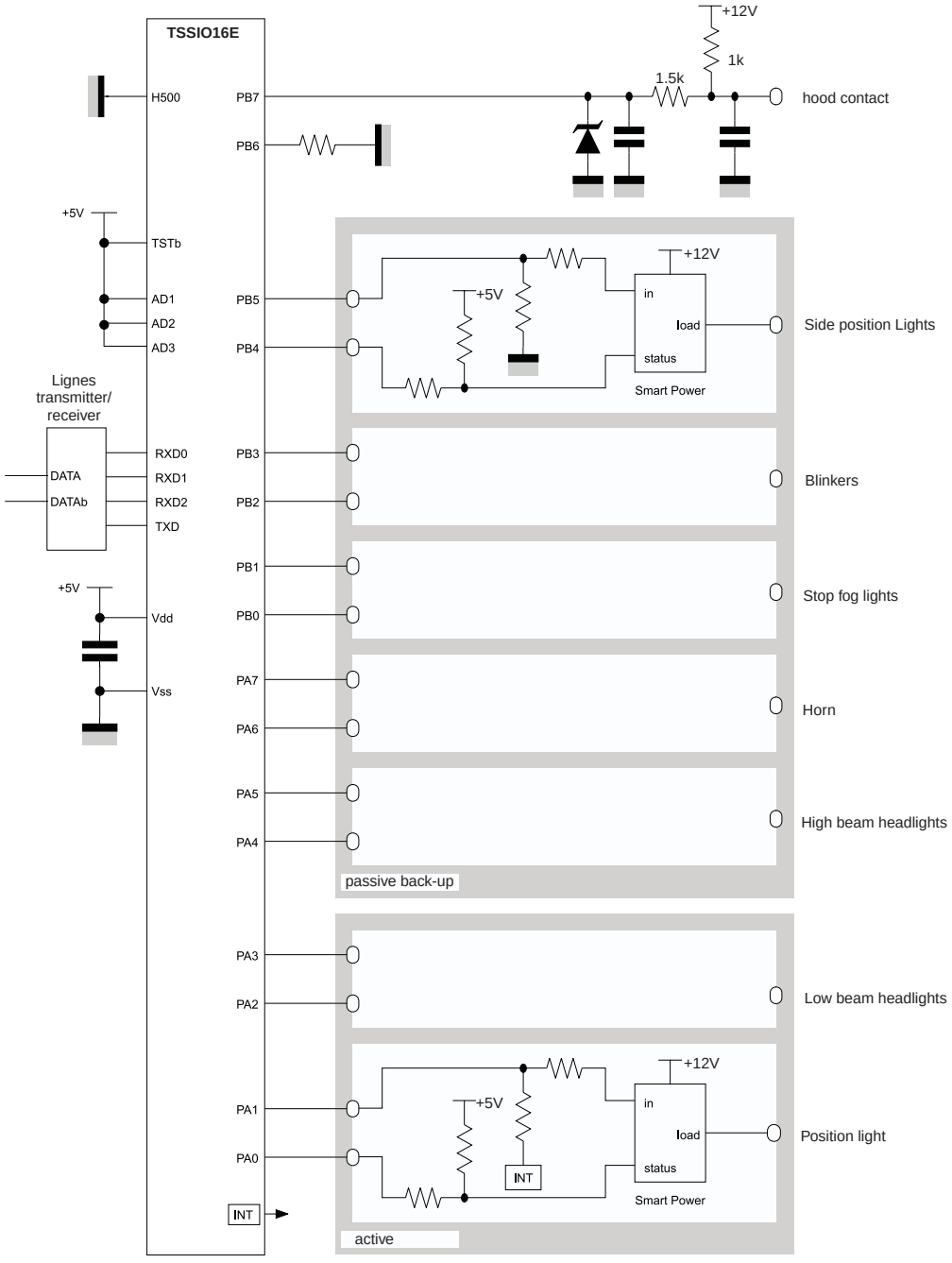


Figure 9.

Notes: *- the use of the INT pin defines the application status in safety mode*

- INT can only work on port A (configured for high impedance in safety mode)

- The unused ports PAx and PBx must be connected to ground or to Vcc via a serial resistance in order to polarize those inputs and avoid a conflict (Shortcut) in case of an output configuration.

9. Ordering information

TSSIO16E-TISA SO28 package

TSSIO16E-TIRA SO28 package Tape and Reel